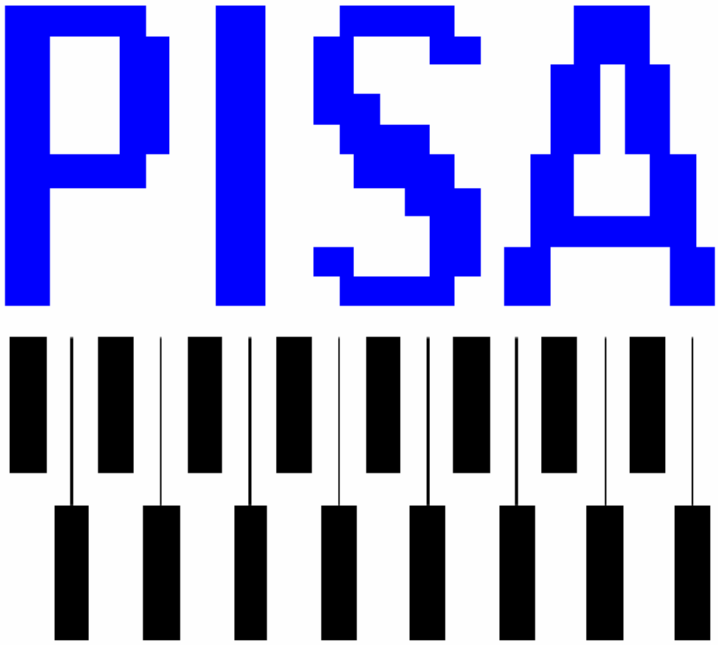
PISA®-Bus



Specification

Document Revision 1.8

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1 User Information

1.1 General Information

This document is based on the former PISA® Specification Rev. 1.7 (released on 04 June 1997). It contains no changes on the electrical and basic mechanical characteristics of the PISA® bus itself. It just adds some additional information and some changes for a better understanding. Some information, especially about companies supporting the PISA®-Bus, has been removed. This has been done because the very old information about the companies was not state of the art.

1.2 Objective

This document is the defining specification for PISA® Single Board Computers. It specifies common mechanical and electrical characteristics for all PISA® SBC designs to ensure physical interchangeability and electrical compatibility between PISA boards and backplanes.

1.3 Target Audience

This guide is intended for hardware engineers who design PISA® single board computers or system baseboards using the PISA®-Bus.

1.4 Assumptions

The reader is assumed to have a hardware engineering background as well as experience with personal computer buses and peripheral interfaces. A working knowledge of practices for designs of multi-layer, printed circuit boards is assumed.

1.5 Scope

This specification should be regarded as a supplement to industry standards that define computer buses and interfaces used on PISA® SBCs. This specification does not include detailed information on protocols, timing, and logic levels. Please refer to the relevant industry standards for this detailed information.

PISA® SBCs typically contain basic signal termination components such as pullup resistors. In some applications it will be necessary to place additional components on the baseboard to meet application-specific ESD, EMI, or safety requirements. These requirements vary among applications and are outside the scope of this document.

1.6 Disclaimer

Although the information presented in this document was carefully reviewed and is believed to be accurate, it is not guaranteed. The reader assumes all liability for the use of the information herein.

1.7 Technical Support

Technicians and engineers from Kontron Embedded Modules and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Before contacting Kontron Embedded Modules technical support, please consult our Web site at http://www.kontron.com/emd for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone.

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2 General Information

2.1 History of PISA BUS and Kontron

January 1996	PISA® Bus has been developed by Giantec Inc. Taiwan in January 1996.
April 1996	Giantec Inc. introduced the Term „PISA® Bus" for their definition.
May 1996	first 486 PISA® compatible product introduced by Giantec Inc.
June 1996	JUMP GmbH is joining Giantec Inc. as the first European Company
Q3/Q4 1996	other Companies join Giantec Inc. to push PISA® as a BUS of the future
January 1997	JUMP GmbH introduced its first Pentium Board using PISA® Bus.
August 1997	JUMP GmbH becomes JUMPtec Industrielle Computertechnik GmbH
July 1998	JUMPtec Industrielle Computertechnik GmbH becomes JUMPtec AG
July 2002	Kontron AG gets the legal successor by the merge with JUMPtec AG

2.2 Supporting Companies and Available Products

The former PISA®-Bus specification rev. 1.7 contained a detailed list of companies, their addresses and their contacts. This part has been removed as well as the list of available products. It is not the task of a specification to give this information and it makes it difficult to keep the specification up to date. Please search the world wide web for companies offering PISA® products.

The main companies which were supporting the PISA®-Bus in 1997 are:

- Atronics International Inc.
- Axiom Technology Inc.
- Boards / Micron AG
- Giantec Inc.
- Jump Industrial Computer GmbH
- Leukhard Systemelektronik GmbH
- Siliconrax Industrial Computer Specialists

2.3 Additional References

This document does not include detailed information on protocols, timing, and logic levels. Please refer to the relevant industry standards for this detailed information. Especially refer to the following industry standard specifications:

- ISA Bus specification P996 rev 1.1
- PCI Bus specification Rev 2.1

The reader can find a list of additional helpful sources, like text books, specifications and forums in the Appendix A: PC Architecture Information.

Note: *Kontron is not allowed to offer or hand out copies of these additional references. Please contact the corresponding owners of the documents and specifications.*

2.4 Advantages of PISA Bus

- half size Boards available for space critical applications including PCI and ISA
- world wide support by many companies
- allows compact backplanes using ISA and PCI, backplanes are about ½ size of PICMG
- allows for 66 MHz PCI Bus because of shorter routing for PCI Bus
- future expansion for 64 Bit PCI Bus possible
- supports 4 external PCI slots
- standard ISA Bus CPU can be used in PISA Slot for upgradeability

3 Pin-Out of PISA Bus

Pin#	ISA, top layer, up row	ISA, bot layer, up row	PCI, top layer, low row	PCI, bot layer, low row
1	/IOCHCHK	GND	I2CLK	I2DAT
2	SD7	RSTDRV	GND	GND
3	SD6	VCC	/INTB	/INTA
4	SD5	IRQ9	/INTD	/INTC
5	SD4	-5V	VCC	VCC
6	SD3	DRQ2		
7	SD2	-12V	VCC	VI/O
8	SD1	/0WS	/PCIRST	PCIVLK2
9	SD0	+12V	/GNT0	GND
10	IOCHRDY	GND	/REQ0	/GNT1
11	AEN	/SMEMW	GND	GND
12	SA19	/SMEMR	PCICLK1	/REQ1
13	SA18	/IOW	GND	AD14
14	SA17	/IOR	AD30	AD29
15	SA16	/DACK3	/REQ2	PCICLK3
16	SA15	DRQ3		
17	SA14	/DACK1	/GNT2	PCICLK4
18	SA13	DRQ1	AD28	AD27
19	SA12	/REFRESH	AD26	AD25
20	SA11	SYSCLK	AD24	/CBE3
21	SA10	IRQ7	AD22	AD23
22	SA9	IRQ6	AD20	AD21
23	SA8	IRQ5	AD18	AD19
24	SA7	IRQ4	PWRGDIN	/REQ3
25	SA6	IRQ3		
26	SA5	/DACK2	GND	/GNT3
27	SA4	T/C	AD16	AD17
28	SA3	BALE	/FRAME	/IRDY
29	SA2	VCC	/CBE2	/DEVSEL
30	SA1	OSC	/TRDY	/LOCK
31	SA0	GND	/STOP	/PERR
32				
33			GND	/SERR
34				AD15
35	/SBHE	/MCS16	/CBE1	AD14
36	LA23	/IOCS16	PAR	AD12
37	LA22	IRQ10	GND	GND
38	LA21	IRQ11		
39	LA20	IRQ12	GND	GND
40	LA19	IRQ15	AD13	AD10
41	LA18	IRQ14	AD11	AD8
42	LA17	/DACK0	AD9	AD7
43	/MEMR	DRQ0	/CBE0	AD5
44	/MEMW	/DACK5	AD6	AD3
45	SD8	DRQ5	AD4	AD1
46	SD9	/DACK6	AD2	AD0
47	SD10	DRQ6		
48	SD11	/DACK7	VCC	VI/O
49	SD12	DRQ7	VCC	VCC
50	SD13	VCC	GND	GND
51	SD14	/MASTER	GND	GND
52	SD15	GND		

3.1 ISA Signals

All required signal pull-ups are integrated. In some applications, it may be desirable to add additional signal-termination components to the baseboard.

NOTE: For further description of ISA signals, refer to the Appendix A: PC Architecture Information.

SD[0..15]

These signals provide data bus bits 0 to 15 for peripheral devices. All 8-bit devices use SD0[0..7] for data transfers. All 16-bit devices use SD[0..15]. To support 8-bit devices, the data on SD[8..15] is gated to SD[0..7] during 8-bit transfers to these devices. All 16-bit CPU cycles automatically convert to two, 8-bit cycles for 8-bit peripherals.

SA[0..19]

Address bits 0 through 15 are used to address I/O devices. Address bits 0 through 19 are used to address memory within the system. These 20 address lines, in addition to LA[17..23], allow access of up to 16MB of memory. SA[0..19] are gated on the ISA bus when BALE is high and latched on to the falling edge of BALE.

/SBHE

Bus High Enable indicates a data transfer on the upper byte of the data bus SD[8..15]. All 16-bit I/O devices use /SBHE to enable data-bus buffers on SD[8..15].

BALE

BALE is an active-high pulse generated at the beginning of a bus cycle initiated by a CPU module. It indicates when the SA[0..19], LA17.23, AEN, and /SBHE signals are valid.

AEN

AEN is an active-high output that indicates a DMA transfer cycle. Only resources with a active /DACK signal should respond to the command lines when AEN is high.

/MEMR

/MEMR instructs memory devices to drive data onto the data bus. /MEMR is active for all memory-read cycles.

/SMEMR

/SMEMR instructs memory devices to drive data onto the data bus. /SMEMR is active for memory-read cycles to addresses below 1MB.

/MEMW

/MEMW instructs memory devices to store the data present on the data bus. /MEMW is active for all memory-write cycles.

/SMEMW

/SMEMW instructs memory devices to store the data present on the data bus. /SMEMW is active for all memory-write cycles to address below 1MB.

/IOR

I/O read instructs an I/O device to drive its data onto the data bus. It may be driven by the CPU or by the DMA controller. /IOR is inactive (high) during refresh cycles.

/IOW

I/O write instructs an I/O device to store the data present on the data bus. It may be driven by the CPU or by the DMA controller. /IOW is inactive (high) during refresh cycles.

/IOCHCHK

/IOCHCHK is an active-low input signal that indicates that an error has occurred on the module bus. If I/O checking is enabled on the CPU module, an /IOCHCHK assertion by a peripheral device sends a NMI to the processor.

IOCHRDY

The I/O Channel Ready is pulled low to extend the read or write cycles of any bus access when required. The CPU, DMA controllers or refresh controller can initiate the cycle. A peripheral that cannot present read data or strobe in write data within this amount of time uses IOCHRDY to extend these cycles. This signal should not be held low for more than 2.5 µs for normal operation. Any extension to more than 2.5 µs does not guarantee proper DRAM memory content because memory refresh is disabled when IOCHRDY is low.

/MCS16

The /MCS16 signal determines when a 16-bit to 8-bit conversion is needed for memory bus cycles. A conversion is done any time the CPU module requests a 16-bit memory cycle while the /MCS16 line is high. If /MCS16 is high, 16-bit CPU cycles are automatically converted on the bus into two 8-bit cycles. If /MCS16 is low, an access to peripherals is done 16-bits wide.

/IOCS16

The /IOCS16 signal determines when a 16-bit to 8-bit conversion is needed for I/O bus cycles. A conversion is done any time the CPU module requests a 16-bit I/O cycle while the /IOCS16 line is high. If /IOCS16 is high, 16-bit CPU cycles are automatically converted on the bus into two 8-bit cycles. If /IOCS16 is low, an access to peripherals is done at 16-bit width.

/REFRESH

/REFRESH is pulled low whenever a refresh cycle is initiated. A refresh cycle is activated every 15.6 us to prevent loss of DRAM data.

/OWS

The Zero wait-state signal tells the CPU to complete the current bus cycle without inserting the default wait states. By default, the CPU inserts 4 wait states for 8-bit transfers and 1 wait state for 16-bit transfers.

/MASTER

This signal is used with a DRQ line to gain control of the system bus.

SYSCLK

SYSCLK is supplied by the CPU module and has a nominal frequency of about 8 MHz with a duty cycle of 40-60 percent. The frequency supplied by different CPU modules may vary.

OSC

The CPU module supplies OSC. It has a nominal frequency of 14.31818 MHz and a duty cycle of 40-60 percent. This signal is supplied at all times except when the CPU module is in sleep mode.

RESETDRV

This active-high output is system reset generated from CPU modules. It is responsible for resetting external devices.

DREQ[0, 1, 2, 3, 5, 6, 7]

The asynchronous DMA request inputs are used by external devices to indicate when they need service from the CPU module's DAM controllers. DREQ0..3 are used for transfers between 8-bit I/O adapters and system memory. DREQ5..7 are used for transfers between 16-bit I/O adapters and system memory. DRQ4 is not available externally. All DRQ pins have pullup resistors on CPU modules.

/DACK[0, 1, 2, 3, 5, 6, 7]

DMA acknowledge 0..3 and 5.7 acknowledge DMA requests. They are active-low.

T/C

The active-high output TC indicates that one of the DMA channels has transferred all data.

IRQ[3..7, 9,15]

These are the asynchronous interrupt request lines. IRQ0, 1, 2 and 8 are not available as external interrupts because they are used internally on the CPU module. All IRQ signals are inactive-high. The interrupt requests are prioritized. IRQ9 through IRQ12 and IRQ14 through IRQ15 have the highest priority (IRQ9 is the highest). IRQ3 through IRQ7 have the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the CPU acknowledges the interrupt request (interrupt-service routine).

3.2 PCI Signals

For compatibility with all PISA® SBCs, external PCI devices should have 3.3V-signal levels and be 5V tolerant. No pull-ups should be implemented externally on the PCI bus.

NOTE: For further description of PCI signals refer to Appendix A: PC Architecture Information.

PCICLK1..4

PCI clock outputs for up to 4 external PCI slots or devices.

/REQ[0..3]

Bus Request signals for up to 4 external bus mastering PCI devices. When asserted, a PCI device is requesting PCI bus ownership from the arbiter.

/GNT[0..3]

Grant signals to PCI Masters. When asserted by the arbiter, the PCI master has been granted ownership of the PCI bus.

AD[0..31]

PCI Address and Data Bus Lines. These lines carry the address and data information for PCI transactions.

/CBE[0..3]

PCI Bus Command and Byte Enables. Bus command and byte enables are multiplexed in these lines for address and data phases, respectively.

PAR

Parity bit for the PCI bus. Generated as even parity across AD[31:0] and /CBE[3:0].

/SERR

System Error. Asserted for hardware-error conditions such as parity errors detected in DRAM.

/PERR

Parity Error. For PCI operation per exception granted by PCI 2.1 Specification.

/LOCK

Lock Resource Signal. This signal indicates that either the PCI master or the bridge intends to run exclusive transfers.

/DEVSEL

Device Select. When the target device has decoded the address as its own cycle, it will assert /DEVSEL.

/TRDY

Target Ready. This signal indicates that the target is ready to complete the current data phase of a transaction.

/IRDY

Initiator Ready. This signal indicates that the initiator is ready to complete the current data phase of a transaction.

/STOP

Stop. This signal indicates that the target is requesting that the master stop the current transaction.

/FRAME

Cycle Frame of PCI Buses. This signal indicates the beginning and duration of a PCI access. The access will be either an output driven by the north bridge on behalf of the CPU, or an input during PCI master access.

/PCIRST

PCI Bus Reset. This output signal resets the entire PCI Bus. This signal is asserted during system reset.

/INTA, /INTB, /INTC, /INTD

PCI interrupts. These interrupts are sharable and are typically wired in rotation to PCI slots or devices. See the ETX Design Guide for details.

IDSEL

This pin is not present on the PISA®-SBCs connector, but it is present on each PCI slot connector or device. IDSEL is an input to the device and is used to set a device's configuration address for PCI configuration cycles. The IDSEL pin of each device is typically connected to one of the AD lines to set a unique configuration address.

3.3 Additional Signals

I2CLK

I2CLK is the I2C-BUS clock for a backplane EEPROM.

I2DAT

I2DAT is the 12C-BUS data for a backplane EEPROM.

PWRGDIN

Powergood input is a low active reset input to the CPU.

NC

The PISA definition includes 3 unconnected Pins for future extension.

3.4 Missing Signals

The PISA® Bus supports all ISA Bus signals and 32Bit PCI signals except the following signals:

- JTAG signals which are only for test purpose
- /SBO and SDONE which are needed for cache on PCI BUS.
- 64 Bit extension signals

3.5 Summary

The PISA®-Bus connector supports a total of 188 pins, 98 are used for ISA Bus signals and 90 for PCI bus signals.

4 Electrical characteristics of PISA Bus

4.1 Power Supply Definition

The PISA®-Bus connector offers the following power pins:

Power	# PISA®-Bus Pins	Max. Current
GND	19	
VCC	9	9 A
+12V	1	1 A
-12V	1	1 A
-5V	1	1 A
V I/O	2	2 A

The PISA Bus power pins are not used to supply power to the I/O Boards. They are just power pins to supply the CPU Board itself. The I/O slots have to be supplied via the backplane.

The PISA CPU Board does generate its own 3.3V and CPU voltages as needed, and therefore needs no 3.3V supply pins.

Whenever a PISA CPU Board offers a separate power connector onboard it is recommended to supply through both, the onboard power connector and the backplane.

4.2 IDSEL mapping

The table below shows the implementation of the necessary IDSEL routings on the CPU board and the backplane.

target device	AD line	Description
0	AD11	PISA CPU chipset internal device
1	AD12	PISA CPU chipset internal device
2	AD13	PISA CPU onboard device # 1
3	AD14	PISA CPU onboard device # 2
4	AD15	PISA CPU onboard device # 3
5	AD16	PISA CPU onboard device # 4
6	AD17	
7	AD18	
8	AD19	PISA Backplane slot # 1
9	AD20	PISA Backplane slot # 2
10	AD21	PISA Backplane slot # 3
11	AD22	PISA Backplane slot # 4
12	AD23	
13	AD24	
14	AD25	
15	AD26	

4.3 Clock distribution

The PISA® CPU supplies all PCI clocks for 4 bus slots over the PISA® connector and all internal Clocks for onboard devices.

The PISA® CPU onboard PCI CLK delay is specified to be 750ps later than the PCI clocks routed to the PISA® connector. The difference is measured from the PISA connector pad to the onboard device input pin.

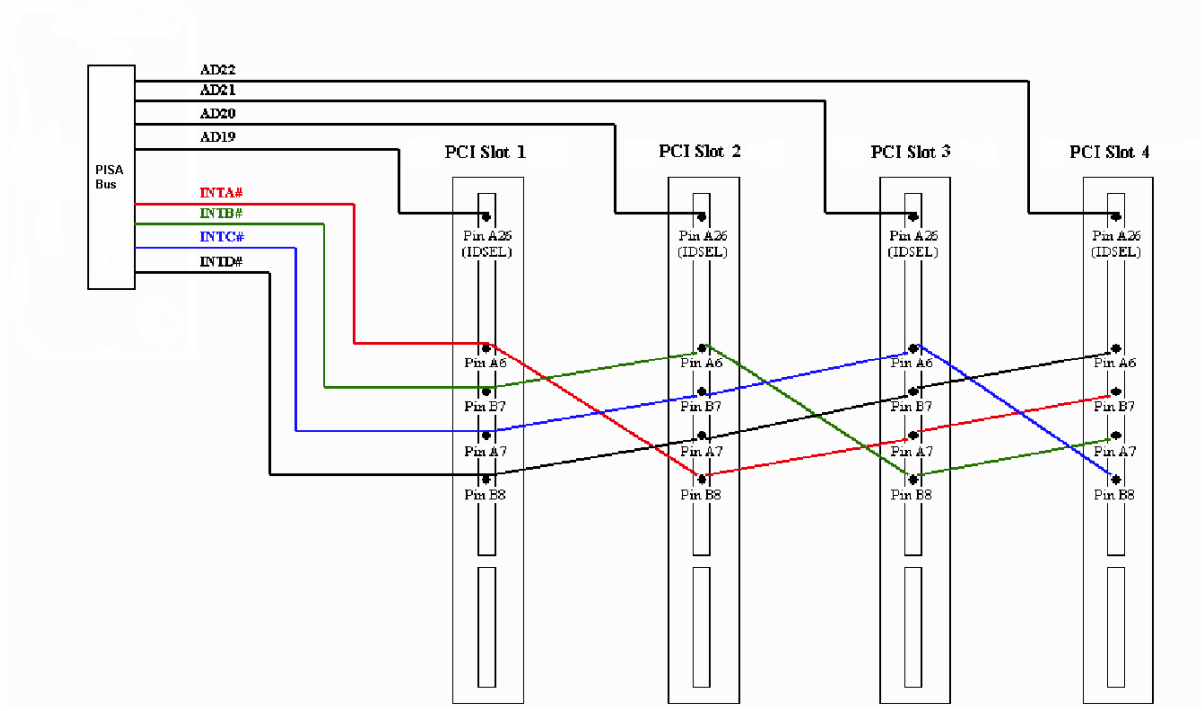
The backplane manufacturer has to route the clocks on the backplane with a delay of 600ps. This has to include the delay of both (the PISA and the PCI) connectors.

4.4 Interrupt-Routing

Following interrupt routing on the backplane is recommended for proper bios support:

Backplane Slot	PISA INT A	PISA INT B	PISA INT C	PISA INT D
Slot 1 (AD19)	INT A	INT B	INT C	INT D
Slot 2 (AD20)	INT D	INT A	INT B	INT C
Slot 3 (AD21)	INT C	INT D	INT A	INT B
Slot 4 (AD22)	INT B	INT C	INT D	INT A

e.g. INT B signal of PCI-Slot 3 (IDSEL AD21) has to be routed to signal INT D of the PISA board

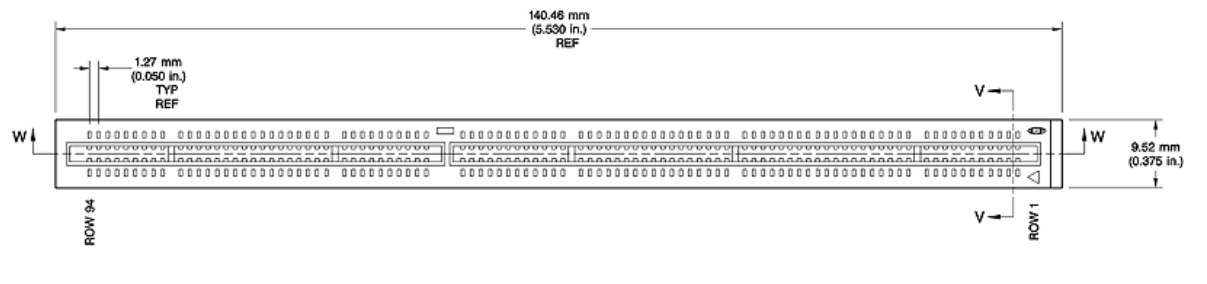


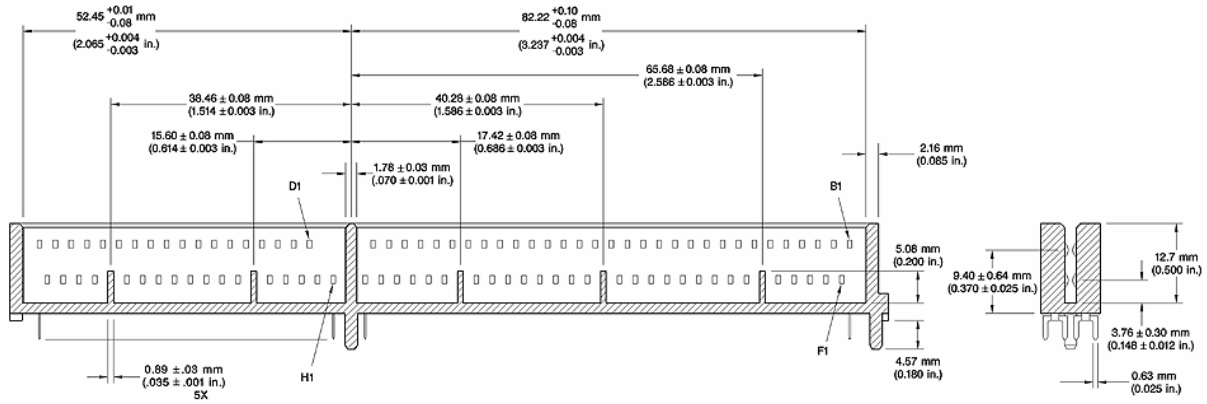
Attension: There are CPU boards and backplanes on the market designed as PCISA. These boards have a different PCI interrupt routing not following the PCI 2.1 recommendations. Check with your supplier, whether the boards you intend to use are PISA compliant or following PCISA standard.

5 Mechanical Specification

5.1 Connector

The PISA®-Bus connector used on backplanes, is the same type used on EISA-systems in former times.





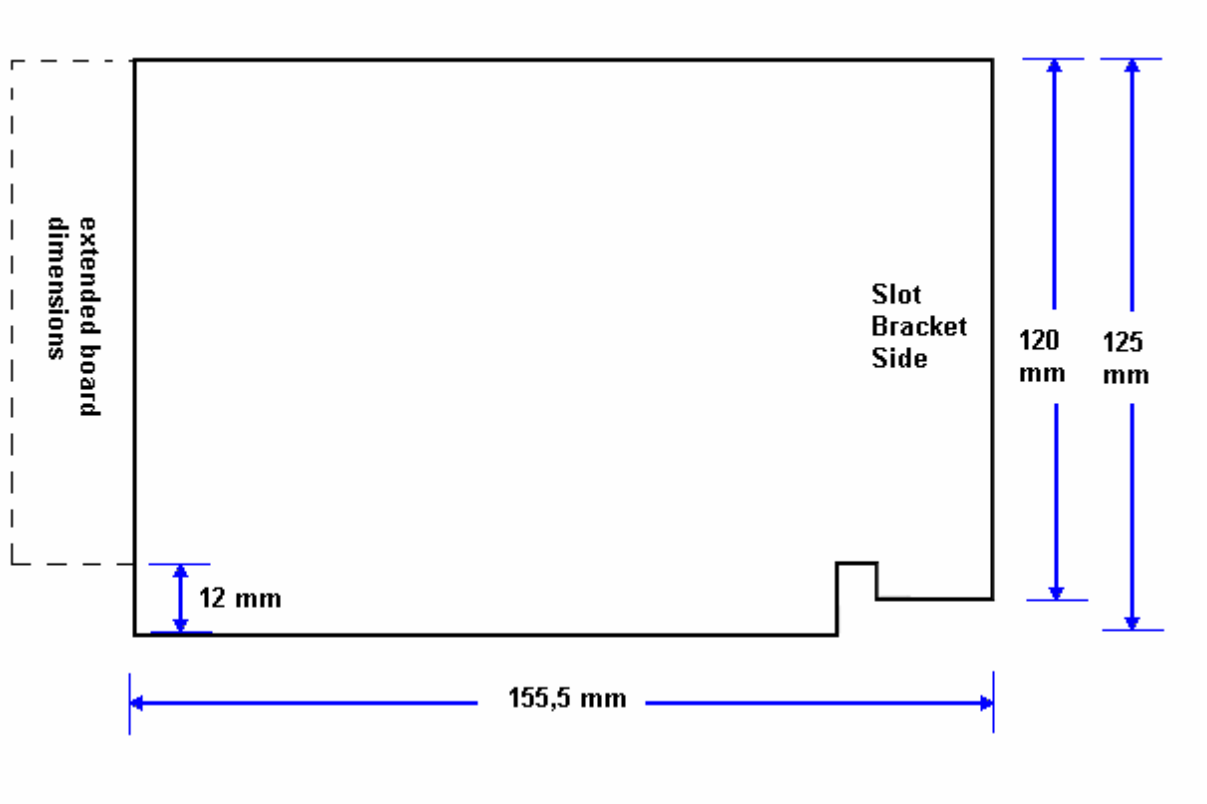
Ordering Information

Supplier	Description	Order Number	Device
BERG	EISA Edge-Card Connector 188 Position with metal holddown	92032-001	JPISACON
FOXCONN	EISA Connector	EI09401-GC	JPISACON

You may use other suppliers instead if their connectors fulfill the same specification as the types above.

5.2 CPU Board Dimensions

The PISA®-Bus CPU Board should be designed to allow as small systems as possible. The Board should either end with the bus connector, or if it is longer, it should not cover the area down to the connector, because this area is reserved for future 64 bit expansion.



6 Appendix A: PC Architecture Information

The following sources of information can help you better understand PC architecture.

6.1 General PC Architecture

- *Embedded PCs*, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- *Hardware Bible*, Winn L. Rosch, SAMS, 1997, ISBN 0-672-30954-8
- *Interfacing to the IBM Personal Computer*, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- *The Indispensable PC Hardware Book*, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- *The PC Handbook: For Engineers, Programmers, and Other Serious PC Users*, Sixth Edition, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

6.1.1 ISA, Standard PS/2 – Connectors

- *AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design*, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- *AT IBM Technical Reference Vol 1&2*, 1985
- *ISA & EISA Theory and Operation*, Edward Solari, Annabooks, 1992, ISBN 0929392159
- *ISA Bus Specifications and Application Notes*, Jan. 30, 1990, Intel
- *ISA System Architecture*, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- *Personal Computer Bus Standard P996*, Draft D2.00, Jan. 18, 1990, IEEE Inc
- *Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus*, Compaq 1989

6.1.2 PCI

- The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- *PCI & PCI-X Hardware and Software Architecture & Design*, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- *PCI System Architecture*, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

6.1.3 Programming

- *C Programmer's Guide to Serial Communications*, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- *Programmer's Guide to the EGA, VGA, and Super VGA Cards*, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4
- *The Programmer's PC Sourcebook*, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- *Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas*, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

7 Revision History

Date	Document Name	Subjects added, changed, deleted	Changed by
04.06.1997	PISAD217.DOC	First public version	WK
30.07.2007	PISAD218.DOC	Updated to new Kontron style, added additional information for better understanding	BHO