ePCI-X, a PCI-Only Evolution for PCI/ISA Systems

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Abstract

Most new designs based on the popular PCI/ISA form factor have no requirements for the ISA bus. They demand more I/O bandwidth, especially in the form of the PCI-X extension to the PCI specification.

Also, recent chipsets have no support for an ISA bus and can even be hostile to the addition of a PCI-to-ISA bridge. The ISA bus is now a cumbersome, expensive, and often useless feature that imposes restrictions on chipset choice.

Those were the motivations of the PICMG 1.2 subcommittee that developed the Embedded PCI-X, or ePCI-X specification. This PCI-only specification was approved in January 2002 by PICMG executives. It defines a single board computer and backplane system with one or two PCI or PCI-X busses.

Two board sizes are defined. A half-size single-bus board, similar to half-size ISA SBCs, targets applications where space is a concern. The full-size single or dual-bus board is intended for more I/O intensive applications.

Hence a very broad range of applications are covered, from the plain vanilla 32-bit 33MHz PCI single-bus computers, or up to 16x more I/O bandwidth with the full-fledge dual PCI-X busses at 133MHz.

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The Goals

The following are the initial goals for the ePCI-X specification. All of them were met.

- Define a low cost PCI-only passive backplane solution
- Give half-size SBCs access to PCI/PCI-X expansion cards
- Keep mechanical compatibility with current ISA chassis
- Fully comply with PCI Local Bus Specification R2.2 and PCI-X Addendum R1.0
- Standardize the SBC component side to comply with the PCI specification
- Provide an optional second PCI/PCI-X bus to double the I/O bandwidth and make possible fully passive backplanes with up to eight expansion slots
- Use low cost, multi-source connectors for the SBC
- Provide keying to avoid putting a PCI card in the SBC slot or vice versa
- Maintain a high degree of interoperability between SBCs and backplanes
- Enable 64-bit peer-to-peer transfers between 64-bit PCI expansion cards even when the SBC is limited to 32-bit
- Add optional power management and SMBus capabilities
- Provide enough reserved pins for future extensions

The Market

Most member companies of the PICMG 1.2 subcommittee offer both PCI/ISA and CompactPCI solutions. It was not the subcommittee's intention to write a specification that would compete with CompactPCI. Instead, ePCI-X aims at applications where CompactPCI specific features are not required (Figure 1). The main targets are low cost solutions through compatibility with off-the-shelf PCI cards.

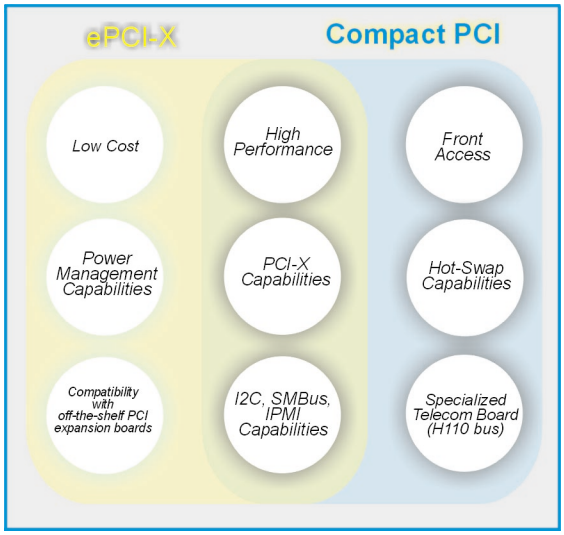

Figure 1: ePCI-X and CompactPCI

The SHB Connector

A dual-bus System Host Board (thereafter SHB) drives two 64-bit PCI/PCI-X busses using three common 32-bit type PCI connectors. This gives almost the same number of pins as two 64-bit PCI connectors would have, but it can be split at 2/3 of its length. This way, single-bus SHBs use only P1 and P2 (Figure 2) while dual-bus SHBs use all three connectors (Figure 3). Single bus SHBs still have enough pins to support all extra features like ATX control, power management, etc. These connectors also enable a complete mechanical keying mechanism on the SHB slot.

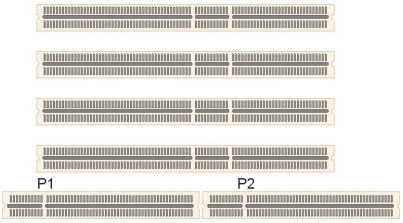

Figure 2: Single-Bus Backplane Example

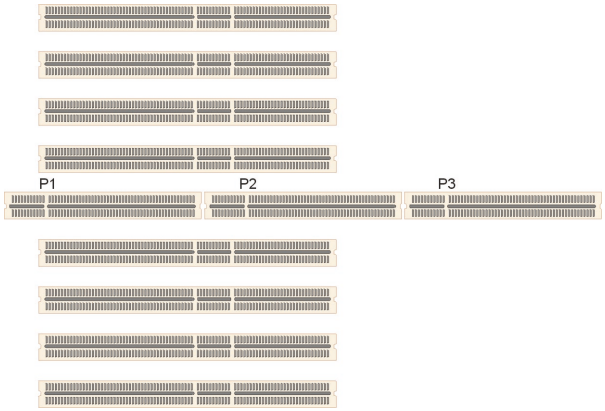

Figure 2: Dual-Bus Backplane Example

Signaling Voltage

Until recently, almost all PCI expansion cards were either 5V or universal (3.3V signaling and 5V tolerant). Today, motherboards with 3.3V PCI slots are more common as well as 3.3V-only PCI cards. But if you have an ePCI-X backplane with 3.3V slots, how do you make sure that your SHB will not drive at 5V or, if the backplane has 5V slots, that the SHB can tolerate 5V signaling?

The ePCI-X specification solves that problem by defining an electrical keying for each bus. The SHB will stay in reset and keep all PCI cards in reset (i.e. 3-state) if it is not compatible with the backplane's I/O voltage, as independently stated by each bus Vio pin. Chipsets that use 3.3V signaling but are 5V-tolerant are common. An SHB based on such a chipset will work in any backplane.

Dual-Bus, Single-Bus and No-Bus

Two signals are used by an ePCI-X backplane to tell the SHB which busses are present. The SHB can use this information to disable any unused hardware.

A dual-bus SHB will work in a single-bus backplane. The single-bus backplane can optionally provide a power-only P3 connector if space/cost constraints permit it.

It is also acceptable to have a backplane without PCI busses. Such a backplane provides power to one or more SHB, and optional ATX power supply control, as well as SMBus capabilities for system monitoring.

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32-bit and 64-bit

Some applications will do 64-bit peer-to-peer transfers between PCI expansion cards but use the SHB for initialization, bus arbitration and user interface. A low cost 32-bit SHB may be enough for such a task.

This is why a SHB with only a 32-bit PCI bus still has all 64-bit pull-up resistors. It will also assert REQ64# during reset for proper initialization of 64-bit PCI cards.

As required by the PCI specification, on a 32-bit backplane, REQ64# is not bussed on PCI expansion slots. This makes possible all 32/64-bit combinations of SHB and backplane.

PCI-X Support

The PCI-X extension to the PCI specification is beginning to gain industry acceptance. Chipsets, peripheral functions and IPs for ASICs and FPGAs are already available. Being able to achieve 1GBps peak bandwidth with 133MHz PCI-X is appealing for high-bandwidth PCI cards and for large backplanes that aggregate many low-bandwidth PCI cards via PCI-X-to-PCI bridges.

At 66MHz, PCI-X is also interesting since four slots can be achieved at twice the peak bandwidth of 33MHz PCI.

One of the difficulties of PCI-X is the clock skew requirement. Traditional 33MHz PCI requests a maximum clock skew of 2ns. With PCI-X, the skew window is now only 500ps. Backplane variations in trace lengths and trace velocity make this almost impossible to achieve with the current PCI/ISA solution since backplane clock trace lengths change from vendor to vendor.

The ePCI-X way of achieving minimal clock skew is to use a feedback trace from the backplane. The SHB can phase lock its PCI clocks with the backplane feedback. This is a common practice on motherboards and on designs with PCI-to-PCI bridges and its a low cost way of achieving very low skew while giving the backplane designer a lot of freedom.

PCI cards capabilities are detected using M66EN and PCIXCAP in the same way it's done on a motherboard implementation. The backplane itself is a virtual fifth slot that can restrict bus mode and speed by grounding M66EN and/or PCIXCAP or having a 10K pull-down resistor on PCIXCAP. Table 1 shows how the SHB senses PCI-X capabilities on a given bus.

PCIXCAP	PCI-X Capabilities
GND	Not capable, standard PCI
2K to 10K pull-down (1 to 5 10K pull-down in parallel)	50/66MHz PCI-X
Open	100/133MHz PCI-X

In a dual-bus system, bus mode and speed of the two busses are independent.

Table 1: PCIXCAP Usage

Power Management and SMBus Options

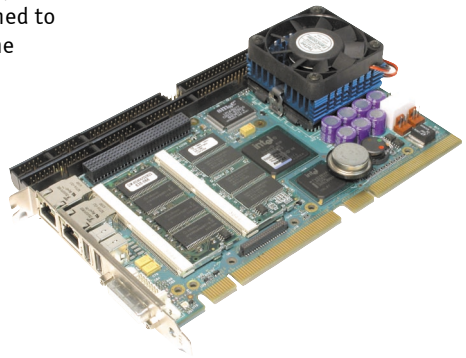
In the PCI/ISA world, ATX power supplies are often used and a special, vendor dependent, cable is required to bring the ATX control signals to the SBC. Those signals are included in the ePCI-X SHB edge connector as well as a provision for the PCI 3.3VAUX auxiliary supply for D3COLD power state. Power management events from PCI expansion cards (PME#) is also provided.

Also, according to the latest ECN from the PCI-SIG, there is now an optional SMBus link on PCI expansion cards. The ePCI-X SHB is also attached to this link.

All those features are optional to avoid increasing the cost of the SHB when they're not required.

Kontron's ePCI-100 Half-Size ePCI-X SHB

Kontron's Pentium III based SHB has two 100Base-TX links, a DVI video output, CompactFlash and a 5V PC/104-Plus (PCI-only) mezzanine support. The PCI bus is 32-bit 33MHz but, as required by ePCI-X, it is 64-bit friendly. This 32-bit SHB can be used in a 32-bit or 64-bit backplane. It will work in a 5V backplane and also in a 3.3V backplane unless it hosts a 5V PC/104-Plus mezzanine. Smart I/O keying is performed to prevent incompatible combinations of backplane and mezzanine from damaging any 3.3V-only backplane PCI cards. It will work in a no-bus backplane or without any backplane when a power cable is used.



Kontron's ePCI-100

Conclusion

The ePCI-X specification comes at the right time and answers a real market need. The specification is very flexible and applicable to small low-power single board computers as well as larger I/O intensive server boards.

The specification offers elegant solutions to I/O voltage keying, PCI-X clock skew and 32/64-bit interoperability issues.

As an upgrade path from ISA, ePCI-X preserves chassis investment while providing more I/O bandwidth.

When comparing a PCI/ISA SBC and an ePCI-X SHB with similar features, the ePCI-X solution is expected to be more cost effective because of the absence of the extra ISA hardware and related engineering development and validation.

Finally, many applications will benefit from a dual-bus, fully passive backplane.

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