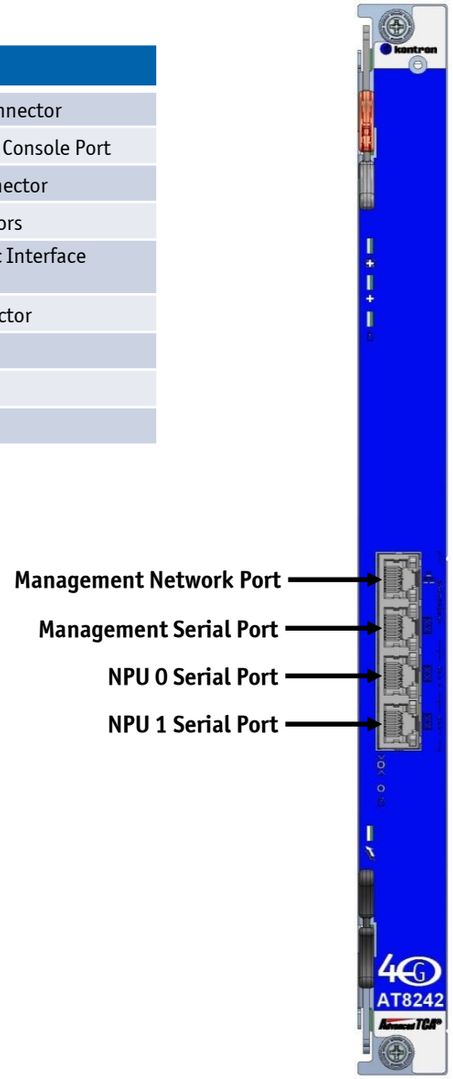
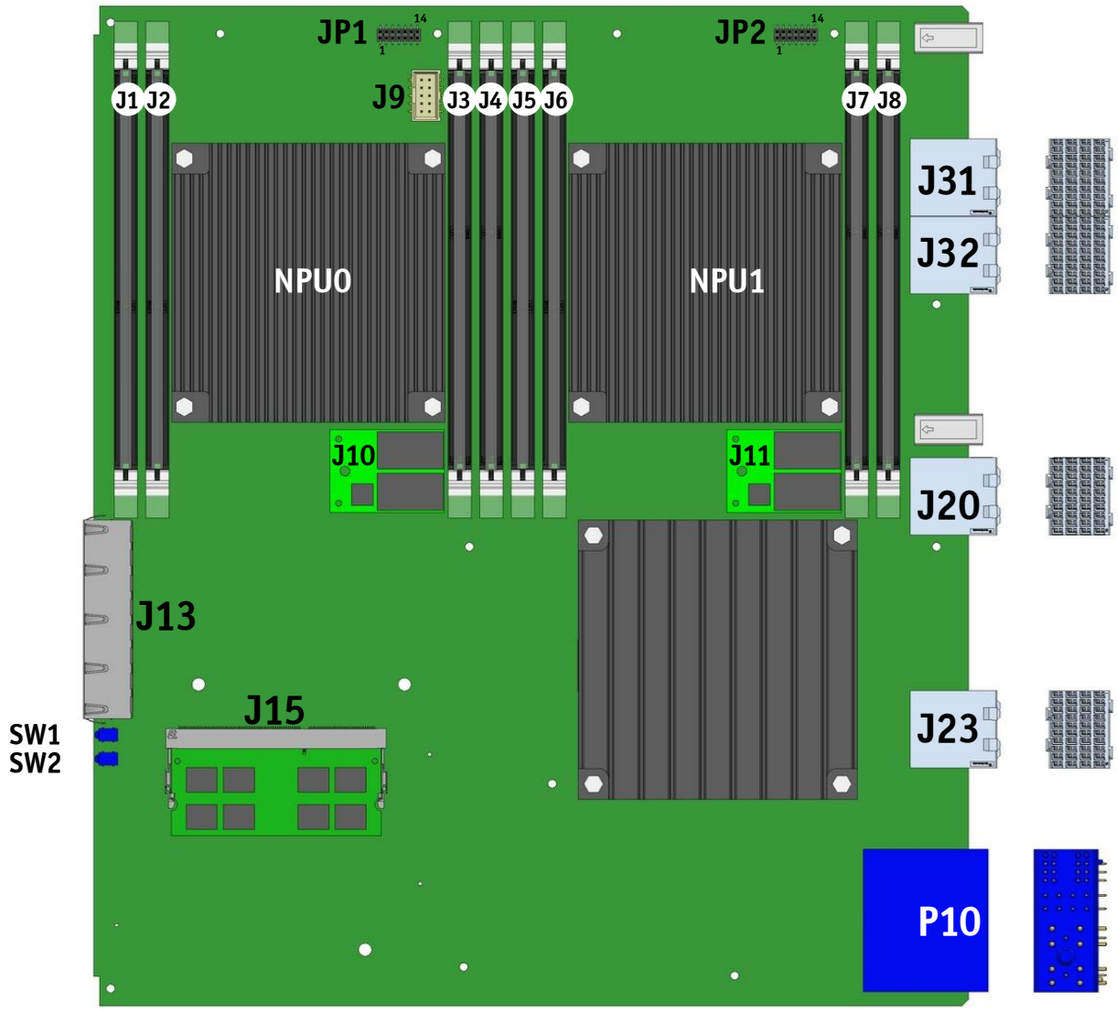
>> AT8242 Quick Reference Sheet <<

Connectors

J1	Memory Socket NPU0 Channel 1	J10 & J11	Usb Flash Connector
J2	Memory Socket NPU0 Channel 3	J13	Management Console Port
J3	Memory Socket NPU0 Channel 2	J15	Memory Connector
J4	Memory Socket NPU0 Channel 0	J31 & J32	RTM Connectors
J5	Memory Socket NPU1 Channel 1	J20 & J23	Base & Fabric Interface Connector
J6	Memory Socket NPU1 Channel 3	P10	Power Connector
J7	Memory Socket NPU1 Channel 2	SW1	Reset Switch
J8	Memory Socket NPU1 Channel 0	SW2	User Switch
J9	NPU Debug Connector		





Symbols Chart

	Hot Swap		Reset Button
	Out of Service		Serial Port
	Healthy		User

LEDs Signification available on back.

LEDs Signification

Hot Swap (Blue)		
Solid On	100% on	FRU Inactive
Long Blink	90% on	FRU Activation Request
Solid Off	0% on	FRU Activation In Progress / FRU Active
Short Blink	10% on	FRU Deactivation Request / FRU Deactivation In Progress

Out of Service (Red / Amber) [Default: Red]	
Solid On	IPMC in reset or starting up
Application Defined	May be controlled by application using PICMG API

Health (Amber / Green) [Default: Green]	
Off	Payload power down
Green	Health Ok
Amber	Health Error (Critical)
Application Defined	May be controlled by application using PICMG API

Jumper Settings (* indicates jumper default position)

JP1 (1-2) FPGA PROM Selection		JP2 (1-2) Watchdog Disable	
IN:	Factory PROM (fail-safe)	IN:	Watchdog Disable
*OUT:	Normal (auto)	*OUT:	Watchdog Enable
JP1 (3-4) IPMC Reserved 0		**JP2 (3-4) Shelf Manager Override**	
IN:	Reserved	IN:	Override
*OUT:	Normal Operation	*OUT:	Normal Operation
JP1 (5-6) IPMC Reserved 1		**JP2 (5-6) IPMC Override**	
IN:	Reserved	IN:	Override (FPGA turn-On Blade)
*OUT:	Normal Operation	*OUT:	Normal Operation
JP1 (7-8) FPGA Reserved #0		**JP2 (7-8) RTM Override**	
IN:	Reserved	IN:	Override (Turn-On AMCs)
*OUT:	Normal Operation	*OUT:	Normal Operation
JP1 (9-10) FPGA Reserved #1		**JP2 (9-10) Reserved for HW Test**	
IN:	Reserved	IN:	Reserved
*OUT:	Normal Operation	*OUT:	Normal Operation
JP1 (11-12) FPGA Reserved #2		**JP2 (11-12) Console Selection bit 1**	
IN:	Reserved	IN:	Selection bit 1
*OUT:	Normal Operation	*OUT:	Normal Operation
JP1 (13-14) Factory Mode		**JP2 (13-14) Console Selection bit 0**	
IN:	Factory Mode	IN:	Selection bit 0
*OUT:	Normal Operation	*OUT:	Normal Operation

J9 NPU Debug Connector

1	NPU0_DEBUG_RTS#	6	NPU1_DEBUG_RTS#
2	NPU0_DEBUG_TX	7	NPU1_DEBUG_TX
3	NPU0_DEBUG_RX	8	NPU1_DEBUG_RX
4	NPU0_DEBUG_CTS#	9	NPU1_DEBUG_CTS#
5	GND	10	GND

J10 & J11 USB Flash Connector

1	VCC	6	N.C.
2	N.C.	7	GND
3	USB_DATA-	8	N.C.
4	N.C.	9	N.C. (KEY)
5	USB_DATA+	10	N.C.

J13 Management Console Port

1	RTS	6	GND
2	DTR	7	RX#
3	TX#	8	DSR
4	GND	9	CTS

J13 Network Management Port

1	TRD0+	6	TRD2-
2	TRD0-	7	TRD1-
3	TRD1+	8	TRD3+
4	TRD2+	9	TRD3-

Support / Download

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The Quick Reference Sheet can be downloaded from the Kontron web site at:
http://www.kontron.com
or from Kontron FTP site at:
ftp://ftp.kontron.ca/Support