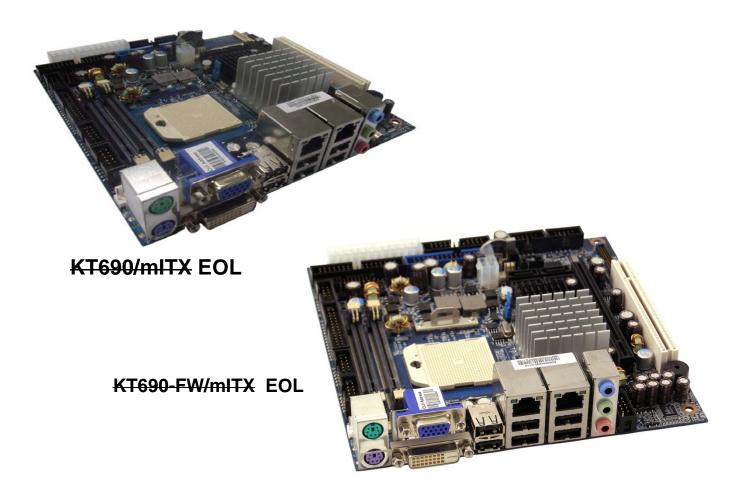


User Manual

for the Motherboards:







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Document revision history.

Revision	Date	Ву	Comment	
J	Jun. 1 st 2012	MLA	EOL products indicated. (Improved description of supported TV-out connector, even though EOL).	
I	Aug. 29 th 2011	MLA	Removed BIOS option "Replace GFX subid". Info "HyperMemory" removed. Added passive cooler.	
Н	Mar. 23 rd 2011	MLA	Added info on System Overview. Added support of Windows 7.	
G	Jan. 19 th 2011	MLA	New BIOS option "Replace GFX subid". Added note on XP Video Driver (OS setup). Added Power consumption for BGA versions.	
F	Sep. 9 th 2010	MLA	Added KT690/mITX BGA. Minor corrections.	
E	Apr. 22 nd 2010	MLA	Feature connector corrections and added note on pin 3 and 4. Added "mounting the board to chassis". Memory size has been corrected. Added warning to Installation Guide (turn off PSU).	
D	May. 14 th 2009	MLA	Correction to LAN connector pinning. Battery alternative added. Added BIOS setting: Default init boot order. Correted Force Boot Devices. Corrected Video Display Devices.	
С	Sep. 16 th 2008	MLA	Added FDD cable info. Corrections to Floppy connector. CPU List updated. Added Clock Distribution.	
В	Aug. 11 th 2008	MLA	Battery lifetime info added. Minor corrections, additions and layout improvements.	
Α	Jul. 23 rd , 2008	PJA	Updated	
0	Dec. 11 th , 2007	PJA	First preliminary manual version.	

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 - 1. Type.
 - 2. Part-number.
 - 3. Serial Number.
- Configuration
 - 1. CPU Type, Clock speed.
 - 2. DRAM Type and Size.
 - 3. BIOS Revision (Find the Version Info in the BIOS Setup).
 - 4. BIOS Settings different than Default Settings (Refer to the BIOS Setup Section).
- System
 - 1. O/S Make and Version.
 - 2. Driver Version numbers (Graphics, Network, and Audio).
 - 3. Attached Hardware: Harddisks, CD-rom, LCD Panels etc.

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1. Introduction

This manual describes the KT690/mITX, KT690/mITX-FW and KT690/mITX (BGA) boards made by KONTRON Technology A/S. The boards will also be denoted KT690 family if no differentiation is required.

The KT690/mITX, KT690/mITX-FW are to be used with the Mobile AMD Sempron[™] and AMD Turion[™] 64 X2 Mobile Processors for S1 socket and the KT690/mITX (BGA) is available in two versions with premounted BGA processor: Single Core 210U and Dual Core L325.

Use of this manual implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the KT690 Board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in chapter 3 before switchingon the power.



2. Installation procedure

2.1 Installing the board

To get the board running, follow these steps. In some cases the board shipped from KONTRON has premounted CPU (incl. KT690/mITX (BGA)), cooler and DDR2 DRAM. In this case step 1-3 can be skipped.



Warnings: Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected while configuring the board. Otherwise components (RAM, LAN cards etc.) might get damaged.

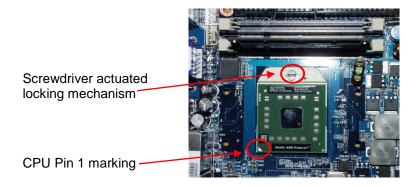
Do not use PSU without 3.3V monitoring watchdog (standard feature in ATX PSU).

Running the board without 3.3V connected will damage the board after a few minutes.

Be careful not to short circuit the lithium battery for instance by placing the board upside down directly on a metal plate etc. (battery 3V connected to ground via IO Connector housing).

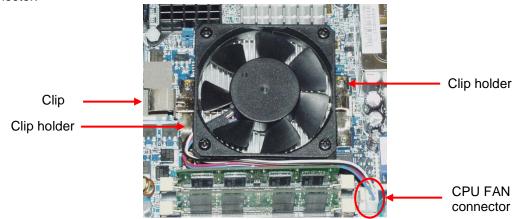
1. Install the processor (KT690/mITX and KT690/mITX-FW only)

The CPU is keyed and will only mount in the CPU socket in one way. Use a 6mm flatheaded screwdriver to open/ close the CPU socket. The Mobile AMD Sempron[™] and AMD Turion[™] 64 X2 Mobile Processors for S1 socket are supported, refer to supported processor overview for details.



2. Cooler Installation (KT690/mITX and KT690/mITX-FW only)

Mount the cooler using the clip holders mounted on the board. Connect the Fan electrically to the CPU FAN connector.



3. Insert the DDR2 SODIMM 200pin DRAM module(s)

Push down the module from the top side until the tabs lock. For a list of approved DDR2 SODIMM modules contact your Distributor or FAE.

DDR2 SODIMM 200pin DRAM modules (PC3200, PC4200, PC5300) are supported.

(continues)



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4. Connecting Interfaces

Insert all external cables for hard disk, keyboard etc. A CRT monitor must be connected in order to change CMOS settings to flat panel support.

5. Connect Power supply

Connect power supply to the board by the ATX/BTXPWR and 4-pin ATX connectors. For board to operate connection of both the ATX/BTX and 4-pin ATX (12V) connectors are required.

6. Turn on the power on the ATX/ BTX power supply

7. Power Button

The PWRBTN_IN must be toggled to start the Power supply; this is done by shorting pins 16 (PWRBTN_IN) and pin 18 (GND) on the FRONTPNL connector (see Connector description). A "normally open" switch can be connected via the FRONTPNL connector.

8. BIOS Setup

Enter the BIOS setup by pressing the key during boot up. Refer to the "BIOS Configuration / Setup" section of this manual for details on BIOS setup.

Enter Advanced Menu / CPU Configuration / Intel SpeedStep Tech. and set this option to "Maximum Performance".

Note: To clear all CMOS settings, including Password protection, move the Clr-CMOS jumper (with or without power) for approximately 1 minute. Alternatively turn off power and remove the battery for 1 minute, but be careful to orientate the battery correctly when reinserted.

9. Mounting the board to chassis



Warning: When mounting the board to chassis etc. please notice that the board contains components on both sides of the PCB which can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the Motherboard on a chassis it is recommended using screws with integrated washer and having diameter of ~7mm.

Note: Don't use washers with teeth, as they can damage the PCB mounting hole resulting in short circuit.



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2.2 Requirement according to EN60950

Users of KT690 boards should take care when designing chassis interface connectors in order to fulfill the EN60950 standard:

When an interface/connector has a VCC (or other power) pin, which is directly connected to a power plane like the VCC plane:

To protect the external power lines of peripheral devices the customer has to take care about:

- That the wires have the right diameter to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

Lithium Battery precautions:

CAUTION!

Danger of explosion if battery is incorrectly replaced.

Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ADVARSEL!

Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri

af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

VORSICHT!

Explosionsgefahr bei unsachgemäßem Austausch der Batterie.

Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

ADVARSEL

Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.

VARNING

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu.

Vaihda paristo ainoastaan laltevalmistajan suosittelemaan

tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.



3. System specification

3.1 Component main data

The table below summarises the features of the KT690/mITX, KT690/mITX-FW and KT690/mITX (BGA) embedded motherboards.

Form factor	KT690/mITX, KT690/mITX-FW and KT690/mITX (BGA): mini ITX (170.18 x 170.18mm)
Processor	 Support for Mobile AMD Sempron[™], AMD Turion[™] 64 and AMD Turion[™] 64 X2 Mobile Processors for S1 socket. (KT690/mITX and KT690/mITX-FW only). 35W maximum TDP 6.4GB/s HyperTransport[™] link, 800 MHz, 16bit/16bit Hypertransport[™] 1.0 Tunnel (I/O Bus) speed of 800MHz Internal L1 cache of 128KB (Single core CPUs) / 128KB x2 (Dual core CPUs) Internal L2 cache of 128/256/512KB (Single core CPUs) / 512KB x2 (Dual core CPUs) Processor technology of 65nm / 90nm Support for AMD Sempron[™] BGA Single Core 210U (KT690/mITX (BGA) only). 15W maximum TDP Up to 6.4GB/s peak HyperTransport[™] link, 800 MHz, 16bit/16bit Internal L1 data cache 64KB + L1 instruktion cache 64KB Processor technology of 65nm Support for AMD Athlon[™] Neo X2 BGA Dual Core L325 KT690/mITX (BGA) only. 18W maximum TDP Up to 6.4GB/s peak HyperTransport[™] link, 800 MHz, 16bit/16bit Internal L1 data cache 2x 64KB + L1 instruktion cache 2x 64KB Internal L2 cache of 2x 512KB Processor technology of 65nm DDR2 memory controller and bus interface
Memory	 Dual Channel DDR2 memory architecture 2 pcs DDR2 SODIMM 200pin DRAM sockets onboard. Support DDR 400/533/667MHz unbuffered memory (PC2-3200/PC2-4200/PC2-5300) Support system memory from 1x 256MB and up to 2 x16GB (PT only up to 2x4GB has been verified). ECC not supported
Chipset	AMD Chipset consisting of: • AMD M690T northbridge (graphics tunnel) • ATI SB600 southbridge (I/O hub)
Video	 Integrated ATI Radeon™ X1200 graphics core CRT Out connector DVI-D connector (Digital only) Onboard LVDS connector TV-Out connector (only configuration "KT690/mITX w TV out") TV-Out pin connector (only configuration "KT690/mITX-FW w TV-out") Dual independent pipe support: Mirror and Dual Independent displays supported. Full DirectX® 9.0 support Maximum resolution of 2048x1536 @ 32bpp for a maximum pixel clock speed of 400MHz. LVDS interface supports dual channel, 24bit OpenLDI/ SPWG panels.

(continues)



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A I' -	A P. 74 CLTOOL COLUMN BUTCHES BUTCHES A P. O. L. C. H. D. H. LANDOOC
Audio	 Audio, 7.1 and 7.2 Channel High Definition Audio Codec using the Realtek ALC888 codec Line-out and Line-in Surround output: SIDE, LFE, CEN, BACK and FRONT Microphone: MIC1, MIC2 CDROM in SPDIF Interface Onboard speaker
I/O Control	Winbond W83627DHG LPC Bus I/O Controller
Peripheral interfaces	 Six USB 2.0 ports on I/O area Four USB 2.0 ports on internal pinrows Two Serial ports (RS232) One Parallel port, SPP/EPP/ECP One Floppy port Four Serial ATA-300 IDE AHCI interfaces One PATA 66/100/133 interface with support for 2 devices CF (Compact Flash) interface (KT690/mITX only) supporting CF type I and II. (UDMA2 max.). Note that only one PATA device is supported when CF is used and only by use of 40-wire cable (not 80-wire cable). Optionally use SATA devices. Two IEEE 1394-1995/ 1394a-2000 OHCI Firewire ports supporting speeds of 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s (KT690/mITX-FW only) PS/2 keyboard and mouse ports
LAN Support	2x 10/100/1000Mbits/s LAN using Realtek RTL8111B PCIe controllers on KT690/mITX and KT690/mITX-FW Intel® Hartwell 82574L PCIe controllers on KT690/mITX (BGA) RPL/PXE netboot supported. Wake On LAN (WOL) supported
BIOS	 Kontron Technology / AMI BIOS (core version 8.00) Support for Advanced Configuration and Power Interface (ACPI 1.0b), Plug and Play Suspend To Ram (S3) Suspend To Disk (S4) Support for Cool'n'Quiet™ Secure CMOS/ OEM Defaults, "Always On" power setting, Forced Boot device. Desktop Management Interface (DMI) Support for addition of System Locked Preinstallation (SLP) key in BIOS RAID Support (RAID modes 0, 1, and 10) (for Linux O/S limitations may apply) TPM onboard
Expansion Capabilities	 PCI Bus routed to PCI slot(s) (PCI Local Bus Specification Revision 2.3) KT690/mITX: 1 slot PCI 2.3, 32 bits, 33 MHz, 5V compliant PCI-Express bus routed to PCI Express slot(s) (PCI Express 1.1a) KT690/mITX: 1 slot PCI-Express x16 with PCI-Express x8 support Mini PCI-Express routed to mini PCI-Express connector Support for Mini PCI-Express modules with no components on backside. SMBus routed to FEATURE, PCI slot, PCI Express and mini-PCI Express connectors LPC Bus routed to TPM connector DDC Bus routed to LVDS and CRT connector 8 x GPIOs (General Purpose I/Os) routed to FEATURE connector
Hardware Monitor Subsystem	 Smart Fan control system, support Thermal® and Speed® cruise for three onboard Fan control connectors: FAN_CPU, FAN_SYS and FEATURE Three thermal inputs: CPU die temperature, System temperature and External temperature input routed to FEATURE connector. (Precision +/- 3°C) Voltage monitoring Intrusion detect input SMI violations (BIOS) on HW monitor not supported. Supported by API.

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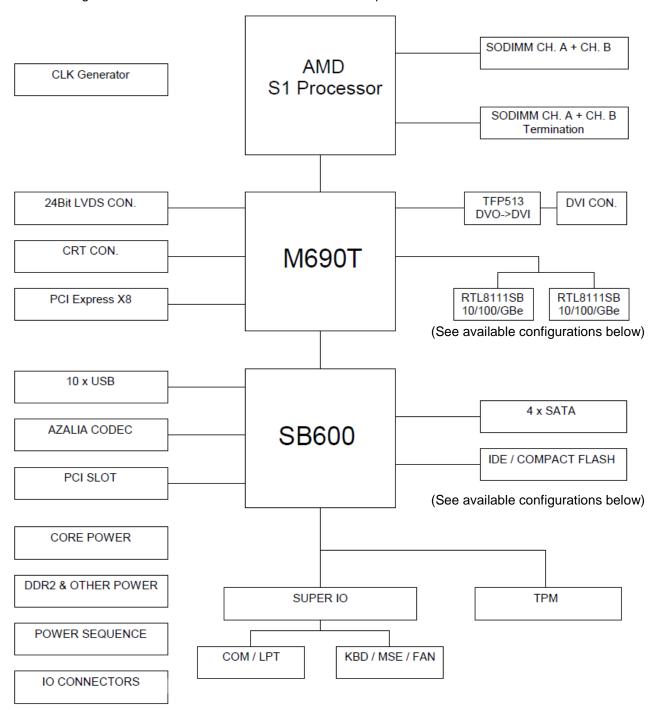


KTD-00738-J **Public User Manual** Date 2012-06-01 Page 13 Operating Win7 **Systems** WinXP Support Windows Vista Windows 2003 WinXP Embedded Linux: Feodora Core 8 **Environmental** Operating: **Conditions** 0°C – 60°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. 10% - 90% relative humidity (non-condensing) Storage: -20°C - 70°C 5% - 95% relative humidity (non-condensing) Electro Static Discharge (ESD) / Radiated Emissions (EMI): All Peripheral interfaces intended for connection to external equipment are ESD/EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard. Safety: UL 60950-1:2003, First Edition CSA C22.2 No. 60950-1-03 1st Ed. April 1, 2003 Product Category: Information Technology Equipment Including Electrical Business Product Category CCN: NWGQ2, NWGQ8 File number: E194252 **Theoretical MTBF:** 234,251 hours or 26.7 years @ 40°C ambient air temperature 135,169 hours or 15.4 years @ 60 °C ambient air temperature Restriction of Hazardeous Substances (RoHS): All boards in the KT690 family are RoHS compliant. Capacitor utilization: No Tantal capacitors on board Only Japanese brand Aluminium and solid electrolytic capacitors rated for 100°C used on board **Battery** Exchangeable 3.0V Lithium battery for onboard Real Time Clock and CMOS RAM. Manufacturer Panasonic / Part-number CR2032NL/LE, CR-2032L/BE or CR-2032L/BN Expected minimum 5 years retention varies depending on temperature, actual application on/off rate and variation within chipset and other components. Approximately current draw is 3µA (no PSU connected). CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.



3.2 KT690 System overview

The block diagram below shows the architecture and main components of the KT690 boards.



Available configurations are:

KT690 configuration	CF socket	IEEE- 1394	TV- Out	LAN	CPU	Cooler
KT690/mITX EOL	+	-	-	Realtek RTL8111B	-	-
KT690/mITX w TV-out EOL	+	-	+	Realtek RTL8111B	-	-
KT690/mITX-FW w TV-out EOL	-	x 2	+ (*)	Realtek RTL8111B	-	-
KT690/mITX (BGA) 210U	+	-	-	Intel 82574L	210U	PN 1037-0921
KT690/mITX (BGA) L325	+	-	-	Intel 82574L	L325	PN 1037-0921

^{* =} pin header



3.3 Processor support table.

The KT690/mITX and KT690/mITX-FW is designed to support the following socket S1 processors:

Processor Brand	Model	Clock Speed [MHz]	Cores	Thermal Guideline [Watt]	Embedded	Order Number
Mobile AMD Sempron™	2100+	1000	1	8W	Yes	SMF2100HAX3DQE
Mobile AMD Sempron™	3500+	1800	1	25W	Yes	SMS3500HAX4CME
Mobile AMD Sempron™	3600+	2000	1	25W	No	SMS3600HAX3DN
Mobile AMD Sempron™	3700+	2000	1	25W	Yes	SMS3700HAX4DQE
Mobile AMD Sempron™	3800+	2200	1	31W	No	SMD3800HAX3CM
Mobile AMD Sempron™	4000+	2200	1	31W	No	SMD4000HAX4DN
AMD Turion [™] 64 X2 Mobile Technology	TL52	1600	2	35W	Yes	TMDTL52HAX5CTE
AMD Turion [™] 64 X2 Mobile Technology	TL56	1800	2	35W	Yes	TMDTL56HAX5DME
AMD Turion™ 64 X2 Mobile Technology	TL58	1900	2	31W	No	TMDTL58HAX5DC
AMD Turion [™] 64 X2 Mobile Technology	TL60	2000	2	31W	No	TMDTL60HAX5DC
AMD Turion [™] 64 X2 Mobile Technology	TL62	2100	2	35W	Yes	TMDTL62HAX5DME
AMD Turion™ 64 X2 Mobile Technology	TL64	2200	2	35W	No	TMDTL64HAX5DC
AMD Turion™ 64 X2 Mobile Technology	TL66	2300	2	35W	No	TMDTL66HAX5DM
AMD Turion [™] 64 X2 Mobile Technology	TL68	2400	2	35W	No	TMDTL68HAX5DM

The KT690/mITX (BGA) is available with pre-mounted processors of the following types:

Processor Brand	Model	Clock Speed [MHz]	Cores	Thermal Guideline [Watt]	Embedded
AMD Sempron [™]	210U	1500	1	15W	Yes
AMD Athlon [™] Neo X2	L325	1500	2	18W	Yes



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3.4 System Memory

The motherboard provides two 200-pin DDR2 Small Outline Dual Inline Memory Module (SO-DIMM) sockets. Each slot can be populated with up to 16 GB of unbuffered DDR2 SO-DIMM modules resulting in a maximum of 32 GB system memory. (PT only up to 2x 4GB has been verified). Memory speeds up to DDR2-667 (PC2-5300) are supported.

3.4.1 Memory Configuration

Dual Channel configuration (128 bit) is enabled by populating both memory channels (DDR2 SLOT 1 and DDR2 SLOT 1). Populating only one memory slot results in 64-bit Single Channel mode.

Mode	DDR2 SLOT 1	DDR2 SLOT 2	
Single Channel (64 bit)	Populated	-	
Single Chainlei (04 bit)	•	Populated	
Dual Channel (128 bit)	Populated	Populated	



3.5 KT690 Fan / Heatsinks

PN 1022-1521 - Passive S1 cooler 35mm

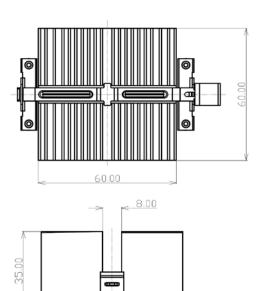
Supports 210U CPU with up to 55°C ambient.

PN 1043-2893 Cooler Passive BGA AMD S1 35mm

Supports CPUs with Thermal Design Power (TDP) up to 9W @ 60°C ambient.

Customer must ensure proper airflow in system





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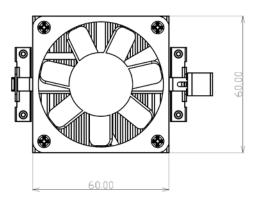
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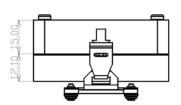
PN 823139 - AMD S1 cooler and PN 1037-0921 Cooler Active BGA AMD S1 35mm

Supports CPUs with Thermal Design Power (TDP) up to: 30W @ 60°C ambient and 35W @ 50°C ambient.

Customer must ensure proper airflow in system.









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3.6 KT690 Power State Map

POWER NET/STATE	S0#	S3#	S5#
+3V3	ON	OFF	OFF
+5V	ON	OFF	OFF
+12V	ON	OFF	OFF
-12V	ON	OFF	OFF
+VCORE	ON	OFF	OFF
+0V9_SUS	ON	ON	OFF
+1V2	ON	OFF	OFF
+1V2_CPU	ON	OFF	OFF
+1V8_SUS	ON	ON	OFF
+2V5_CPU_VDDA	ON	OFF	OFF
+3V3_CLK	ON	OFF	OFF
+3V3_DUAL	ON	ON	ON
+1V8	ON	OFF	OFF
+5V_DUAL	ON	ON	ON
+3V3_ETH1	ON	(ON)	(ON)
+3V3_ETH2	ON	(ON)	(ON)
+V_BAT	ON	ON	ON
+1V2_DUAL	ON	ON	ON
+5V_ALWAYS	ON	ON	ON
+2V5	ON	OFF	OFF
+1V5	ON	OFF	OFF

3.7 Power Consumption

In order to ensure safe operation of the board, the ATX power supply must monitor the supply voltage and shut down if the supplies are out of range – refer to the hardware manual for actual power specification.

The KT690/mITX and KT690/mITX-FW board is powered through the ATX connector and the additional 12V separate supply for CPU as specified in the ATX specification; besides this the power supplied to the board must be within the ATX specification.

The requirements to the supply voltages are as follows:

Supply	Min	Max	Note
Vcc3	3.14V	3.46V	Should be $\pm 5\%$ for compliance with the ATX specification
Vcc	4.75V	5.25V	Should be ±5% for compliance with the ATX specification
+12V	11.4V	12.6V	Should be ±5% for compliance with the ATX specification
-12V	-13.2V	-10.8V	Should be ±10% for compliance with the ATX specification
-5V	-5,50V	-4.5V	Not required for the KT690/mITX board
5VSB	4.75V	-5.25V	Should be ±5% for compliance with the ATX specification

Static Power Consumption

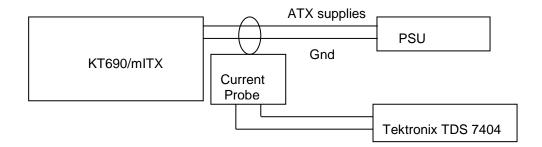
The power consumption of the KT690/mITX and KT690/mITX-FW Board is measured under:

- 1- WindowsXP, Running 3DMARK & CPU BURN, mean
- 2- WindowsXP, Running 3DMARK & CPU BURN, peak
- 3- S1, mean
- 4- S3, mean
- 5- Inrush, peak

Test setup

The following items were used in the test setup:

- 1. KT690/mITX board
- 2. 12V active cooler
- 3. PS/2 keyboard & mouse, CRT, HD, ATX PSU
- 4. Tektronix TDS 7404, P6345 probes
- 5. Fluke Current Probe 80i-100S AC/DC



Note: The Power consumption of CRT, HD and Fan is not included.



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KT690/mITX w/1.6GHz Turion 64 X2 2GB DDR2

Windows XP, 3DMARK2001 & CPUBURN, mean

Supply	Current draw	Power consumption
+12V	2.0A	24W
+5V	2.6A	13W
+3V3	1.1A	3.63W
-12V	0A	0W
5VSB	0A	0W
Total	X	40.63W

Windows XP, 3DMARK2001 & CPUBURN, peak

Supply	Current draw	Power consumption
+12V	2.4A	28.8W
+5V	3.2A	16W
+3V3	1.3A	4.29W
-12V	0A	0W
5VSB	0A	OW
Total	X	49.09W

S1, mean

Supply	Current draw	Power consumption
		•
+12V	0.24A	2.88W
+5V	1.4A	7.00W
+3V3	0.83A	2.74W
-12V	0.0A	OW
5VSB	0A	OW
Total	X	12.62W

S3, mean

Supply	Current draw	Power consumption
+12V	Χ	0W
+5V	Χ	0W
+3V3	Χ	0W
-12V	Χ	0W
5VSB	0.25A	1.25W
Total	X	1.25W

Supply	Current draw
+12V	2.0A
+5V	4.7A
+3V3	1.5A
-12V	0A
5VSB	2.5A



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KT690/mITX w/1.00GHz Sempron 2100+ 256MB DDR2

Windows XP, 3DMARK2001 & CPUBURN, mean

Supply	Current draw	Power consumption
+12V	0.65A	7.8W
+5V	1.9A	9.5W
+3V3	1.1A	3.63W
-12V	0A	0W
5VSB	0A	0W
Total	X	20.93W

Windows XP, 3DMARK2001 & CPUBURN, peak

Supply	Current draw	Power consumption
+12V	0.82A	9.84W
+5V	2.4A	12W
+3V3	1.3A	4.29W
-12V	0A	0W
5VSB	0A	0W
Total	X	26.13W

S1, mean

Supply	Current draw	Power consumption
+12V	0.3A	3.6W
+5V	1.4A	7W
+3V3	0.8A	2.64W
-12V	0A	OW
5VSB	0A	OW
Total	X	13.24W

S3, mean

Supply	Current draw	Power consumption
+12V	Χ	OW
+5V	Χ	OW
+3V3	X	OW
-12V	X	OW
5VSB	0.25A	1.25W
Total	X	1.25W

Supply	Current draw
+12V	1.4A
+5V	4.6A
+3V3	1.1A
-12V	0A
5VSB	2.5A



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KT690/mITX BGA w/ Dual Core 1.5GHz L325 + 2x2GB DDR2

Windows XP, 3DMARK2001 & CPUBURN, mean

Supply	Current draw	Power consumption
+12V	1.8A	21.6W
+5V	2.8A	14.0W
+3V3	1.2A	3,96W
-12V	0	0
5VSB	0	0
Total	X	39.56W

Windows XP, 3DMARK2001 & CPUBURN, peak

Supply	Current draw	Power consumption
+12V	2.06A	24,72W
+5V	3.06A	15,3W
+3V3	1.34A	4.4W
-12V	0A	OW
5VSB	0A	0W
Total	X	44.42W

S1, mean

Supply	Current draw	Power consumption
+12V	0.31A	3.72W
+5V	1.41A	7.05W
+3V3	0.84A	2.77W
-12V	0A	0
5VSB	0A	0
Total	X	13.54W

S3, mean

Supply	Current draw	Power consumption
+12V	0.019A	0.22W
+5V	0.08A	0.4W
+3V3	0.08A	0.26W
-12V	0.076A	0.91W
5VSB w WOL	0.40A	2.0W
5VSB wo WOL	0.31A	1.5W
Total	X	3.3 – 3.8W

S5, mean

Supply	Current draw	Power consumption
5VSB w WOL	0.28A	1.4W
5VSB wo WOL	0.19A	0.9W

Supply	Current draw
+12V	7.2 A
+5V	4.4A
+3V3	2.0A
-12V	0A
5VSB	5.28A



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KT690/mITX BGA w/ Single Core 1.5GHz 210U + 2x2GB DDR2

Windows XP, 3DMARK2001 & CPUBURN, mean

Supply	Current draw	Power consumption
+12V	1.18A	14,16W
+5V	2.05A	10.25W
+3V3	0.9A	2.97W
-12V	0	0
5VSB	0	0
Total	X	27.38W

Windows XP, 3DMARK2001 & CPUBURN, peak

Supply	Current draw	Power consumption				
+12V	1.2A	14.4W				
+5V	2.72A	13.6W				
+3V3	0.9A	2.97W				
-12V	0A	0W				
5VSB	0A	0W				
Total	X	30.97W				

S1, mean

Supply	Current draw	Power consumption
+12V	0.38A	4.56W
+5V	1.15A	5.75W
+3V3	0.87A	2.87W
-12V	0A	0
5VSB	0A	0
Total	X	13.18W

S3, mean

Supply	Current draw	Power consumption
+12V	0.08A	0.96W
+5V	0,08A	0.4W
+3V3	0.068A	0.22W
-12V	0.074A	0.88W
5VSB w WOL	0.40A	2.0W
5VSB wo WOL	0.31A	1.5W
Total	X	3.96 – 4.46W

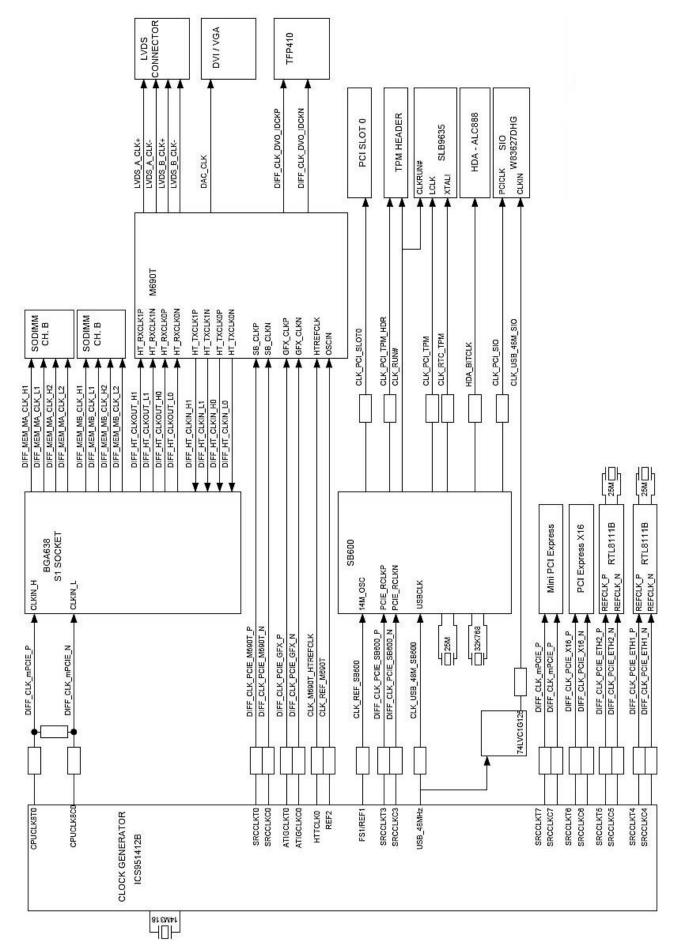
S5, mean

Supply	Current draw	Power consumption
5VSB w WOL	0.28A	1.4W
5VSB wo WOL	0.19A	0.9W

Supply	Current draw
+12V	7.44A
+5V	4.64A
+3V3	2.2A
-12V	0
5VSB	5.6A

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3.8 KT690 Clock Distribution



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4. Connector Definitions

The following sections provide pin definitions and detailed description of all on-board connectors.

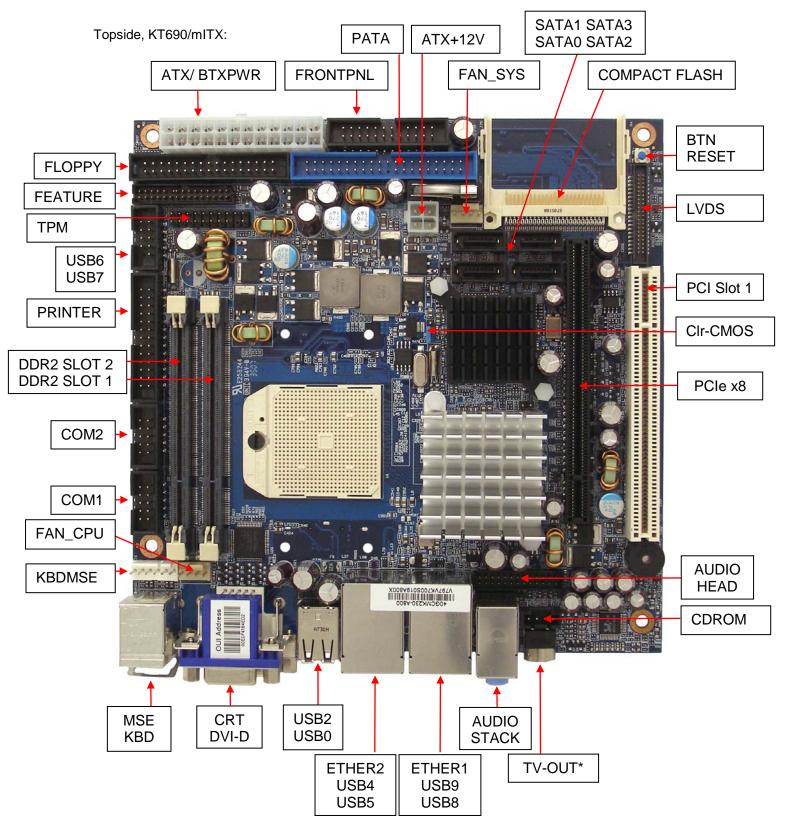
The connector definitions follow the following notation:

Column name	Description	Description					
Pin		pin-numbers in the connector. The graphical layout of the connector definition nade similar to the physical connectors.					
Signal	The mnem	nonic name of the signal at the current pin. The notation "XX#" states that the signal tive low.					
Туре	AI:	Analog Input.					
	AO:	Analog Output.					
	1:	Input, TTL compatible if nothing else stated.					
	IO:	Input / Output. TTL compatible if nothing else stated.					
	IOT: Bi-directional tristate IO pin.						
	IS: Schmitt-trigger input, TTL compatible.						
	IOC:	Input / open-collector Output, TTL compatible.					
	NC:	Pin not connected.					
	O:	Output, TTL compatible.					
	OC:	Output, open-collector or open-drain, TTL compatible.					
	OT: Output with tri-state capability, TTL compatible.						
	LVDS:	Low Voltage Differential Signal.					
	PWR:	Power supply or ground reference pins.					
		al current in mA flowing out of an output pin through a grounded load, while the tage is > 2.4 V DC (if nothing else stated).					
	Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).						
Pull U/D	On-board	pull-up or pull-down resistors on input pins or open-collector output pins.					
Note	Special re	marks concerning the signal.					

The abbreviation *TBD* is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

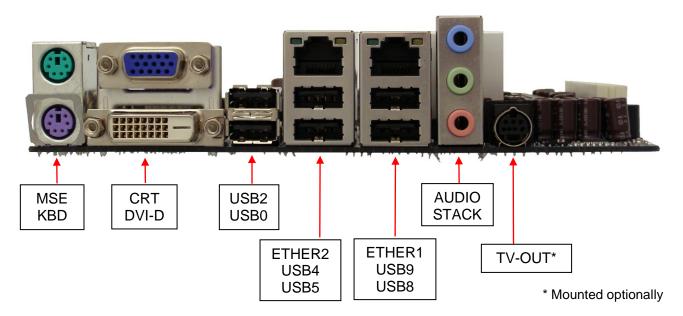
4.1 Connector layout

4.1.1 KT690/mITX

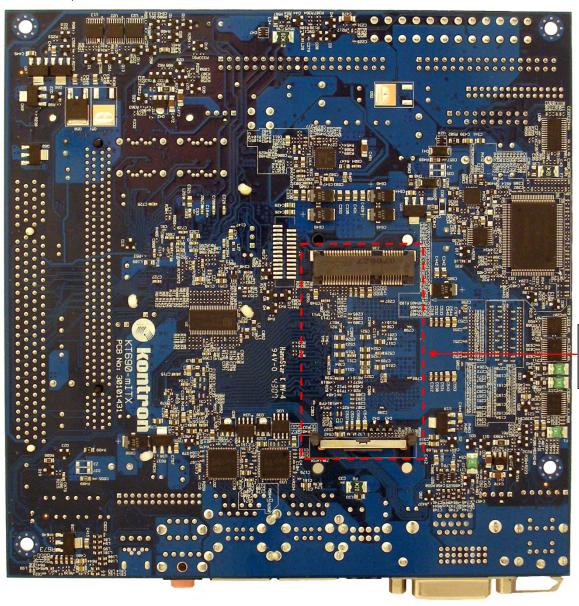


^{*} Mounted optionally

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Backside, KT690/mITX:

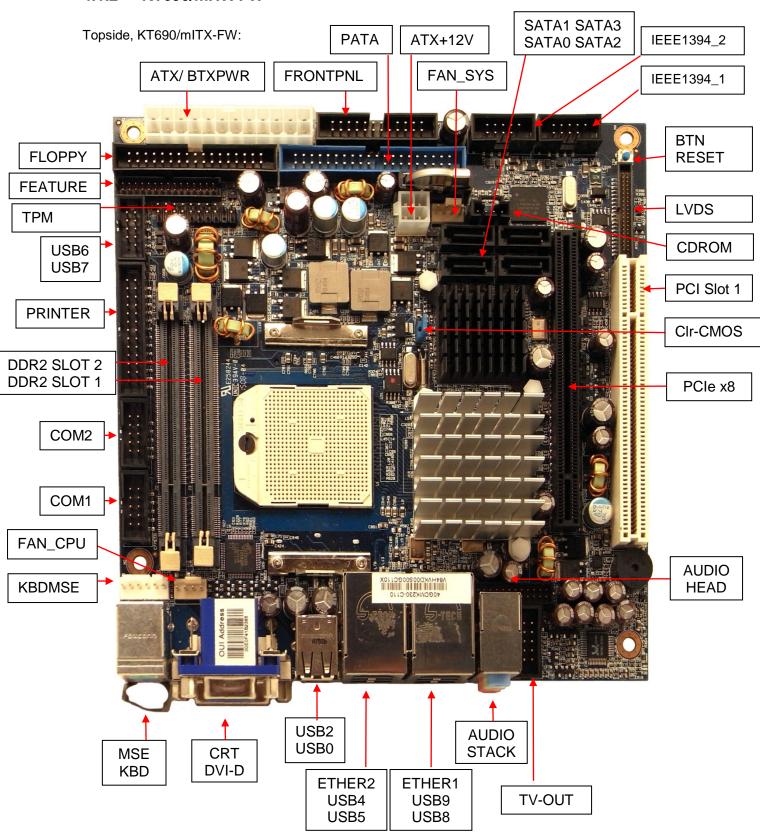


Mini-PCI express slot



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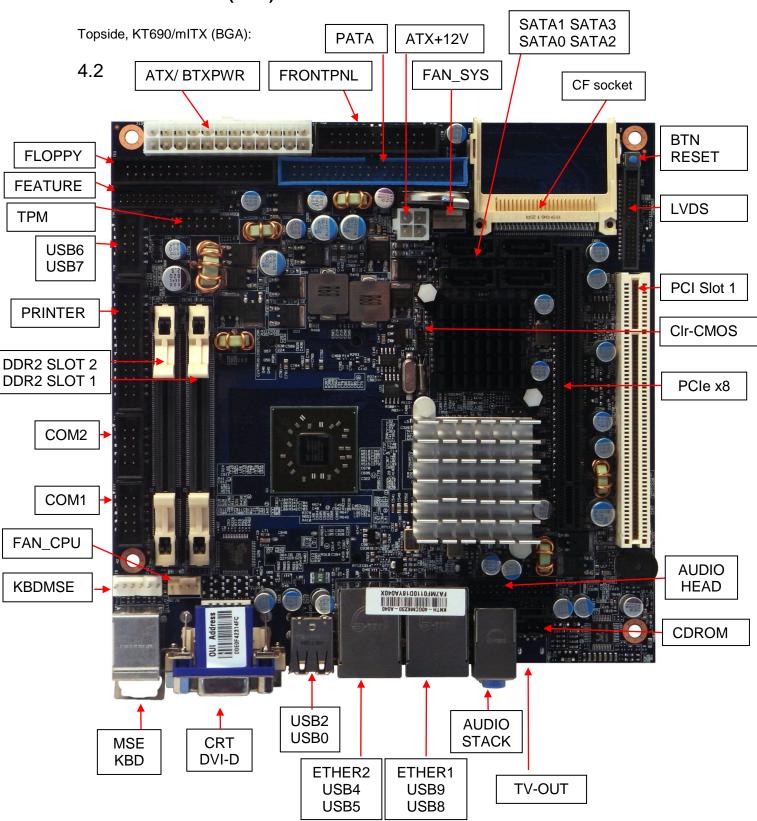
4.1.2 KT690/mITX-FW





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Power Connector (ATXPWR)

The KT690 boards are designed to be supplied from a standard ATX or BTX power supply.

ATX/ BTX Power Connector:

	Pull				Р	IN				Pull	
Note	U/D	loh/lol	Type	Signal			Signal	Type	loh/lol	U/D	Note
	-	-	PWR	3V3	12	24	GND	PWR	-	-	
			PWR	+12V	11	23	5V	PWR			
			PWR	+12V	10	22	5V	PWR			
	-	-	PWR	SB5V	9	21	5V	PWR	-	-	
	-	-		P_OK	8	20	-5V	PWR	-	-	1
	-	-	PWR	GND	7	19	GND	PWR	-	-	
	-	-	PWR	5V	6	18	GND	PWR	-	-	
	-	-	PWR	GND	5	17	GND	PWR	-	-	
	-	-	PWR	5V	4	16	PSON#	OC	-	-	
	-	-	PWR	GND	3	15	GND	PWR	-	-	
	-	-	PWR	3V3	2	14	-12V	PWR	-	•	
	•	-	PWR	3V3	1	13	3V3	PWR	-	•	

Note 1: -5V supply is not used onboard.

Note 2: Use of BTX supply not required for operation, but may be required to drive high-power PCI Express x16 Add cards.

ATX+12V Power Connector:

	Pull				PIN		PIN					Pull	
Note	U/D	loh/lol	Type	Signal			Signal	Type	loh/lol	U/D	Note		
1	-	-	PWR	GND	1	3	+12V	PWR	-	-	1		
1			PWR	GND	2	4	+12V	PWR			1		

Note 1: Use of the 4-pin ATX+12V Power Connector is required for operation of the KT690 boards.

See chapter "Power Consumption" regarding input tolerances on 3.3V, 5V, SB5V, +12 and -12V (also refer to ATX specification version 2.2).

Control signal description:

Signal	Description
P_OK	P_OK is a power good signal and should be asserted high by the power supply to indicate that the +5VDC and +3.3VDC outputs are above the undervoltage thresholds of the power supply. When this signal is asserted high, there should be sufficient energy stored by the converter to guarantee continuous power operation within specification. Conversely, when the output voltages fall below the undervoltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, P_OK should be de-asserted to a low state. The recommended electrical and timing characteristics of the P_OK (PWR_OK) signal are provided in the <i>ATX12V Power SupplyDesign Guide</i> . It is strongly recommended to use an ATX or BTX supply with the KT690 boards, in order to
	implement the supervision of the 5V and 3V3 supplies. These supplies are not supervised onboard the KT690 boards.
PS_ON#	Active low open drain signal from the board to the power supply to turn on the power supply outputs. Signal must be pulled high by the power supply.



4.3 Keyboard and PS/2 mouse connectors

Attachment of a keyboard or PS/2 mouse adapter can be done through the stacked PS/2 mouse and keyboard connector (MSE & KBD).

Both interfaces utilize open-drain signaling with on-board pull-up.

The PS/2 mouse and keyboard is supplied from SB5V when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resetable fuse.

4.3.1 Stacked MINI-DIN keyboard and mouse Connector (MSE & KBD)

Note	Pull U/D	loh/lol	Туре	Signal	PIN					Signal	Туре	loh/lol	Pull U/D	Note
	-	-	-	NC	6			ļ	5	MSCLK	IOC	TBD	2K7	
						=								
	-	•	PWR	5V/SB5V	4		_		3	GND	PWR	•	-	
	-	-	-	NC		2		1		MSDAT	IOC	TBD	2K7	
			-	NC	6				5	KBDCLK	IOC	TBD	2K7	
						_								
	-	-	PWR	5V/SB5V	4		_		3	GND	PWR	-	-	
	-	-	-	NC		2		1		KBDDAT	IOC	TBD	2K7	

Signal Description – Keyboard & and mouse Connector (MSE & KBD), see below.

4.3.2 Keyboard and mouse pin-row Connector (KBDMSE)

PIN	Signal	Туре	loh/lol	Pull U/D	Note
1	KBDCLK	IOC	TBD	4K7	
2	KBDDAT	IOC	TBD	4K7	
3	MSCLK	IOC	TBD	4K7	
4	MSDAT	IOC	TBD	4K7	
5	5V/SB5V	PWR	-	-	
6	GND	PWR	-	-	

Signal Description – Keyboard & and mouse Connector (KBDMSE).

Signal	Description
MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.
KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

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4.4 Display Connectors

The KT690 board provides:

- 1. Analog CRT interface (IO Bracket)
- 2. Digital DVI (DVI-D) (IO Bracket)
- 3. LVDS connector (internal connector)
- 4. TV-Out (IO Bracket) ("KT690/mITX w. TV-out" only)
- 5. TV-Out (Internal pin header) ("KT690/mITX-FW w. TV-out" only)

The KT690 board does not support ADD2 / SDVO cards on the PCI Express x16 connector.

The KT690 integrates the ATI Radeon™ X1250 Graphics Core with support for Dual Clone display and Dual independent display.

The supported combinations are listed in the below matrix:

		Primary Display									
		CRT	DVI-D	LVDS	TV-Out						
ý	CRT		Clone / Dual	Clone / Dual	Not supported						
ndar olay	DVI-D	Clone / Dual		Clone / Dual	Clone / Dual						
Secondary Display	LVDS	Clone / Dual	Clone / Dual		Clone / Dual						
Ň	TV-Out	Not supported	Clone / Dual	Clone / Dual							



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4.4.1 CRT Connector (CRT)

	Pull					PIN					Pull	
Note	U/D	loh/lol	Type	Signal				Signal	Туре	loh/lol	U/D	Note
						_						
					·	6		GND	PWR	-	•	
	/75R	*	A0	RED	1		11	NC	-	-	•	
						7		GND	PWR	-	-	
	/75R	*	A0	GREEN	2		12	DDCDAT	10	TBD	6K81	2
						8		GND	PWR	-	-	
	/75R	*	A0	BLUE	3		13	HSYNC	0	TBD		
						9		5V	PWR	-	-	1
	-	-	-	NC	4		14	VSYNC	0	TBD		
						10		GND	PWR	-	-	
	-	-	PWR	GND	5		15	DDCCLK	Ю	TBD	6K81	2

Note 1: The 5V supply in the CRT connector is fused by a 1.1A reset-able fuse.

Note 2: Pull-up to +5V.

Signal Description - CRT Connector:

Signal	Description
HSYNC	CRT horizontal synchronization output.
VSYNC	CRT vertical synchronization output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red color signal to the CRT. For 75 Ohm cable impedance.
GREEN	Analog output carrying the green color signal to the CRT. For 75 Ohm cable impedance.
BLUE	Analog output carrying the blue color signal to the CRT. For 75 Ohm cable impedance.
DIG-GND	Ground reference for HSYNC and VSYNC.
ANA-GND	Ground reference for RED, GREEN, and BLUE.



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4.4.2 DVI Connector (DVI-D, digital only)

1	2	3	4	5	6	7	8	
9	10	11	12	13	14	15	16	
17	18	19	20	21	22	23	24	

Female socket, front view

Note: DVI analogue signals are not supported

Signal Description - DVI Connector:

Pin No.	Signal	Description	Туре	Pull Up
1	TMDS Data 2-	Digital Red – (Link 1)	LVDS OUT	
2	TMDS Data 2+	Digital Red + (Link 1)	LVDS OUT	
3	TMDS Data 2/4 Shield		PWR	
4	N.C.		-	
5	N.C.		-	
6	DDC Clock	DDC Clock	IO	2K2
7	DDC Data	DDC Data	IO	2K2
8	N.C.		-	
9	TMDS Data 1-	Digital Green – (Link 1)	LVDS OUT	
10	TMDS Data 1+	Digital Green + (Link 1)	LVDS OUT	
11	TMDS Data 1/3 Shield		PWR	
12	N.C.		-	
13	N.C.		-	
14	+5V (55mA)	Power for monitor when in standby	PWR	
15	GND		PWR	
16	Hot Plug Detect	Hot Plug Detect	I	
17	TMDS Data 0-	Digital Blue – (Link 1) / Digital sync	LVDS OUT	
18	TMDS Data 0+	Digital Blue + (Link 1) / Digital sync	LVDS OUT	
19	TMDS Data 0/5 Shield		PWR	
20	N.C.		-	
21	N.C.		-	
22	TMDS Clock Shield		PWR	
23	TMDS Clock+	Digital clock + (Link 1)	LVDS OUT	
24	TMDS Clock-	Digital clock - (Link 1)	LVDS OUT	
C1 - C5	N.C.		-	



4.4.3 LVDS Flat Panel Connector (LVDS)

Note	Type	Signal	Р	in	Signal	Type	Note
Max. 0.5A	PWR	+12V	1	2	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	3	4	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	5	6	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	+5V	7	8	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	LCDVCC	9	10	LCDVCC	PWR	Max. 0.5A
2K2Ω, 3.3V	OT	DDC CLK	11	12	DDC DATA	OT	2K2Ω, 3.3V
3.3V level	OT	BKLTCTL	13	14	VDD ENABLE	OT	3.3V level
3.3V level	OT	BKLTEN#	15	16	GND	PWR	Max. 0.5A
	LVDS	LVDS A0-	17	18	LVDS A0+	LVDS	
	LVDS	LVDS A1-	19	20	LVDS A1+	LVDS	
	LVDS	LVDS A2-	21	22	LVDS A2+	LVDS	
	LVDS	LVDS ACLK-	23	24	LVDS ACLK+	LVDS	
	LVDS	LVDS A3-	25	26	LVDS A3+	LVDS	
Max. 0.5A	PWR	GND	27	28	GND	PWR	Max. 0.5A
	LVDS	LVDS B0-	29	30	LVDS B0+	LVDS	
	LVDS	LVDS B1-	31	32	LVDS B1+	LVDS	
	LVDS	LVDS B2-	33	34	LVDS B2+	LVDS	
	LVDS	LVDS BCLK-	35	36	LVDS BCLK+	LVDS	
	LVDS	LVDS B3-	37	38	LVDS B3+	LVDS	
Max. 0.5A	PWR	GND	39	40	GND	PWR	Max. 0.5A

Note 1: The KT690 board support dual channel, 24bit OpenLDI/ SPWG panels on the LVDS interface

Signal Description – LVDS Flat Panel Connector:

Signal	Description
LVDS A0A3	LVDS A Channel data
LVDS ACLK	LVDS A Channel clock
LVDS B0B3	LVDS B Channel data
LVDS BCLK	LVDS B Channel clock
BKLTCTL	Backlight control (1), PWM signal to implement voltage in the range 0-3.3V
BKLTEN#	Backlight Enable signal (active low) (2)
VDD ENABLE	Output Display Enable.
LCDVCC	VCC supply to the flat panel. This supply includes power-on/off sequencing. The flat panel supply may be either 5V DC or 3.3V DC depending on the CMOS configuration. Maximum load is 1A at both voltages.
DDC CLK	DDC Channel Clock
DDC DATA	DDC Channel Data

Note 1) Windows API will be available to operate the BKLTCTL signal. Some Inverters has a limited voltage range 0- 2.5V for this signal: If voltage is > 2.5V the Inverter might latch up. Some Inverters generates noise to the BKLTCTL signal resulting in making the lvds transmision fail (corrupted picture on the display). By adding 1K Ohm resistor in series with this signal and mounted in the Inverter end of the cable kit the noise is limited and picture is stabil.

Note 2) If the Backlight Enable is required to be active high then make the BIOS Chipset setting: Backlight Signal Inversion = Enabled.



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4.4.4 TV-Out (Optional)

The KT690/mITX boards include TV-Out connector with support for Component, S-Video and Composite Output interfaces and NTSC/ PAL output format.

The KT690 board includes Macrovision support.

IMPORTANT: If the TV-Out option is available then you must make agreement with Macrovision (http://www.macrovision.com/) about licence fee. Only Macrovision (not Kontron) can determine the actual licence fee which depends on the application.

KT690/mITX TV-Out connector:

Note	Pull U/D	loh/lol	Туре	Signal	PIN					Signal	Туре	loh/lol	Pull U/D	Note
								$\overline{}$		GND				
				TVDACC		4	7	3	\	TVDACB				
				GND		2 6	5	1		GND				
				GND	1	<u></u>				TVDACA				
						7		7						

Signal	Description					
TVDACA	TVDAC Channel A output supports: Composite: CVBS signal Component: Chrominance (Pb) analog signal					
TVDACB	TVDAC Channel B output supports: S-Video: Luminance analog signal Component: Luminance (Y) analog signal					
TVDACC	TVDAC Channel C output supports: S-Video: Chrominance analog signal Component: Chrominance (Pr) analog signal					

KT690/mITX-FW TV-Out connector:

Note	Pull U/D	loh/lol	Туре	Signal	PIN		Signal	Туре	loh/lol	Pull U/D	Note
				TVDACC	1	2	TVDACB				
				SMBC	3	4	TVDACA				
				SMBD	5	6	-12V				
				+5V	7	8	+12V				
				GND	9	10	GND				

4.5 PCI-Express Connectors

The KT690 board contains one 8-lane (x8) PCI Express port on a PCI Express x16 connector. The PCI Express port is compliant to the PCI Express Specification revision 1.1a.

The x8 port operates at a frequency of 2.5 Gb/s on each lane; the port supports a maximum theoretical bandwidth of 20 Gb/s in each direction.

The 8-lane (x8) PCI Express port supports:

- 1. An external graphics device utilizing all 8 lanes
- 2. A single x1, x2 or x4 general purpose PCI Express link

The PCI Express port does not support SDVO and ADD2 cards.

4.5.1 PCI-Express x8

The KT690 boards supports one 8-lane (x8) PCI Express port for external PCI Express based graphics boards.

Note Type		Signal	Р	IN	Signal	Type	Note
		+12V	B1	A1	NC		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE_x16 CLK		
		PEG_TXP[0]	B14	A14	PCIE_x16 CLK#		
		PEG_TXN[0]	B15	A15	GND		
		GND	B16	A16	PEG_RXP[0]		
		I2C_CLK	B17	A17	PEG_RXN[0]		
		GND	B18	A18	GND		
		PEG_TXP[1]	B19	A19	NC		
		PEG_TXN[1]	B20	A20	GND		
		GND	B21	A21	PEG_RXP[1]		
		GND	B22	A22	PEG_RXN[1]		
		PEG_TXP[2]	B23	A23	GND		
		PEG_TXN[2]	B24	A24	GND		
		GND	B25	A25	PEG_RXP[2]		
		GND	B26	A26	PEG_RXN[2]		
		PEG_TXP[3]	B27	A27	GND		
		PEG_TXN[3]	B28	A28	GND		
		GND	B29	A29	PEG_RXP[3]		
		NC	B30	A30	PEG_RXN[3]		
		DDC_DATA	B31	A31	GND		
		GND	B32	A32	NC		
		PEG_TXP[4]	B33	A33	NC		
		PEG_TXN[4]	B34	A34	GND		
		GND	B35	A35	PEG_RXP[4]		
		GND	B36	A36	PEG_RXN[4]		
		PEG_TXP[5]	B37	A37	GND		
		PEG_TXN[5]	B38	A38	GND		
		GND	B39	A39	PEG_RXP[5]		
		GND	B40	A40	PEG_RXN[5]		
		PEG_TXP[6]	B41	A41	GND		
		PEG_TXN[6]	B42	A42	GND		
		GND	B43	A43	PEG_RXP[6]		
		GND	B44	A44	PEG_RXN[6]		
		PEG_TXP[7]	B45	A45	GND		
		PEG_TXN[7]	B46	A46	GND		
		GND	B47	A47	PEG_RXP[7]		

(continues)



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PRSNT#2	B48	A48	PEG_RXN[7]	
GND	B49	A49	GND	
NC	B50	A50	NC	
NC	B51	A51	GND	
GND	B52	A52	NC	
GND	B53	A53	NC	
NC	B54	A54	GND	
NC	B55	A55	GND	
GND	B56	A56	NC	
GND	B57	A57	NC	
NC	B58	A58	GND	
NC	B59	A59	GND	
GND	B60	A60	NC	
GND	B61	A61	NC	
NC	B62	A62	GND	
NC	B63	A63	GND	
GND	B64	A64	NC	
GND	B65	A65	NC	
NC	B66	A66	GND	
NC	B67	A67	GND	
GND	B68	A68	NC	
GND	B69	A69	NC	
NC	B70	A70	GND	
NC	B71	A71	GND	
GND	B72	A72	NC	
GND	B73	A73	NC	
NC	B74	A74	GND	
NC	B75	A75	GND	
GND	B76	A76	NC	
GND	B77	A77	NC	
NC	B78	A78	GND	
NC	B79	A79	GND	
GND	B80	A80	NC	
NC	B81	A81	NC	
NC	B82	A82	GND	



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4.5.2 miniPCI-Express connector

The KT690 board supports one miniPCI Express port compliant to the Mini PCI Specification, Revision 1.0.

This allows for implementation for small form factor PCI cards also referred to as Mini PCI Cards.

Note	Type	Signal	Р	IN	Signal	Type	Note
		WAKE#	1	2	+3V3		
		NC	3	4	GND		
		NC	5	6	+1.5V		
		NC	7	8	NC		
		GND	9	10	NC		
		PCIE_mini CLK#	11	12	NC		
		PCIE_mini CLK	13	14	NC		
		GND	15	16	NC		
		NC	17	18	GND		
		NC	19	20	W_Disable		
		GND	21	22	RST#		
		PCIE_RXN	23	24	+3V3		
		PCIE_RXP	25	26	GND		
		GND	27	28	+1.5V		
		GND	29	30	SMB_CLK		
		PCIE_TXN	31	32	SMB_DATA		
		PCIE_TXP	33	34	GND		
		GND	35	36	NC		
		NC	37	38	NC		
		NC	39	40	GND		
		NC	41	42	NC		
		NC	43	44	NC		
		NC	45	46	NC		
		NC	47	48	+1.5V		
		NC	49	50	GND		
		NC	51	52	+3V3		



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4.6 Parallel ATA harddisk interface

One parallel ATA harddisk controllers is available on the board – a primary controller. Standard 3½" harddisks or CD-ROM drives may be attached to the primary controller by means of the 40 pin IDC connector, PATA.

The parallel ATA harddisk controller is shared between the PATA connector and the CF connector.

If the CF connector is not used then two devices (a primary and a secondary device) are supported on the PATA interface.

The harddisk controllers support Bus master IDE, ultra DMA 33/66/100/133 MHz and standard operation modes. For support of ultra DMA 66/100/133 MHz, a 80-wire cable is required.

If the CF connector is used then only one PATA device is supported and only by use of 40-wire cable (not 80-wire cable). Optionally use SATA device(s).

The signals used for the harddisk interface are the following:

Signal	Description
DAA20	Address lines, used to address the I/O registers in the IDE hard disk.
HDCSA10#	Hard Disk Chip-Select. HDCS0# selects the primary hard disk.
DA158	High part of data bus.
DA70	Low part of data bus.
IORA#	I/O Read.
IOWA#	I/O Write.
IORDYA#	This signal may be driven by the hard disk to extend the current I/O cycle.
RESETA#	Reset signal to the hard disk.
HDIRQA	Interrupt line from hard disk.
CBLIDA	This input signal (CaBLe ID) is used to detect the type of attached cable: 80-wire cable when low input and 40-wire cable when 5V via 10Kohm (pull-up resistor).
DDREQA	Disk DMA Request might be driven by the IDE hard disk to request bus master access to the PCI bus. The signal is used in conjunction with the PCI bus master IDE function and is not associated with any PC-AT bus compatible DMA channel.
DDACKA#	Disk DMA Acknowledge. Active low signal grants IDE bus master access to the PCI bus.
HDACTA#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signals from primary and secondary controller are routed together through diodes and passed to the connector FEATURE.

All of the above signals are compliant to [4].

The pinout of the connectors are defined in the following sections.



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4.6.1 IDE Hard Disk Connector (PATA)

This connector can be used for connection of two primary IDE drives.

Note	Pull U/D	loh/lol	Туре	Signal	Pl	IN	Signal	Туре	loh/lol	Pull U/D	Note
	-	TBD	0	RESET_P#	1	2	GND	PWR	-	-	
	-	TBD	10	DA7	3	4	DA8	10	TBD	-	
	-	TBD	10	DA6	5	6	DA9	10	TBD	-	
	-	TBD	10	DA5	7	8	DA10	Ю	TBD	•	
	-	TBD	10	DA4	9	10	DA11	Ю	TBD	•	
	-	TBD	10	DA3	11	12	DA12	10	TBD	-	
	-	TBD	IO	DA2	13	14	DA13	Ю	TBD	-	
	-	TBD	IO	DA1	15	16	DA14	Ю	TBD	-	
	-	TBD	10	DA0	17	18	DA15	Ю	TBD	•	
	-	-	PWR	GND	19	20	KEY	-	-	-	
	-	-	- 1	DDRQA	21	22	GND	PWR	-	-	
	-	TBD	0	IOWA#	23	24	GND	PWR	•	•	
	-	TBD	0	IORA#	25	26	GND	PWR	-	-	
	4K7	-	- 1	IORDYA	27	28	GND	PWR	-	-	
	-	-	0	DDACKA#	29	30	GND	PWR	•	•	
	10K	-	1	HDIRQA	31	32	NC	-	•	ı	
	-	TBD	0	DAA1	33	34	CBLIDA#	ı	-		
	-	TBD	0	DAA0	35	36	DAA2	0	TBD	-	
	-	TBD	0	HDCSA0#	37	38	HDCSA1#	0	TBD	•	
	-	-	I	HDACTA#	39	40	GND	PWR	-	-	

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4.6.2 CF Connector (CF)

This connector is mounted on the topside of the KT690/mITX (CF is not available on KT690/mITX-FW).

The CF socket support DMA/UDMA modules up to UDMA2.

NOTE: If the CF connector is used then only one PATA device is supported and only by use of 40-wire cable (not 80-wire cable). Optionally use SATA device(s). Normally CF is Master and then possible PATA device must be Slave.

Note	Pull U/D	loh/lol	Туре	Signal	Pl	IN	Signal	Туре	loh/lol	Pull U/D	Note
2	-	-	-	NC	26	1	GND	PWR	-	-	1
	-	TBD	Ю	DA11	27	2	DB3	10	TBD	-	
	-	TBD	Ю	DA12	28	3	DB4	10	TBD	-	
	-	TBD	Ю	DA13	29	4	DB5	10	TBD	-	
	-	TBD	10	DA14	30	5	DB6	IO	TBD	-	
	-	TBD	Ю	DA15	31	6	DB7	IO	TBD	-	
	-	TBD	0	HDCSA1#	32	7	HDCSA0#	0	TBD	-	
	-	-	-	NC	33	8	GND	PWR	-	-	
	-	TBD	0	IORA#	34	9	GND	PWR	-	-	
	-	TBD	0	IOWA#	35	10	GND	PWR	-	-	
	-	-	PWR	5V	36	11	GND	PWR	-	-	
	8K2	-	I	HDIRQA	37	12	GND	PWR	-	-	
	-	-	PWR	5V	38	13	5V	PWR	-	-	
	-	-	PWR	GND	39	14	GND	PWR	-	-	
	-	-	-	NC	40	15	GND	PWR	-	-	
	-	TBD	0	RESET_C#	41	16	GND	PWR	-	-	
	4K7	-		IORDYA	42	17	GND	PWR	-	-	
	-	-	I	DDRQA	43	18	DAA2	0	-	-	
	-	-	0	DDACKA#	44	19	DAA1	0	-	-	
	-	-		HDACTA#	45	20	DAA0	0	-	-	
	-	-	I	CBLIDA#	46	21	DB0	Ю	TBD	-	
	-	TBD	Ю	DB8	47	22	DB1	10	TBD	-	
	-	TBD	Ю	DB9	48	23	DB2	Ю	TBD	-	
	-	TBD	Ю	DB10	49	24	NC				
1	-	-	PWR	GND	50	25	NC	-	-	-	2

Note 1: Pin is longer than average length of the other pins.

Note 2: Pin is shorter than average length of the other pins.

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4.7 Serial ATA harddisk interface

The KT690 boards have an integrated SATA Host controller that supports independent operation on four ports and data transfer rates of up to 3.0Gb/s (300MB/s). The SATA controller supports AHCI mode and has integrated RAID functionality with support for RAID modes 0, 1 and 10.

The board provides four Serial ATA (SATA) connectors, which support one device per connector. The SB600 Southbridge Serial ATA controller offers four independent Serial ATA ports with a theoretical maximum transfer rate of 3 Gbits/sec per port.

A point-to-point interface is used for host to device connections, unlike Parallel ATA IDE which supports a master/slave configuration and two devices per channel.

For compatibility, the underlying Serial ATA functionality is transparent to the operating system. The Serial ATA controller can operate in both legacy and native modes. In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15). In Native mode, standard PCI Conventional bus resource steering is used. Native mode is the preferred mode for configurations using the Windows XP and Windows 2000 operating systems.

The KT690 supports the following RAID (Redundant Array of Independent Drives) levels:

- RAID 0 data striping
- RAID 1 data mirroring
- RAID 0+1 (or RAID 10) data striping and mirroring

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 Toward Or and linear Control of the striping and mirroring and mirr

Limitations depending on Target Operating System apply.

4.7.1 SATA Hard Disk Connector (SATA0, SATA1, SATA2, SATA3)

SATA:

PIN	Signal	Туре	loh/lol	Pull U/D	Note
Key					
1	GND	PWR	-	-	
2	SATA* TX+				
3	SATA* TX-				
4	GND	PWR	-	-	
5	SATA* RX-				
6	SATA* RX+				
7	GND	PWR	-	-	

The signals used for the primary Serial ATA harddisk interface are the following:

Signal	Description
SATA* RX+	Host transmitter differential signal pair
SATA* RX-	
SATA* TX+	Host receiver differential signal pair
SATA* TX-	

[&]quot;*" specifies 0, 1, 2, and 3 depending on SATA port.

All of the above signals are compliant to [4].



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4.8 Firewire/ IEEE-1394 connectors.

The KT690/mITX-FW board supports two IEEE Std 1394a-2000 fully compliant cable ports at 100M bits/s, 200Mbits/s, and 400M bits/s.

Note: Firewire interface is not available on the KT690/mITX board.

4.8.1 IEEE1394 Connector (IEEE1394_1 and IEEE1394_2)

The pinout of the Firewire / IEEE1394 connectors are as follows:

Note	Pull U/D	loh/lol	Туре	Signal	PIN		Signal	Туре	loh/lol	Pull U/D	Note
				TPA1+	1	2	TPA1-				
				GND	3	4	GND				
				TPB1+	5	6	TPB1-				
1				+12V	7	8	+12V				1
				KEY	9	10	GND				

Note 1: The 12V supply for the IEEE1394 devices is on-board fused with a 1.5A reset-able fuse.

Signal	Description
TPA1+	Differential signal pair A
TPA1-	
TPB1+	Differential signal pair B
TPB1-	
+12V	+12V supply

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4.9 Printer Port Connector (PRINTER).

The signal definition in standard printer port mode is as follows:

Note	Pull U/D	loh/lol	Туре	Signal	Р	IN	Signal	Туре	loh/lol	Pull U/D	Note
	2K2	(24)/24	OC(O)	STB#	1	2	AFD#	OC(O)	(24)/24	2K2	
	2K2	24/24	10	PD0	3	4	ERR#	l	-	2K2	
	2K2	24/24	10	PD1	5	6	INIT#	OC(O)	(24)/24	2K2	
	2K2	24/24	10	PD2	7	8	SLIN#	OC(O)	(24)/24	2K2	
	2K2	24/24	10	PD3	9	10	GND	PWR	-	-	
	2K2	24/24	10	PD4	11	12	GND	PWR	•	-	
	2K2	24/24	10	PD5	13	14	GND	PWR	•	-	
	2K2	24/24	10	PD6	15	16	GND	PWR	1	-	
	2K2	24/24	10	PD7	17	18	GND	PWR	•	-	
	2K2	-		ACK#	19	20	GND	PWR	•	-	
	2K2	-	Ī	BUSY	21	22	GND	PWR	-	-	
	2K2	-		PE	23	24	GND	PWR	•	-	
	2K2	-	I	SLCT	25	26	GND	PWR	-	-	

The interpretation of the signals in standard Centronics mode (SPP) with a printer attached is as follows:

Signal	Description
PD70	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Signal to select the printer sent from CPU board to printer.
SLCT	Signal from printer to indicate that the printer is selected.
STB#	This signal indicates to the printer that data at PD70 are valid.
BUSY	Signal from printer indicating that the printer cannot accept further data.
ACK#	Signal from printer indicating that the printer has received the data and is ready to accept further data.
INIT#	This active low output initializes (resets) the printer.
AFD#	This active low output causes the printer to add a line feed after each line printed.
ERR#	Signal from printer indicating that an error has been detected.
PE#	Signal from printer indicating that the printer is out of paper.

The printer port additionally supports operation in the EPP and ECP mode as defined in [3].



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4.10 Floppy connector (FLOPPY).

The KT690 supports connection of one standard 1.44M Floppy Disk Drive. The Floppy Drive shall be connected as A: (The "last" connector on a standard Floppy Disk cable kit).

	Pull				Р	IN				Pull	
Note	U/D	loh/lol	Type	Signal			Signal	Type	loh/lol	U/D	Note
	-	-	PWR	GND	1	2	DENSEL0#	ОС	/48	-	
	-	-	PWR	GND	3	4	NC	-	-	-	
	-	-	PWR	GND	5	6	NC	-	-	-	
	-	-	PWR	GND	7	8	INDEX#	IS	-	330R	
	-	-	PWR	GND	9	10	MOTEA#	OC	/48	-	
	-	-	PWR	GND	11	12	NC	-	-	-	
	-	-	PWR	GND	13	14	DRVA#	OC	/48	-	
	-	-	PWR	GND	15	16	NC	-	-	-	
	-	-	PWR	GND	17	18	DIR#	OC	/48	-	
	-	-	PWR	GND	19	20	STEP#	OC	/48	-	
	-	-	PWR	GND	21	22	WDATA#	OC	/48	-	
	-	-	PWR	GND	23	24	WGATE#	OC	/48	-	
	-	-	PWR	GND	25	26	TRK0#	IS	-	330R	
	-	-	PWR	GND	27	28	WPT#	IS	-	330R	
	-	-	-	NC	29	30	RDATA#	IS	-	330R	
	-	-	PWR	GND	31	32	SIDE1#	OC	/48	-	
	-	-	-	NC	33	34	DSKCHG#	IS	-	330R	

Signal Description:

RDATA#	Read Disk Data, active low, serial data input from the floppy disk drive.
WDATA#	Write Disk Data, active low, serial data output to the floppy disk drive.
WGATE#	This output signal enables the head of the selected disk drive to write to the disk.
MOTEA#	This output signal enables the motor in floppy disk drive A.
DRVA#	Active low output signal to select floppy disk drive A.
SIDE1#	This output signal selects side of the disk in the selected drive.
DIR#	This signal controls the direction of the floppy disk drive head movement during a seek operation. A low level request steps through centre.
STEP#	This output signal supplies step pulses to move the head during seek operations.
DENSEL0#	This output indicates whether a low data rate (250/300kbps at low level) or a high data rate (500/1000kbps at high level) has been selected.
TRK0#	Floppy Disk Track 0, active low input to indicate that the head of the selected drive is at track 0.
INDEX#	Floppy Disk Index, active low input indicates the beginning of a disk track.
WPT#	Active low input signal indicating that the selected drive contains a write protected disk.
DSKCHG#	Input pin that senses whether the drive door has been opened or the diskette has been changed.



4.11 Serial Ports

Two RS232 serial ports are available on the KT690/mITX boards

The typical interpretation of the signals in the COM ports is as follows:

Signal	Description
TxD	Transmitte Data, sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Receive Data, receives serial data from the communication link.
DTR	Data Terminal Ready, indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send, indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a telephone-ringing signal.

The connector pinout for each operation mode is defined in the following sections.

4.11.1 Com1 Pin Header Connector.

The pinout of Serial ports Com1 is as follows:

Note	Pull U/D	loh/lol	Туре	Signal	Р	IN	Signal	Туре	loh/lol	Pull U/D	Note
		-	1	DCD	1	2	DSR	ı	-		
		-	I	RxD	3	4	RTS	0		-	
	-		0	TxD	5	6	CTS	ı	-		
	-		0	DTR	7	8	RI	Ī	-		
	-	-	PWR	GND	9	10	5V	PWR	-	-	1

Note 1: The Com1 header 5V supply is fused with a 1.1A resetable fuse.

A DB9 adapter (ribbon cable) can be used to make a DB9 pinout available.

4.11.2 Com2 Pin Header Connector.

The pinout of Serial ports Com2 is as follows:

Note	Pull U/D	loh/lol	Туре	Signal	Р	IN	Signal	Туре	loh/lol	Pull U/D	Note
		-	- 1	DCD	1	2	DSR	1	-		
		-	- 1	RxD	3	4	RTS	0		-	
	-		0	TxD	5	6	CTS	- 1	-		
	-		0	DTR	7	8	RI	- 1	-		
·	-	-	PWR	GND	9	10	5V	PWR	-	-	1

Note 1: The Com2 header 5V supply is fused with a 1.1A resetable fuse.

A DB9 adapter (ribbon cable) can be used to make a DB9 pinout available.

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4.12 Ethernet connectors.

The KT690/mITX boards supports 2 channels of 10/100/1000Mb Ethernet RTL8111B LAN controllers.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB and Category 5E, 6 or 6E with 1Gb LAN networks.

The signals for the Ethernet ports are as follows:

Signal	Description
MDI[0]+	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit
MDI[0]-	pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[1]+	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the
MDI[1]-	receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[2]+	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair.
MDI[2]-	In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDI[3]+	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair.
MDI[3]-	In MDI crossover mode, this pair acts as the BI_DC+/- pair.

Note: MDI = Media Dependent Interface.

4.12.1 Ethernet connectors (ETHER1 and ETHER2)

Ethernet connector 1 is mounted together with USB Ports 8 and 9. Ethernet connector 2 is mounted together with USB Ports 4 and 5.

The pinout of the RJ45 connector is as follows:

Signal				Р	IN				Type	loh/lol	Note
MDI0+											
MDI0-							_				
MDI1+						_					
MDI2+					_						
MDI2-											
MDI1-			_								
MDI3+		_									
MDI3-											
	8	7	6	5	4	3	2	1			



4.13 USB Connector (USB)

The KT690 boards contains one Enhanced Host Controller Interface (EHCI) host controllers that supports USB 2.0 allowing data transfers up to 480Mb/s. The KT690 boards also contains five Open Host Controller Interface (OHCI) controllers that support USB full-speed and low-speed signaling (USB 1.1). The KT690 boards supports a total of ten USB 2.0 ports. All ten ports are high-speed (USB 2.0), full-speed (USB 1.1), and low-speed (USB 1.1) capable and USB Legacy mode is supported.

Over-current detection on all ten USB ports is supported.

USB Port 0 and 2 are supplied on the USB0, USB2 frontpanel connector.

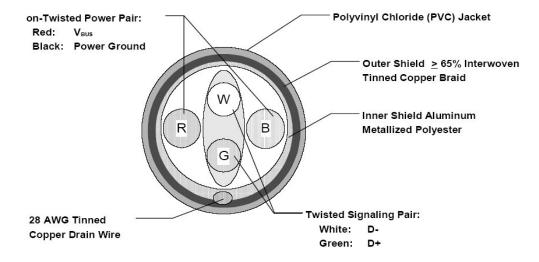
USB Ports 1 and 3 are supplied on the internal FRONTPNL connector; please refer to the FRONTPNL connector section for the pin-out.

USB Port 4 and 5 are supplied on the combined ETHER2, USB4, USB5 connector.

USB Port 6 and 7 are supplied on the internal USB6, USB7 pinrow connector.

USB Port 8 and 9 are supplied on the combined ETHER1, USB8, USB9 connector.

Note: It is recommended to use only High-/Full-Speed USB cable, specified in USB2.0 standard:



4.13.1 USB Connector 0/2 (USB0/2)

USB Ports 0 and 2 are supplied on the USB0, USB2 frontpanel connector.

Note	Pull U/D	loh/lol	Туре	Signal	PIN			Signal	Туре	loh/lol	Pull U/D	Note
					1 2	3 4	4					
1	-	-	PWR	5V/SB5V				GND	PWR	-	-	
	/15K	0.25/2	10	USB2-	_			USB2+	10	0.25/2	/15K	
					1 2	3 4	4					
1	-	-	PWR	5V/SB5V				GND	PWR	-	-	
	/15K	0.25/2	10	USB0-				USB0+	10	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB0+ USB0-	Differential pair works as Data/Address/Command Bus.
USB2+ USB2-	
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

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4.13.2 USB Connector 4/5 (USB4/5)

USB Ports 4 and 5 are are supplied on the combined ETHER2, USB4, USB5 connector.

Note	Pull U/D	loh/lol	Туре	Signal	PIN			Signal	Туре	loh/lol	Pull U/D	Note
					1 2	3	4					
1	-	-	PWR	5V/SB5V				GND	PWR	-	-	
	/15K	0.25/2	10	USB4-				USB4+	Ю	0.25/2	/15K	
					1 2	3	4					
1	-	-	PWR	5V/SB5V				GND	PWR	-	-	
	/15K	0.25/2	Ю	USB5-				USB5+	10	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB4+ USB4-	Differential pair works as Data/Address/Command Bus.
USB5+ USB5-	
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

4.13.3 USB Connector 6/7 (USB6/7)

USB Ports 6 and 7 are are supplied on the internal USB6, USB7 pinrow connector.

Note	Pull U/D	loh/lol	Туре	Signal	Р	IN	Signal	Туре	loh/lol	Pull U/D	Note
1		-	PWR	5V/SB5V	1	2	5V/SB5V	PWR	-		1
		-	10	USB6-	3	4	USB7-	10		-	
	-		10	USB6+	5	6	USB7+	10	-		
	-		PWR	GND	7	8	GND	PWR	-		
	-	-		KEY	9	10	NC		-	-	

Signal	Description
USB6+ USB6-	Differential pair works as Data/Address/Command Bus.
USB7+ USB7-	
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.



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4.13.4 USB Connector 8/9 (USB8/9)

USB Ports 8 and 9 are supplied on the combined ETHER1, USB8, USB9 connector.

Note	Pull U/D	loh/lol	Туре	Signal	PIN		Signal	Туре	loh/lol	Pull U/D	Note
					1 2	3 4					
1	-	-	PWR	5V/SB5V			GND	PWR	-	-	
	/15K	0.25/2	10	USB9-		-	USB9+	Ю	0.25/2	/15K	
					1 2	3 4					
1	-	-	PWR	5V/SB5V			GND	PWR	-	-	
	/15K	0.25/2	10	USB8-			USB8+	10	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB8+ USB8-	Differential pair works as Data/Address/Command Bus.
USB9+ USB9-	
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

4.14 Audio Connector

The onboard Audio circuit implements 7.1+2 Channel High Definition Audio, featuring ten 24-bit stereo DACs and two 20-bit stereo ADCs.

Thew Audio signals are made available on the Frontpanel stacked connector (Line in / Line out / MIC) and the onboard AUDIO_HEAD and CDROM Audioinput connectors.

4.14.1 Audio Line-in, Line-out and Microphone

Audio Line-in, Line-out and Microphone are available in the stacked audio jack connector.

IN	Signal	Type	Note
TIP	LINE1-IN-L	IA	1
RING	LINE1-IN-R	IA	1
SLEEVE	GND	PWR	
			_
TIP	FRONT-OUT-L	OA	
RING	FRONT-OUT-R	OA	
SLEEVE	GND	PWR	
TIP	MIC1-L	IA	1
RING	MIC1-R	IA	1
SLEEVE	GND	PWR	

Note 1: Signals are shorted to GND internally in the connector, when jack-plug not inserted.

4.14.2 CD-ROM Audio input (CDROM)

CD-ROM audio input may be connected to this connector. It may also be used as a secondary line-in signal.

PIN	Signal	Type	loh/lol	Pull U/D	Note
1	CD_Left	IA	-	-	1
2	CD_GND	IA	-	-	
3	CD_GND	IA	-	-	
4	CD_Right	IA	-	•	1

Note 1: The definition of which pins are use for the Left and Right channels is not a worldwide accepted standard. Some CDROM cable kits expect reverse pin order.

Signal	Description
CD_Left CD_Right	Left and right CD audio input lines or secondary Line-in.
CD_GND	Analogue GND for Left and Right CD. (This analogue GND is not shorted to the general digital GND on the board).



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4.14.3 AUDIO Header (AUDIO_HEAD)

Note	Pull U/D	loh/ lol	Туре	Signal	PIN		Signal	Туре	loh/ lol	Pull U/D	Note
	t.			LFE-OUT	1	2	CEN-OUT		Ξ.		
				AAGND	3	4	AAGND				
				FRONT-OUT-L	5	6	FRONT-OUT-R				
				AAGND	7	8	AAGND				
				REAR-OUT-L	9	10	REAR-OUT-R				
				SIDE-OUT-L	11	12	SIDE-OUT-R				
				AAGND	13	14	AAGND				
				MIC1-L	15	16	MIC1-R				
				AAGND	17	18	AAGND				
				LINE1-IN-L	19	20	LINE1-IN-R				
				NC	21	22	AAGND				
	-	-	PWR	GND	23	24	SPDIF-IN				
				SPDIF-OUT	25	26	GND	PWR	-	-	

Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
REAR-OUT-L	Rear Speakers (Surround Out Left).	
REAR-OUT-R	Rear Speakers (Surround Out Right).	
SIDE-OUT-L	Side speakers (Surround Out Left)	
SIDE-OUT-R	Side speakers (Surround Out Right)	
CEN-OUT	Center Speaker (Center Out channel).	
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).	
NC	No connection	
MIC1	MIC Input 1	
LINE1-IN	Line in 1 signals	
F-SPDIF-IN	S/PDIF Input	
F-SPDIF-OUT	S/PDIF Output	
AAGND	Audio Analogue ground	



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4.15 Fan connectors, FAN_CPU and FAN_SYS.

The **FAN_CPU** is used for connection of the active cooler for the CPU.

The FAN_SYS can be used to power, control and monitor a fan for chassis ventilation etc.

The 4pin header supports connection of 3-pin FANs, but it is recommended to use the 4-pin type for optimized FAN speed control. The 3- or 4-pin mode is controlled in the BIOS setup menu.

4-pin Mode:

PIN	Signal	Туре	loh/lol	Pull U/D	Note
1	CONTROL	0		-	
2	SENSE		-	-	
3	+12 V	PWR		-	
4	GND	PWR	-	-	

Signal description:

Signal	Description
CONTROL	PWM signal for FAN speed control
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. On board is a pull-up resistor 4K7 to +12V. The signal has to be pulses, typically 2 Hz per rotation.
12V	+12V supply for fan. A maximum of 2000 mA can be supplied from this pin.
GND	Power Supply GND signal

3-pin Mode:

PIN	Signal	Туре	loh/lol	Pull U/D	Note
2	SENSE	I	-	-	
3	+12 V	PWR	-	-	
4	GND	PWR	-	-	

Signal description:

Signal	Description
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. On board is a pull-up resistor 4K7 to +12V. The signal has to be pulses, typically 2 Hz per rotation.
12V	+12V supply for fan, can be turned on/off or modulated (PWM) by the chipset. A maximum of 2000 mA can be supplied from this pin.
GND	Power Supply GND signal

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4.16 The Clear CMOS Jumper, CIr-CMOS.

The Clr-CMOS Jumper is used to clear the CMOS content.

	CPU location ↑
No Jumper installed	1 2 3 (Pin numbers)
Jumper normal position	•
Jumper in Clear CMOS position	•

To clear all CMOS settings, including Password protection, move the CMOS_CLR jumper (with or without power on the system) for approximately 1 minute.

Alternatively if no jumper is available, turn off power and remove the battery for 1 minute, but be careful to orientate the battery corretly when reinserted.

4.17 **TPM connector (unsupported).**

Note	Pull U/D	loh/lol	Туре	Signal	P	IN	Signal	Туре	loh/lol	Pull U/D	Note
	-	-	PWR	LPC CLK	1	2	GND				
	-	-	PWR	LPC FRAME#	3		KEY				
				LPC RST#	5	6	+5V				
				LPC AD3	7	8	LPC AD2				
				+3V3	9	10	LPC AD1				
				LPC AD0	11	12	GND				
				SMB_CLK	13	14	SMB_DATA				
				SB3V3	15	16	LPC SERIRQ				
				GND	17	18	CLKRUN#				
				SUS_STAT#	19	20	LPC IRQ#				

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4.18 Front Panel connector (FRONTPNL).

Note	Pull U/D	loh/lol	Туре	Signal	Pl	IN	Signal	Туре	loh/lol	Pull U/D	Note
				USB13_5V	1	2	USB13_5V				
				USB1-	3	4	USB3-				
				USB1+	5	6	USB3+				
	-	-	PWR	GND	7	8	GND	PWR	-	-	
	-	-	-	KEY		10	LINE2-IN-L	-	-	-	
	-	-	PWR	+5V	11	12	+5V	PWR	-	-	
			OC	HD_LED	13	14	SUS_LED				
	-	-	PWR	GND	15	16	PWRBTN_IN#				
				RSTIN#	17	18	GND	PWR	-	-	
				SB3V3	19	20	LINE2-IN-R	-	-	-	
				AGND	21	22	AGND				
1				MIC2-L	23	24	MIC2-R				1

Note 1: Unsupported inputs, leave these inputs unconnected.

Signal	Description
USB13_5V	+5V supply for the USB devices on USB Port 1 and 3 is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity.
USB1+ USB1-	Universal Serial Bus Port 1 Differentials: Bus Data/Address/Command Bus.
USB3+ USB3-	Universal Serial Bus Port 3 Differentials: Bus Data/Address/Command Bus.
+5V	Maximum load is 1A or 2A per pin if using IDC connectorfladkabel or crimp terminals respectively.
HD_LED	Hard Disk Activity LED (active low signal). Output is via 475Ω to OC.
SUS_LED	Suspend Mode LED (active high signal). Output is via 475Ω.
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX / BTX PSU and boot the board.
RSTIN#	Reset Input. When pulled low for minimum 16mS the reset process will be initiated. The reset process continues even though the Reset Input is kept low.
LINE2-IN	Line in 2 signals
MIC2	MIC2-L and MIC2-R are unsupported. Leave these terminals unconnected.
SB3V3	Standby 3.3V voltage
AGND	Analogue Ground for Audio



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4.19 Feature Connector (FEATURE)

kontron

Note	Pull U/D	loh/lol	Туре	Signal	P	IN	Signal	Туре	loh/lol	Pull U/D	Note
2	2M/	-	- 1	INTRUDER#	1	2	GND	PWR	-	-	
4			I	EXT_ISAIRQ#	3	4	EXT_SMI#	I			4
				PWR_OK	5	6	SB5V	PWR	-	-	
	-	-	PWR	SB3V3	7	8	EXT_BAT	PWR	-	-	
	-	-	PWR	+5V	9	10	GND	PWR	-	-	
1	4K7/	/12mA	IOT	GPIO0	11	12	GPIO1	IOT	/12mA	2K7/	1
1	4K7/	/12mA	IOT	GPIO2	13	14	GPIO3	IOT	/12mA	2K7/	1
1	4K7/	/12mA	IOT	GPIO4	15	16	GPIO5	IOT	/12mA	2K7/	3
3	4K7/	/12mA	IOT	GPIO6	17	18	GPIO7	IOT	/12mA	2K7/	3
	-	-	PWR	GND	19	20	FAN3OUT				
				FAN3IN	21	22	+12V	PWR	-	-	
				TEMP3IN	23	24	VREF				
	-	-	PWR	GND	25	26	IRRX				
				IRTX	27	28	GND	PWR	-	-	
1	2K7/			SMBC	29	30	SMBD			2K7/	1

Note 1: Pull-up to +3V3Dual (+3V3 or SB3V3). Note 2: Pull-up to RTC-Voltage. Note 3: Pull-up to +3V3. Note 4: NOT supported.

Signal	Description
INTRUDER#	INTRUDER, may be used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the Intruder switch is not needed.
EXT_ISAIRQ#	EXTernal ISA IRQ, (active low input) can activate standard AT-Bus IRQ-interrupt.
EXT_SMI#	External SMI, (active low input) signal can activate SMI interrupt.
PWR_OK	PoWeR OK, signal is high if no power failures is detected.
SB5V	StandBy +5V supply.
SB3V3	Max. load is 0.75A (1.5A < 1 sec.)
EXT_BAT	(EXTernal BATtery) the + terminal of an external primary cell battery can be connected to this pin. The – terminal of the battery shall be connected to GND (etc. pin 10). The external battery is protected against charging and can be used with or without the on board battery installed. The external battery voltage shall be in the range: 2.5 - 4.0 V DC. Current draw is 3μA when PSU is disconnected.
+5V	Max. load is 0.75A (1.5A < 1 sec.)
GPI007	General Purpose Input/Output. The GPIO's may be controlled or monitored through the use of the KT-API-V2 (Application Programming Interface).
FAN3OUT	FAN 3 speed control OUTput. This analogue voltage output signal can be set to output voltages from 0 – 3V3 to control the Fan's speed For more information please look into the datasheet for the Winbond I/O controller W83627.
FAN3IN	FAN3 Input. 0V to +3V3 amplitude Fan 3 tachometer input.
+12V	Max. load is 0.75A (1.5A < 1 sec.)
TEMP3IN	Temperature sensor 3 input. (Recommended: Transistor 2N3904, having emitter connected to GND (pin 25), collector and basis shorted and connected to pin23 (Temp3-In). Further a resistor 30K/1% shall be connected between pin 23 and pin 24 (Vref). (Precision +/- 3°C)
VREF	Voltage REFerence, reference voltage to be used with TEMP3IN input.
IRRX	IR Receive input (IrDA 1.0, SIR up to 1.152K bps)
IRTX	IR Transmit output (IrDA 1.0, SIR up to 1.152K bps)
SMBC	SMBus Clock signal
SMBD	SMBus Data signal



4.20 PCI Slot Connector

			Tern	ninal			
Note	Type	Signal	S	С	Signal	Туре	Note
	PWR	-12V	F01	E01	TRST#	0	
	0	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	0	
		NC	F04	E04	TDI	0	
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	1	
		INTB#	F07	E07	INTC#	l DV/D	
	I	INTD#	F08	E08	+5V NC	PWR	
		NC NC	F09 F10	E09 E10	+5V (I/O)	PWR	
		NC NC	F11	E11	NC	0	
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
		NC	F14	E14	3V3	OT	
	PWR	GND	F15	E15	RST#	0	
	0	PCICLK	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0#	OT	
	I	REQ0#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	PME#	0	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3# AD23	F26 F27	E26 E27	IDSEL +3.3V	PWR	
	PWR	GND	F28	E28	43.3V AD22	IOT	
	IOT	AD21	F29	E29	AD22	IOT	
	IOT	AD19	F30	E30	GND	PWR	
	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	
	IOT PWR	PERR# +3.3V	F40 F41	E40 E41	SMB_CLK SMB_DATA	10 10	
	IOC	SERR#	F41	E41	GND	PWR	
	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
		SOLDER SIDE			COMPONE	NT SIDE	
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	
	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
0K2/ DI I	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	01/0/ DLL
8K2/ PU	IOT PWR	ACK64# +5V	F60 F61	E60 E61	REQ64# +5V	IOT PWR	8K2/PU
	PWR	+5V +5V	F62	E62	+5V +5V	PWR	
	LAAL	⊤JV	F0Z	L0Z	+3∨	LAAL	



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4.20.1 Signal Description –PCI Slot Connector

SYSTEM PIN	IS
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33 MHz.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level—they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS A	ND DATA
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE	CONTROL PINS
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected. (continues)

(continues)



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	ION PINS (BUS MASTERS ONLY) Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every
REQ#	master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every
	master has its own GNT# which must be ignored while RST# is asserted.
	While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain
	a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore
	its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O
	buffer.
ERROR RE	PORTING PINS.
The error re	porting pins are required by all devices and maybe asserted when enabled
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase
	or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the 60signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.
	T PINS (OPTIONAL).
drivers. The attention from pending reconstruction single functions.	n PCI are optional and defined as "level sensitive," asserted low (negative true), using open drain output assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting in its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the puest. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a sion device and up to four interrupt lines for a multi-function device or connector. For a single function device, may be used while the other three interrupt lines have no meaning.
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

4.20.2 KT690 PCI IRQ & INT routing

Board type	Slot	IDSEL	INTA	INTB	INTC	INTD
KT690/mITX	1	AD16	INT_PIRQ#A	INT_PIRQ#B	INT_PIRQ#C	INT_PIRQ#D
KT690/mITX-FW	1	AD16	INT_PIRQ#A	INT_PIRQ#B	INT_PIRQ#C	INT_PIRQ#D
KT690/mITX (BGA)	1	AD16	INT_PIRQ#A	INT_PIRQ#B	INT_PIRQ#C	INT_PIRQ#D

When using the 820982 "PCI Riser - Flex - 2slot w. arbiter" the lower slot has IDSEL / IRQs routed straight through and the top slot has the routing: IDSEL=AD22, INT_PIRQ#F, INT_PIRQ#G, INT_PIRQ#H, INT_PIRQ#E. 820982 PCI Riser shall be plugged into Slot #1.



5. Onboard Connectors

Connector	Onboard	Connectors	Mating Connectors			
Connector	Manufacturer	Type no.	Manufacturer	Type no.		
FAN_SYS,	Molex	22-23-2031	AMP	1375820-3		
FAN_CPU						
KBDMSE	Molex	22-23-2061	Molex	22-01-2065		
CDROM	Foxconn	HF1104E	Molex	50-57-9404		
	Molex	70543-0038				
SATA0-3	Molex	67491-0020	Molex	67489-8005		
			Kontron	KT 821035 (cable kit)		
IEEE1394_0 IEEE1394_1	Foxconn	HC11051-P9	Kontron	KT 821040 (cable kit)		
ATXPWR	Foxconn	HM2510E	Molex	39-01-2205		
COM1 + COM2	Foxconn	HL20051	Molex	90635-1103		
			Kontron	KT 821016 (cable kit)		
			Kontron	KT 821017 (cable kit)		
USB6 USB7	Foxconn	HC11051-P9	Kontron	KT 821401 (cable kit)		
PRINTER	Foxconn	HL2213F	Molex	90635-1263		
			Kontron	KT 821031 (cable kit)		
AUDIO_HEAD	Molex	87831-2620	Molex	51110-2651		
			Kontron	KT 821043 (cable kit)		
FRONTPNL	Foxconn	HL20121	Molex	90635-1243		
			Kontron	KT 821042 (cable kit)		
FEATURE	Molex	87831-3020	Molex	51110-3051		
			Kontron	KT 821041 (cable kit)		
LVDS	Don Connex	C44-40BSB1-G	Don Connex	A32-40-C-G-B-1		
			Kontron	KT 821515 (cable kit)		
			Kontron	KT 821155 (cable kit)		



6. System Ressources

6.1 **Memory map**

000A0000 000 000A0000 000 000A0000 000 000C0000 000 000D0000 000 00100000 37F 38000000 DFI E0000000 EFI F0000000 F7F	O9FFF OBFFF OBFFF OFFFF OFFFF FFFFF FFFFF FFFFF FFFFF FFFFF FFFF	655359 131071 131071 131071 65535 65535 131071 938475519 134217727 2818572287 268435455 134217727	System board ATI Radeon X1200 Series PCI bus PCI standart PCI-to-PCI brigde System board PCI bus System board System board System board Motherboard resources PCI bus Motherboard resources ATI Radeon X1200 Series
000A0000 000 000A0000 000 000C0000 000 000D0000 000 000E0000 000 00100000 37F 38000000 DFI E0000000 EFI F0000000 F7F	DBFFFF DBFFFF DCFFFF DFFFFF DFFFFF FFFFFF FFFFFF FFFFFF FFFFFF	131071 131071 65535 65535 131071 938475519 134217727 2818572287 268435455 134217727	PCI bus PCI standart PCI-to-PCI brigde System board PCI bus System board System board Motherboard resources PCI bus Motherboard resources
000A0000 000 000C0000 000 000D0000 000 000E0000 000 00100000 37F 38000000 3FF 38000000 DFI E0000000 F7F	OBFFF OCFFF ODFFFF OFFFF FFFFF FFFFF FFFFF FFFFF FFFFF	131071 65535 65535 131071 938475519 134217727 2818572287 268435455 134217727	PCI standart PCI-to-PCI brigde System board PCI bus System board System board Motherboard resources PCI bus Motherboard resources
000C0000 000 000D0000 000 000E0000 000 00100000 37F 38000000 3FF 38000000 DFI E0000000 F7F	OCFFFF ODFFFF OFFFFF FFFFFF FFFFFF FFFFFF FFFFFF FFFFFF	65535 65535 131071 938475519 134217727 2818572287 268435455 134217727	System board PCI bus System board System board Motherboard resources PCI bus Motherboard resources
000D0000 000 000E0000 000 00100000 37F 38000000 3FF 38000000 DFF E0000000 FFF F0000000 F7F	DDFFFF DFFFFFF FFFFFF FFFFFF FFFFFF FFFFFF	65535 131071 938475519 134217727 2818572287 268435455 134217727	PCI bus System board System board Motherboard resources PCI bus Motherboard resources
000E0000 000 00100000 37F 38000000 3FF 38000000 DFI E0000000 EFF F00000000 F7F	OFFFF FFFFF FFFFF FFFFF FFFFF FFFFF	131071 938475519 134217727 2818572287 268435455 134217727	System board System board Motherboard resources PCI bus Motherboard resources
00100000 37F 38000000 3FF 38000000 DFI E0000000 EFF F0000000 F7F	FFFFFF FFFFFF FFFFFF FFFFFF	938475519 134217727 2818572287 268435455 134217727	System board Motherboard resources PCI bus Motherboard resources
38000000 3FF 38000000 DFI E0000000 EFF F0000000 F7F	FFFFFF FFFFFF FFFFFF FFFFFF	134217727 2818572287 268435455 134217727	Motherboard resources PCI bus Motherboard resources
38000000 DFI E0000000 EFI F0000000 F7F	FFFFFF FFFFFF FFFFFF	2818572287 268435455 134217727	PCI bus Motherboard resources
E0000000 EFF F0000000 F7F	FFFFFF FFFFFF	268435455 134217727	Motherboard resources
F0000000 F7F	FFFFFF FFFFFF	134217727	
	FFFFFF		ATI Radeon X1200 Series
F0000000 F7F		404047707	7.11 1.445011 7.1200 001100
	D44FFF	134217727	PCI standart PCI-to-PCI brigde
F0000000 FEI		248795135	PCI bus
FE7F4000 FE7	7F7FFF	16383	Microsoft UAA Bus Driver for High Definition Audio
FE7FA000 FE7	7FAFFF	4095	Standard OpenHCD USB Host Controller
FE7FB000 FE7	7FBFFF	4095	Standard OpenHCD USB Host Controller
FE7FC000 FE7	7FCFFF	4095	Standard OpenHCD USB Host Controller
FE7FD000 FE7	7FDFFF	4095	Standard OpenHCD USB Host Controller
FE7FE000 FE7	7FEFFF	4095	Standard OpenHCD USB Host Controller
FE7FF000 FE7	7FFFFF	4095	Standard Enchanced PCI to USB Host Controller
FE7FF800 FE7	7FFBFF	1023	Standart Dual Channel PCI IDE Controller
FE800000 FE8	8FFFFF	1048575	ATI Radeon X1200 Series
FE800000 FE9	9FFFFF	2097151	PCI standart PCI-to-PCI brigde
FE9F0000 FE9	9FFFFF	65535	ATI Radeon X1200 Series
FEA00000 FEA	AFFFFF	1048575	PCI standart PCI-to-PCI brigde
FEAFF000 FEA	AFFFFF	4095	Realtek RTL8168/8111 PCI-E Gigabit Ethernet NIC
FEB00000 FEE	BFFFFF	1048575	PCI standart PCI-to-PCI brigde
FEBFF000 FEE	BFFFFF	4095	Realtek RTL8168/8111 PCI-E Gigabit Ethernet NIC
FEC00000 FE	C00FFF	4095	Motherboard resources
FED00000 FEI	D003FF	1023	High precision event timer
FED45000 FFF	FFFFFF	19640319	System board
FEE00000 FE	E00FFF	4095	Motherboard resources
FFB80000 FFE	BFFFFF	524287	Motherboard resources

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6.2 PCI devices

Bus #	Device #	Function #	Vendor ID	Device ID	IDSEL	Chip	Device Function
0	0	0	1002h	7910h		SB600	Host brigde
0	1	0	1002h	7912h		SB600	Pci to Pci Brigde
0	6	0	1002h	7916h		SB600	Pci to Pci Brigde
0	7	0	1002h	7917h		SB600	Pci to Pci Brigde
0	18	0	1002h	4380h		SB600	IDE Controller
0	19	0	1002h	4387h		SB600	USB
0	19	1	1002h	4388h		SB600	USB
0	19	2	1002h	4389h		SB600	USB
0	19	3	1002h	438Ah		SB600	USB
0	19	4	1002h	438Bh		SB600	USB
0	19	5	1002h	4386h		SB600	USB
0	20	0	1002h	4385h		SB600	SMBus
0	20	1	1002h	438Ch		SB600	IDE Controller
0	20	2	1002h	4383h		SB600	HD Audio
0	20	3	1002h	438Dh		SB600	ISA Brigde
0	20	4	1002h	4384h		SB600	Pci to Pci Brigde
0	24	0	1002h	1100h		SB600	Host brigde
0	24	1	1022h	1101h		SB600	Host brigde
0	24	2	1022h	1102h		SB600	Host brigde
0	24	3	1022h	1103h		SB600	Host brigde
1	5	0	1022h	791Fh		RS690	VGA Controller
2	0	0	10ECh	8168h		RTL8111	Ethernet
3	0	0	10ECh	8168h		RTL8111	Ethernet
4	0	0	-	-		-	PCI Slot
*	-	-	-	-		-	PCI-E Slot

When a PCI-E card is used it could change the BUS number on other PCI-E and PCI devices like RTL8111b.

Note: PCI slot supports PCI BUS Mastering.



6.3 Interrupt Usage

IRQ0	IRQ	Onboard system parity errors and IOCHCHK signal activation	Onboard Timer 0 Interrupt	Onboard Keyboard Interrupt	Used for Cascading IRQ8-IRQ15	May be used by onboard Serial Port A	May be used by onboard Serial Port B / IrDA Port	May be used by onboard Parallel Port	Used by onboard Real Time Clock Alarm	May be used by onboard P/S 2 support	Used for Onboard co-processor support	May be used for SATA RAID controller	May be used for onboard Sound System	May be used for PCI Express Root Port	May be used by onboard USB controller	May be used by onboard Ethernet controller 1	May be used by onboard Ethernet controller 2	May be used by onboard VGA Controller	May be used by onboard IDE Controller	May be used by Microsoft ACPI-Compliant System	Available on PCI slots as IRQA-IRQD depending on selections in BIOS	Notes
IRQ1	NMI	•										?										
IRQ2			•																			
IRQ3				•																		
IRQ4					•																	
IRQ5							•															
IRQ6						•																
IRQ7																					•	1, 2
IRQ8																						1, 2
IRQ9								•													•	1, 2
IRQ10									•													
IRQ12																				•	•	1, 2
IRQ12																					•	1, 2
IRQ13 IRQ14 IRQ15 IRQ16 IRQ17 IRQ18 IRQ19 IRQ20 IRQ20 IRQ21 IRQ22 IRQ23 IRQ23 IRQ24 IRQ25 IRQ25 IRQ25 IRQ25 IRQ25 IRQ25 IRQ26 IRQ27 IRQ28 IRQ29	IRQ11																				•	
IRQ14	IRQ12									•												1
IRQ15 IRQ16 IRQ16 IRQ17 IRQ18 IRQ19 IRQ20 IRQ20 IRQ21 IRQ22 IRQ22 IRQ23 IRQ24 IRQ25 IRQ25 IRQ25 IRQ25 IRQ25 IRQ25 IRQ26 IRQ27 IRQ28 IRQ28 IRQ29											•											
IRQ16								ļ														
IRQ17 IRQ18 IRQ19 IRQ20 IRQ20 IRQ21 IRQ22 IRQ22 IRQ23 IRQ24 IRQ25 IRQ25 IRQ25 IRQ25 IRQ25 IRQ26 IRQ27 IRQ28 IRQ29																						
IRQ18 IRQ19 IRQ20 IRQ21 IRQ22 IRQ22 IRQ23 IRQ24 IRQ25 IRQ25 IRQ25 IRQ25 IRQ25 IRQ26 IRQ27 IRQ28 IRQ29													•									
IRQ19																		<u> </u>				
IRQ20 3 3 IRQ21 5 3 3 IRQ22 5 5 3 3 IRQ24 5 3 3 IRQ25 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5																•	_	•				
IRQ21															•		<u> </u>					
IRQ22 • 3 3 IRQ24 • 3 3 IRQ25 • 3 3 3																						
IRQ23 3 3 IRQ24 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3																			_			
IRQ24 3 IRQ25 3																			<u> </u>			
IRQ25 3																						
	IRQ25 IRQ26																					3

Notes:

- 1. Availability of the shaded IRQs depends on the setting in the BIOS. According to the PCI Standard, PCI Interrupts IRQA-IRQD can be shared.
- 2. These IRQ's are managed by the PnP handler and are subject to change during system initialisation.
- 3. IRQ16 to IRQ26 are APIC interrupts



6.4 **I/O Map**

Addres	s (hex)	Size	Description			
0020	0021	2	Programmable interupt controller			
0040	0043	4	System timer			
0060	0060	1	Standard Keyboard			
0061	0061	1	System speaker			
0064	0064	1	Standard Keyboard			
0070	0071	2	System CMOS/Real time clock			
00F0	00FF	16	Numeric data processor			
0170	0177	8	Secondary IDE Channel			
01F0	01F7	8	Primary IDE Channel			
0274	0277	4	ISAPNP Read Data Port			
0279	0279	1	ISAPNP Read Data Port			
02F8	02FF	8	Com2			
0376	0376	1	Secondary IDE Channel			
0378	037F	8	LPT1			
03B0	03BB	12	PCI-to-PCI brigde			
03C0	03DF	32	PCI-to-PCI brigde			
03F6	03F6	1	Primary IDE Channel			
0A79	0A79	1	ISAPNP Read Data Port			
0B00	0B0F	16	ATI SMBus			
7000	700F	16	Standart Dual Channel PCI IDE Controller			
8000	8003	4	Standart Dual Channel PCI IDE Controller			
9000	9007	8	Standart Dual Channel PCI IDE Controller			
A000	A003	4	Standart Dual Channel PCI IDE Controller			
B000	B007	8	Standart Dual Channel PCI IDE Controller			
C000	CFFF	4096	PCI-to-PCI brigde			
C000	C0FF	256	ATI Radeon X1200 Series			
D000	DFFF	4096	PCI-to-PCI brigde			
D800	D8FF	256	Realtek RTL8168/8111 PCI-E Gigabit Ethernet NIC			
E000	EFFF	4096	PCI-to-PCI brigde			
E800	E8FF	256	Realtek RTL8168/8111 PCI-E Gigabit Ethernet NIC 2			
FF00	FF0F	16	Standart Dual Channel PCI IDE Controller			

Notes: This is the IO map after a standard Windows XP SP2 installation

6.5 **DMA Channel Usage**

DMA Channel Number	Data Width	System Ressources
0	8 or 16 bits	Available
1	8 or 16 bits	Available
2	8 or 16 bits	Available
3	8 or 16 bits	Available
4	8 or 16 bits	DMA Controller
5	16 bits	Available
6	16 bits	Available
7	16 bits	Available



7. Overview of BIOS features

This Manual section details specific BIOS features for the KT690 boards. The KT690 boards are based on the AMI BIOS core version 8.10 with Kontron BIOS extensions.

7.1 System Management BIOS (SMBIOS / DMI)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components.

The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS.

The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

7.2 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

- 1. When you apply power to the computer, legacy support is disabled.
- 2. POST begins.
- 3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
- 4. POST completes.
- 5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
- After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.



8. BIOS Configuration / Setup

8.1 Introduction

The BIOS Setup is used to view and configure BIOS settings for the KT690 board. KT690/mITX (BGA) is supported by BIOS version from KT690013. The BIOS Setup is accessed by pressing the DEL key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The Menu bar look like this:

		BIOS	SETUP U	FILITY			
Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit	

The available keys for the Menu screens are:

Select Menu: $<\leftarrow>$ or $<\rightarrow>$ Select Item: $<\uparrow>$ or $<\downarrow>$ Select Field: <Tab> Change Field: <+> or <->

Help: <F1>

Save and Exit: <F10> Exits the Menu: <Esc>

Please note that in the following the different BIOS Features will be described as having some options. These options will be selected automatically when loading either Failsafe Defaults or Optimal Defaults. The Default options will be indicated by the option in bold, but please notice that when Failsafe Defaults are loaded a few of the options, marked with "*", are now the default option.

8.2 Main Menu

	В	IOS SETUP U	TILITY					
Main Ad	vanced PCIPr	nP Boot	Security	Chipset Exit				
System Overview AMIBIOS Version : 08.0				Use [ENTER], [TAB] or [SHIFT-TAB] to select a field.				
Build Date: 07/3 ID : KT69 PCB ID : 82 Serial # : 0061 Part # : 6162	90013			Use [+] or [-] to configure system Time.				
Processor AMD Turion(tm) 6 Speed : 1600 Count : 2		echnology TL	-52	<- Select Screen Select Item +- Change Field Tab Select Field				
System Memory Size : 896N	MB			F1 General Help F10 Save and Exit				
System Time System Date		=		ESC Exit				
V02.59	V02.59+ (C)Copyright 1985-2005, American Megatrends, Inc.							

Main Menu Selections

You can make the following selections. Use the sub menus for other selections.

Feature	Options	Description
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.



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8.3 Advanced Menu

			BIOS	SETUP UT	TILITY			
	Main	Advanced	PCIPnP	Boot	Security	Chips	et	Exit
	Advanced Set	ttings				Confi	gure (CPU.
	_	tting wrong wrong wrong wrong wrong the contract of the contra			ctions			
>	CPU Configu	ration						
>	IDE Configu	ration						
>	LAN Configu	ration						
>	Floppy Conf:	iguration						
>	SuperIO Cont	figuration						
>	Hardware Hea	alth Configu	ration					
>	Voltage Mon:	itor				<-	Selec	ct Screen
>	ACPI Configu	uration					Selec	t Item
>	Remote Acces	ss Configurat	cion			Enter		Sub Screen
>	Trusted Comp	puting				F1		al Help
>	USB Configu	ration				F10		and Exit
>	Clock Genera	ator Settings	5			ESC	Exit	
	V0	2.59+ (C)Cop	yright 198	5-2005,	American Meg	atrends	, Inc.	

8.3.1 Advanced settings – CPU Configuration

В	IOS SETUP UTILITY	
Advanced		
CPU Configure Module Version -13.14 AGESA Version: 02.08.13 Physical Count: 1 Logical Count: 2		Enable/Disable Secure Virtual Mode (SVM)
AMD Turion(tm) 64 X2 Mobile Te Revision: F2 Cache L1 : 256 KB Cache L2 : 1024 KB Speed : 1600MHz Current FSB Multiplier: 8x uCode Patch Level : 0x62 Able to Change Freq. : Yes Maximum FSB Multiplier: 8x	echnology TL-52	<- Select Screen
Secure Virtual Machine Mode Runtime Legacy PSB C1E Support	[Enabled] [Disabled] [Disabled]	+- Change Option F1 General Help F10 Save and Exit ESC Exit
V02.59+ (C)Copyright	1985-2005, American Mega	atrends, Inc.

Feature	Options	Description
Secure Virtual Machine Mode	Enabled Disabled	Enable/Disable Secure Virtual Mode (SVM)
Runtime Legacy PSB	Enabled Disabled	Enable/disable the generation of Power State block for use of PowerNow™ driver in single core system
C1E Support	Enabled Disabled	Enable/disable C1E support.

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8.3.2 Advanced settings – IDE Configuration

В	IOS SETUP UTILITY	
Advanced		
IDE Configuration OnBoard PCI IDE Controller OnChip SATA Type OnChip SATA Channel	[Primary] [Enabled] [Native IDE]	Options Controls the 40Pin PATA connector and CF interface.
Primary IDE Master Secondary IDE Master Third IDE Master Third IDE Slave Fourth IDE Master Fourth IDE Slave	<pre>: [Hard Disk] : [Not Detected] : [Not Detected] : [Not Detected] : [Not Detected] : [Not Detected]</pre>	<- Select Screen Select Item +- change option F1 General Help
Hard Disk Write Protect IDE Detect Time Out (Sec) ATA(PI) 80Pin Cable Detection	[35]	F1 General Help F10 Save and Exit ESC Exit
V02.59+ (C)Copyright	1985-2005, American Mega	trends, Inc.

Feature	Options	Description
OnBoard PCI IDE Controller	Disable Primary	Controls the 40Pin PATA connector and CF interface.

Feature	Options	Description
OnChip SATA Channel	Enabled Disabled	Enabled/Disabled the SATA circuit
OnChip SATA Channel	Native IDE RAID AHCI Legacy IDE	Native IDE RAID (Press <ctrl><f> to enter RAID BIOS menu) AHCI Legacy IDE</f></ctrl>

Feature	Options	Description
Hard Disk Write Protect	Disabled Enabled	Disabled Enhanced
IDE Detect Time Out (Sec)	0 5 10 15 20 25 30 35	Select the time out value for detecting ATA/ATAPI device(s)
ATA(PI) 80Pin Cable Detection	Host & Device Host Device	Select the mechanism for detecting 80Pin ATA(PI) Cable



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Ad	vanced			
Primary IDE	Master			ct the type of
Device	:Hard Disk			ces connected to
Vendor	:ST340014A		the s	system
Size	:40.0GB			
LBA Mode				
Block Mode	:16Sectors			
PIO Mode	: 4			
	:MultiWord DMA-2			
	:Ultra DMA-5			
S.M.A.R.T.	:Supported			
Type		[Auto]		
LBA/Large M	ode	[Auto]	<-	Select Screen
Block (Mult	i-Sector Transfer)	[Auto]	111	Select Item
PIO Mode		[Auto]	+-	Change Option
DMA Mode		[Auto]	F1	General Help
S.M.A.R.T.		[Auto]	F10	Save and Exit
32Bit Data	Transfer	[Disabled]	ESC	Exit

Feature	Options	Description
Туре	Not Installed Auto CDROM ARMD	Select the type of device installed
LBA/Large Mode	Disabled Auto	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, and Sectors.
Block (Multi-Sector Transfer)	Disabled Auto	Select if the device should run in Block mode
PIO Mode	Auto 0 1 2 3 4	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
DMA Mode	Auto SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA2 UDMA3 UDMA4 UDMA5	Selects the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode. Note: To use UDMA Mode 2, 3, 4 and 5 with a device, the harddisk cable used MUST be UDMA66/100 cable (80-conductor cable).
S.M.A.R.T.	Auto Disabled Enabled	Select if the Device should be monitoring itself (Self-Monitoring, Analysis and Reporting Technology System)
32Bit Data Transfer	Disabled Enabled	Select if the Device should be using 32Bit data Transfer

(continues)



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Feature	Options	Description
Hard Disk Write Protect	Disabled Enabled	Enable write protection on HDDs, only works when it is accessed through the BIOS
IDE Detect Time Out (Sec)	0 5 10 15 20 25 30 35	Select the time out value when the BIOS is detecting ATA/ATAPI Devices
ATA(PI) 80Pin Cable Detection	Host & Device Host Device	Select the mechanism for detecting 80Pin ATA (PI) Cable

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8.3.3 Advanced settings – LAN Configuration

BIOS SETUP UTILITY			
Advanced			
LAN Configuration	Control of Ethernet Devices and PXE boot		
ETH1 Configuration (Left) [Enabled] MAC Address : 00E0F4000001 ETH2 Configuration (Right) [Enabled] MAC Address : 00E0F4000002	<pre><- Select Screen Select Item +- change option F1 General Help F10 Save and Exit ESC Exit</pre>		
V02.59+ (C)Copyright 1985-2005, American Mega	V02.59+ (C)Copyright 1985-2005, American Megatrends, Inc.		

Feature	Options	Description
ETH1 Configuration	Disabled Enabled With RPL/PXE boot	Select if you want to enable the LAN adapter, or if you want to activate the RPL/PXE boot rom
ETH2 Configuration	Disabled Enabled With RPL/PXE boot	Select if you want to enable the LAN adapter, or if you want to activate the RPL/PXE boot rom

8.3.4 Advanced settings – Floppy Configuration

BIOS SETUP UTILITY			
Advanced			
Floppy Configuration Floppy A	[Disabled]	Select the type of floppy drive connected to the	
		system.	
		<- Select Screen	
		+- change option	
		F1 General Help F10 Save and Exit ESC Exit	
V02.59+ (C)Cop	V02.59+ (C)Copyright 1985-2005, American Megatrends, Inc.		

Feature	Options	Description
Floppy A	Disabled Enabled	Select the type of floppy drive connected to the system.



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8.3.5 Advanced settings – Super IO Configuration

BIOS SETUP UTILITY		
Advanced		
Configure Win627DHG Super IO Cl OnBoard Floppy Controller Serial Port1 Address Serial Port2 Address Serial Port2 Mode Parallel Port Address Parallel Port IRQ	hipset [Enabled] [3F8/IRQ4] [2F8/IRQ3] [Normal] [378] [Normal] [IRQ7]	Allows BIOS to Enable or Disable Floppy Controller. <- Select Screen Select Item +- change option F1 General Help F10 Save and Exit ESC Exit
V02.59+ (C)Copyright 1985-2005, American Megatrends, Inc.		

Feature	Options	Description
OnBoard Floppy Controller	Enabled Disabled	Allows BIOS to Enable or Disable Floppy Controller.
Serial Port1 Address	Disabled 3F8/IRQ4 3E8/IRQ4 3E8/IRQ6 3E8/IRQ10 2E8/IRQ11	Select the BASE I/O addresse and IRQ. (The available options depends on the setup for the the other Serial Ports).
Serial Port2 Address	Disabled 2F8/IRQ3 2E8/IRQ3 3E8/IRQ6 3E8/IRQ10 2E8/IRQ11	Select the BASE I/O addresse and IRQ. (The available options depends on the setup for the the other Serial Ports).
Serial Port2 Mode	Normal IRDA ASK IR	Select Mode for Serial Port2
Parallel Port Address	Disabled * 378 278 3BC	Select the I/O address for the PRINTER.
Parallel Port Mode	Normal Bi-Directional EPP ECP & EEP	Select the mode that the parallel port will operate in
EPP Version	1.9 1.7	Setup with version of EPP you want to run on the parallel port
ECP Mode DMA Channel	DMA0 DMA1 DMA3	Select a DMA channel
Parallel Port IRQ	IRQ5 IRQ7	Select a IRQ



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8.3.6 Advanced settings – Hardware Health Configuration

	BIOS SETUP UTILITY	
Advanced		
Hardware Health Configuration	n	Disable = Full Speed
System Temperature CPU Temperature External Temperature Sensor	:37°C/98°F :43°C/109°F :N/A	Thermal: Does regulate fan speed according to specified temperature
System Fan Speed Fan Cruise Control Fan Type CPUFanO Speed Fan Cruise Control Fan Setting Fan Type AUXFAN Speed Fan Cruise Control Fan Setting	:Fail [Disabled] [4 Wire] :2537 RPM [Thermal] [45°C/113°F] [4 Wire] :2164 [Speed] [2177 RPM]	Speed: Does regulate according to specified RPM
Watchdog Function	[Disabled]	Select Item +- change option F1 General Help F10 Save and Exit ESC Exit

Feature	Options	Description
Fan Cruise Control	Disabled Thermal Speed	Select how the Fan shall operate. When set to Thermal, the Fan will start to run at the CPU die temperature set below. When set to Speed, the Fan will run at the Fixed speed set below.
Fan Type	4 wire 3 wire	Select the electrical interface for the fan: 3 Wire = PWM output to fan power line. RPM reading and speed regulation at lower speed might be poor. 4 Wire = 12VDC always PWM on control signal
Fan Settings	1406-5625 RPM 30°-75°C	The fan can operate in Thermal mode or in a fixed fan speed mode
Watchdog	Disabled 15 seconds 30 seconds 1 minute 2 minutes 5 minutes 10 minutes	To be serviced via API.



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8.3.7 Advanced settings – Voltage Monitor

	Enable Hardware Health Monitoring Device.
:1.100 V	Monitoring Device.
:1.088 V	
:3.248 V	
:3.248 V	
:12.029 V	
:Good	<- Select Screen
:5.165 V	Select Item
:1.792 V	+- change option
:1.184 V	F1 General Help
:3.264 V	F10 Save and Exit
:3.200 V	ESC Exit
	:1.088 V :3.248 V :3.248 V :12.029 V :Good :5.165 V :1.792 V :1.184 V :3.264 V

8.3.8 Advanced settings – ACPI Configuration

Advanced	
ACPI Settings	General ACPI Configuration setting
>Advanced ACPI Configuration >Chipset ACPI Configuration	<- Select Screen Select Item +- change option F1 General Help F10 Save and Exit ESC Exit

Advanced ACPI Configuration

Feature	Options	Description
ACPI Version Features	ACPI v1.0 ACPI v2.0 ACPI v3.0	Enable RSDP pointers to 64-bit Fixed System Description Tables. Di ACPI version has some.
ACPI APIC support	Disbled Enabled	Include ACPI APIC table pointer to RSDT pointer list.
Suspend mode	S1 (POS) * S3 (STR) Auto	Select the ACPI state used for System Suspend
Repost Video on S3 Resume	No Yes	Determines whether to invoke VGA BIOS post on S3/STR resume

Chipset ACPI Configuration

Feature	Options	Description
HPET in SB	Disabled Enabled	Enable/Disable



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8.3.9 Advanced settings – Remote Access Configuration

BIOS SETUP UTILITY		
Advanced		
Configure Remote Access type	and parameters	Select Remote Access
Remote Access	[Enabled]	type.
Serial port number Base Address, IRQ Serial Port Mode Flow Control Redirection After BIOS POST Terminal Type	[COM1] [3F8h, 4] [115200 8,n,1] [None] [Always] [ANSI]	<pre><- Select Screen Select Item +- change option F1 General Help F10 Save and Exit ESC Exit</pre>
V02.59+ (C)Copyright	1985-2005, American Mega	trends, Inc.

Feature	Options	Description
Remote Access	Disabled Enabled	When Enabled then a remote PC can via one of the serial ports behave like a TTY terminal, so that keyboard and monitor (in a terminal window) is emulated by the remote PC. As remote PC terminal program the Windows Hyperterminal can be used.
Serial port number	COM1 COM2	Setup which comport that should be used for communication
Serial Port Mode	115200 8 n 1 57600 8 n 1 38400 8 n 1 19200 8 n 1 9600 8 n 1	Select the serial port speed
Flow Control	None Hardware Software	Select Flow Control for serial port
Redirection After BIOS POST	Disabled Boot Loader Always	How long shall the BIOS send the picture over the serial port
Terminal Type	ANSI VT100 VT-UTF8	Select the target terminal type
VT.UTF8 Combo Key Support	Enabled Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Sredir Memory Display Delay	No Delay Delay 1 Sec Delay 2 Sec Delay 4 Sec	Gives the delay in seconds to display memory information

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8.3.10 Advanced settings – Trusted Support

	BIOS SETUP UTILITY	
Advanced		
Trusted Computing TCG/TPM Support	[No]	Enables/Disable TPM TCG (Tpm 1.1/1.2) Support in Bios
		<pre><- Select Screen Select Item +- change option F1 General Help F10 Save and Exit ESC Exit</pre>
V02.59+ (C)Cc	opyright 1985-2005, America	n Megatrends, Inc.

Feature	Options	Description
TCG/TPM Support	No Yes	Enables/Disable TPM TCG (TPM 1.1/1.2) Support.

8.3.11 Advanced settings – USB Configuration

Advanced			
USB Configuration		Enables si legacy US	upport for
Module Version - 2.24.2-13	. 4		sables if no
USB Devices Enabled : 1 Drive		connected	
Legacy USB Support USB 2.0 Controller Mode	[Enabled] [HiSpeed]		ect Screen
BIOS EHCI Hand-Off	[Enabled]	+- char	ect Item nge option
USB Mass Storage Device Configuration			eral Help e and Exit

Feature	Options	Description
Legacy USB Support	Disabled Enabled Auto	Support for legacy USB Keyboard
USB 2.0 Controller Mode	FullSpeed HiSpeed	Configure the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps). Note: This feature is not available when Failsafe Defaults are loaded, because USB2.0 controller is disabled as default.
BIOS EHCI Hand-Off	Enabled Disabled	This is a workaround for OSes without EHCI hand-off support. The EHCI Ownership change should claim by EHCI driver.



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8.3.12 Advanced settings – USB Mass Storage Device Configuration

BIOS SETUP UTILITY						
Advanced	Advanced					
USB Mass Storage Device Confi USB Mass Storage Reset Delay Device #1	Number of seconds POST waits for the USB mass storage device after start unit command.					
Emulation Type	[Auto]	<- Select Screen Select Item +- change option F1 General Help F10 Save and Exit ESC Exit				
V02.59+ (C)Copyright 1985-2005, American Megatrends, Inc.						

Feature	Options	Description
USB Mass Storage Reset Delay	10 Sec 20 Sec 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Emulation Type	Auto Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

8.3.13 Advanced settings – Clock Generator Settings

BIOS SETUP UTILITY						
Advanced						
Clock Generator Settings Spread Spectrum	[Disabled]	[Disabled]				
		<- Select Screen Select Item +- change option F1 General Help F10 Save and Exit ESC Exit				
V02.59+ (C)Copyri	V02.59+ (C)Copyright 1985-2005, American Megatrends, Inc.					

Feature	Options	Description
Spread Spectrum	Disabled 0.5%	Controls the clock generator clock output to enable (0.5%) or disable Spread spectrum

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8.4 PCIPnP Menu

BIOS SETUP UTILITY				
PCII				
Advanced PCI/PnP Settin	gs	NO: lets the BIOS		
Warning: Setting wrong values in below sections May cause system to malfunction.		configure all the devices in the system. YES: lets the		
		operating system configure Plug and		
IRQ3 IRQ4 IRQ5 IRQ7 IRQ9 IRQ10	[Available] [Available] [Available] [Available] [Available] [Available]	Play (PnP) devices not required for boot if your system has a Plug and Play operating system.		
IRQ11 IRQ14 IRQ15	[Available] [Available] [Available]	<- Select Screen Select Item +- change option F1 General Help F10 Save and Exit ESC Exit		
V02.59+ (C)Cor	pyright 1985-2005, American M	Megatrends, Inc.		

Feature	Options	Description
Plug & Play O/S	No * Yes	NO: lets the BIOS configure all the devices in the system. YES: lets the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.
IRQ	Available Reserved	Available: Specified IRQ is available to be used by PCI/PnP device. Reserved: Specified IRQ is reserved for use by Legacy ISA device.

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8.5 **Boot Menu**

				BIOS	SETUP UI	LITY			
		Main	Advanced	PCIPnP	Boot	Security	Chips	et	Exit
	Boot	Setting	ıs				-	_	Settings stem Boot.
>	Boot	Setting	s Configurat	cion					
>	Boot	Device	Priority				<- Enter F1 F10 ESC	Sele Go t Gene Save	ect Screen ect Item to Sub Screen eral Help e and Exit
	V02.59+ (C)Copyright 1985-2005, American Megatrends, Inc.								

8.5.1 Boot – Boot Settings Configuration

Boot				
Boot Settings		Configure Settings during System Boot.		
Quick Boot Quiet Boot AddOn ROM Display Mode Bootup Num-Lock PS/2 Mouse Support Wait for 'F1' If Error Hit 'DEL' Message Display Interrupt 19 Capture PC Speaker/Beep Default init boot order Force boot Device	[Enabled] [Disabled] [Force BIOS] [On] [Auto] [Enabled] [Enabled] [Disabled] [Enabled] [O->4->3->5->2->1] [Disabled]	<- Select Screen Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit		



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Feature	Options	Description
Quick Boot	Enabled Disabled	Allows BIOS to skip certain test while booting in order to decrease boot time.
Quiet Boot	Disabled Enabled	Disabled: Displays normal POST messages. Enabled: Displays OEM Logo (no POST messages).
AddOn ROM Display Mode	Force BIOS Keep current	Set display mode for Option ROM.
Bootup Num-Lock	Off On	Select Power-on state for numlock
PS/2 Mouse Support	Disabled Enabled Auto	Select support for PS/2 Mouse.
Wait for 'F1' If Error (see note)	Disabled Enabled	Wait for F1 key to be pressed if error occurs.
Hit 'DEL' Message Display	Disabled Enabled	Displays "Press DEL to run Setup" in POST.
Interrupt 19 Capture	Disabled Enabled	Enabled: Allows option ROMs to trap interrupt 19
PC Speaker/Beep	Disabled Enabled	Control the default beeps during boot of the system. This setting will aldo control the beep during enumeration and (un)plug of USB.
Default init boot order	0->4->3->5->2->1 0->4->3->5->1->2 1->2->3->5->0->4 3->5->1->2->0->4 3->0->4->1->2->5 2->1->0->4->3->5 2->0->4->3->1->5 3->1->0->4->2->5	The numbers in the sequence means: 0 = "Removables" (Floppy, LS100 etc.) 1 = "Hard Disk" 2 = "ATAPI CDROM" 3 = "BEV/onboard LAN" 4 = "USB" (any bootable USB device) 5 = "External LAN" (PCIe/PCI LAN card)
Force boot Device	Disabled Primary IDE Master Primary IDE Slave Third IDE Master Third IDE Slave Fourth IDE Master Fourth IDE Slave Network	Does override current boot setting. Device must be in the boot priority menu though. If the device fails to boot, the system will NOT try other devices.

Note: List of errors: <INS> Pressed Timer Error

Interrupt Controller-1 error Keyboard/Interface Error Halt on Invalid Time/Date

NVRAM Bad

Primary Master Hard Disk Error S.M.A.R.T HDD Error Cache Memory Error DMA Controller Error Resource Conflict Static Resource Conflict PCI I/O conflict
PCI ROM conflict
PCI IRQ conflict
PCI IRQ routing table of

PCI IRQ routing table error



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8.5.2 Boot – Boot Device Priority

BIOS SETUP UTILITY						
Boot						
Boot Device Priority		Specifies the boot sequence from the available devices.				
1st Boot Device	[ESS-ST380811AS]	available devices.				
		A device enclosed in paranthesis has been disabled in the corresponding type menu.				
		<- Select Screen Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit				
V02.59+ (C)Copyrigh	V02.59+ (C)Copyright 1985-2005, American Megatrends, Inc.					

Note: When pressing <F11> while booting it is possible manually to select boot device.

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8.6 Security Menu

		BIOS	SETUP UT	ILITY		
Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit
Security Set	ttings				Install or password.	Change the
-	Password :Ins rd :Ins					
Change Super Change User	rvisor Passwo Password	ord				
Boot Sector	Virus Protec	ction [Disabled]			
Hard Disk Se	ecurity				<- Sele	ct Screen
Primary Sla	ter HDD User ve HDD User F lave HDD User	assword			Enter Go t	
V0	2.59+ (C)Copy	yright 198	5-2005, A	merican Meg	 atrends, Inc	

Feature	Options	Description
Change Supervisor Password	Password	Change the Supervisor Password
Change User Password	Password	Change the User Password
Boot Sector Virus Protection	Enabled Disabled	Will write protect the MBR when the BIOS is used to access the harddrive
HDD Password	Password	Locks the HDD with a password, the user needs to type the password on power on

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8.7 Chipset Menu

	В	IOS SETUP UT	LITY			
Main Adv	anced PCIPr	nP Boot	Security	Chipse	et	Exit
Advanced Chipset	Settings			1	_	North tures.
Warning: Setting may cau	wrong values se system to m		ctions			
North Bridge ConSouth Bridge ConAMD 690G Configu	figuration			F1 F10	Sele Go t Gene	ct Screen ct Item o Sub Screen ral Help and Exit
V02.59+	(C)Copyright	1985-2005,	American Mega	trends	, Inc	•

8.7.1 Advanced Chipset Settings – North Bridge Chipset Configuration

		Chipset
North Bridge Adapter P	riority Configuration	Allow DIMMs to enter
> Power Down Control	[Auto]	power down mode by deasserting the clock enable signal when
Memory CLK CAS Latency(Tcl) RAS/CAS Delay(Trcd) Min Active RAS(Tras) Row Precharge Time(Trp RAS/RAS Delay(Trrd) Row Cycle (Trc)	:5.0 :5 CLK :18 CLK):5 CLK :3 CLK	DIMMs are not in use.
Asynchronous Latency		<pre><- Select Screen Select Item Enter Go to Sub Screer F1 General Help F10 Save and Exit ESC Exit</pre>

Feature	Options	Description
Power Down Control	Auto Disabled	Allow DIMMs to enter power down mode by deasserting the clock enable signal when DIMMs are not in use.



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8.7.2 Advanced Chipset Settings – SouthBridge Configuration

	BIOS SETUP UTILITY				
					Chipset
>		Chipset Configura Configuration	tion		Disabled 2 USB Ports
	USB 1.1 OHCI	Controllers Controller	[Enabled] [Enabled]		4 USB Ports 6 USB Ports 8 USB Ports 10 USB Ports
					<- Select Screen
					Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
	V02	.59+ (C)Copyright	1985-2005,	American Meg	gatrends, Inc.

SB HD Azalia Configuration

Feature	Options	Description		
HD Audio Azalia Device	Disabled Enabled	Enable/Disable complete HD (Azalia) Audio circuit		
Audio Jack sensing	Disabled Enabled	Enable/Disable sensing of audio jack plugs insertion		
Azalia Front Panel	Disabled Enabled	Enable/Disable the "Front Panel Connector" Audio circuit		

Feature	Options	Description
USB 1.1 OHCI Controllers	Disabled Enabled	Disabled Enabled
USB 2.0 Controller	Disabled * Enabled	Disabled Enabled



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8.7.3 Advanced Chipset Settings - AMD 690G Configuration

BIOS SETUP UTILITY		
Chipset		
AMD 690G Configuration	Internal Graphics Configuration	
> Internal Graphics Configuration > Display Configuration	<- Select Screen Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit	
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Internal Graphics Configuration:

Video Display Devices [Auto] <- Select TV Standard [NTSC] Expansion Mode [Disabled] F1 Genera Replace GFX subid [Enabled] F10 Save a		BIOS SETUP UTILITY			
Internal Graphics Mode [UMA] UMA Frame Buffer Size [Auto] Current UMA Size [128MB] Primary Video Controller [PCIE/IGFX/PCI] Video Display Devices [Auto] TV Standard [NTSC] Expansion Mode [Disabled] Replace GFX subid [Enabled] UMA - Select Controller Contro	Chipset				
UMA Frame Buffer Size [Auto] Current UMA Size [128MB] Primary Video Controller [PCIE/IGFX/PCI] Video Display Devices [Auto] TV Standard [NTSC] Expansion Mode [Disabled] Replace GFX subid [Enabled] TO Save a	Internal Graphics Configurat	ion			
Loc Bare	UMA Frame Buffer Size Current UMA Size Primary Video Controller Video Display Devices TV Standard Expansion Mode	[Auto] [128MB] [PCIE/IGFX/PCI] [Auto] [NTSC] [Disabled]	Select Item Enter Go to Sub Scree F1 General Help		

Feature	Options	Description
Internal Graphics Mode	Disabled UMA	Disabled UMA
UMA Frame Buffer Size	Auto 32MB 64MB 128MB 256MB 512MB 1024MB	auto 32MB 64MB 128MB 256MB 512MB 1024MB
Primary Video Controller	PCIE/IGFX/PCI PCI/PCIE/IGFX IGFX/PCIE/PCI	PCIE/IGFX/PCI PCI/PCIE/IGFX IGFX/PCIE/PCI
Video Display Devices	Auto CRT LVDS DVI EDFP TV CRT + LVDS CRT + DVI CRT + EDFP DVI + LVDS DVI + EDFP LVDS + EDFP TV + LVDS TV + DVI TV + EDFP	Auto CRT: onboard analogue VGA output LVDS: onboard LVDS output DVI: onboard DVI output EDFP: External Digital Flat Panel via PCle card TV: onboard TV output (if TV-out version of board)
TV Standard	NTSC PAL PAL-M PAL-60 NTSC-JAP PAL-CN Pal-N Scart_RGB	NTSC PAL PAL-M PAL-60 NTSC-JAP PAL-CN Pal-N Scart_RGB
Expansion Mode	Enabled Disabled	Enabled/Disabled Expansion Mode



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Displays Configuration:

	BIOS SETUP UTILITY	
	Ch	ipset
Displays Configuration	D	isplay module V0.04
LVDS Backlight Signal Inversion LCDVCC Voltage TMDS Support	[None] [Disabled] [3.3V] [Auto]	
	E F F	Select Screen Select Item Select Item Senter Go to Sub Screen General Help Save and Exit SC Exit
V02.59+ (C)Copyrigh	t 1985-2005, American Megatr	ends, Inc.

Feature	Options	Description
LVDS	None	Select Panel setup
Backlight Signal Inversion	Disabled Enabled	Select signal Polarity
LCDVCC Voltage	3.3V 5.0V	LVDVCC voltage selection (power sequenced)
TMDS Support	Disabled Enabled Auto	Disabled Enabled Auto



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8.8 **Power**

		В	IOS SETUP	UTILITY	
Main	Advanced	PCIPnP	Boot	Security	Chipset Power Exit
Power Management/APM Power Button Mode Restore on AC Power Loss RTC Resume PME/WOL Enable PS/2 Kbd/Mouse S4/S5 Wake Keyboard Wake Hotkey		[Enabled] [On/Off] [Power On] [Disabled] [Disabled] [Disabled] [Any key]		Enable/Disable SMI based power management and APM support	
					<- Select Screen Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
	V02.59+ (C)	Copyright	1985-2005	, American	Megatrends, Inc.

Feature	Options	Description
Power Management/APM	Disabled Enabled	Enable/Disable SMI based power management and APM support
Power Button Mode	Disabled Standby Suspend	Disabled Standby Suspend
Restore on AC Power Loss	Power On Power Off Last state	Select whether or not to restart the system after AC power loss (ATX +5VSB signal goes high): Power Off keeps the power off until the power button is pressed. Power On restores power to the computer. Last State use same power state as before power loss occurred.
RTC Resume	Disabled Enabled	RTC to generate a wake event
PME/WOL Enable	Disabled Enabled	Disabled/Enabled PME to power on system with Wake on Lan function
PS/2 kbd/Mouse S4/S5 Wake	Disabled Enabled	Enabled: System can be waked also from S4 or S5. Disabled: PS/2 KBD/MSE can still wake system from S3
Keyboard Wake Hotkey	Any key "SPACE" "ENTER" "Sleep button"	Any key "SPACE" "ENTER" "Sleep button"



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8.9 Exit Menu

			BIOS	SETUP UTI	LITY			
	Main	Advanced	PCIPnP	Boot	Security	Chipse	et :	Exit
Save Disca Disca Load	ard Chang ard Chang Optimal	and Exit ges and Exit ges Defaults e Defaults				after change F10 Ke	savinges. ey can	setup g the be used eration.
	on inva	lid Time/Dat	e	[Enable	-	<- 		t Screen t Item
	170.2	.59+ (C)Copy		2005	wasi san Wasa	F1 F10 ESC	Go to Genera Save a Exit	Sub Screen al Help and Exit

Feature	Options	Description
Save Changes and Exit	Ok Cancel	Exit system setup after saving the changes
Discard Changes and Exit	Ok Cancel	Exit system setup without saving any changes
Discard Changes	Ok Cancel	Discards changes done so far to any of the setup questions
Load Optimal Defaults	Ok Cancel	Load Optimal Default values for all the setup questions
Load Failsafe Defaults	Ok Cancel	Load Failsafe Default values for all the setup questions
Halt on invalid Time/Date	Enabled Disabled	Enabled: System halt if incorrect Date & Time.
Secure CMOS	Enabled Disabled	Enable will store current CMOS in non volatile ram. (For protection of CMOS data in case of battery failure etc.)



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9. AMI BIOS Beep Codes

Boot Block Beep Codes:

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

POST BIOS Beep Codes:

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

Troubleshooting POST BIOS Beep Codes:

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.



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10. OS setup

Use the Setup.exe files for all relevant drivers. The drivers can be found on KT690 Driver CD or they can be downloaded from the homepage www.kontron.com

Note: P.T. on the web you will now find latest Video XP driver (version 9.11) for the KT690. On ATI homepage you will find newer drivers, but they do not support KT690.



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11. Warranty

KONTRON Technology warrants its products to be free from defects in material and workmanship during the warranty period. If a product proves to be defective in material or workmanship during the warranty period, KONTRON Technology will, at its sole option, repair or replace the product with a similar product. Replacement Product or parts may include remanufactured or refurbished parts or components.

The warranty does not cover:

- 1. Damage, deterioration or malfunction resulting from:
 - 1.1. Accident, misuse, neglect, fire, water, lightning, or other acts of nature, unauthorized product modification, or failure to follow instructions supplied with the product.
 - 1.2. Repair or attempted repair by anyone not authorized by KONTRON Technology.
 - 1.3. Causes external to the product, such as electric power fluctuations or failure.
 - 1.4. Normal wear and tear.
 - 1.5. Any other causes which does not relate to a product defect.
- 2. Removal, installation, and set-up service charges.

Exclusion of damages:

KONTRON TECHNOLOGY LIABILITY IS LIMITED TO THE COST OF REPAIR OR REPLACEMENT OF THE PRODUCT. KONTRON TECHNOLOGY SHALL NOT BE LIABLE FOR:

- DAMAGE TO OTHER PROPERTY CAUSED BY ANY DEFECTS IN THE PRODUCT, DAMAGES BASED UPON INCONVENIENCE, LOSS OF USE OF THE PRODUCT, LOSS OF TIME, LOSS OF PROFITS, LOSS OF BUSINESS OPPORTUNITY, LOSS OF GOODWILL, INTERFERENCE WITH BUSINESS RELATIONSHIPS, OR OTHER COMMERCIAL LOSS, EVEN IF ADVISED OF THEIR POSSIBILITY OF SUCH DAMAGES.
- 2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.
- 3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.