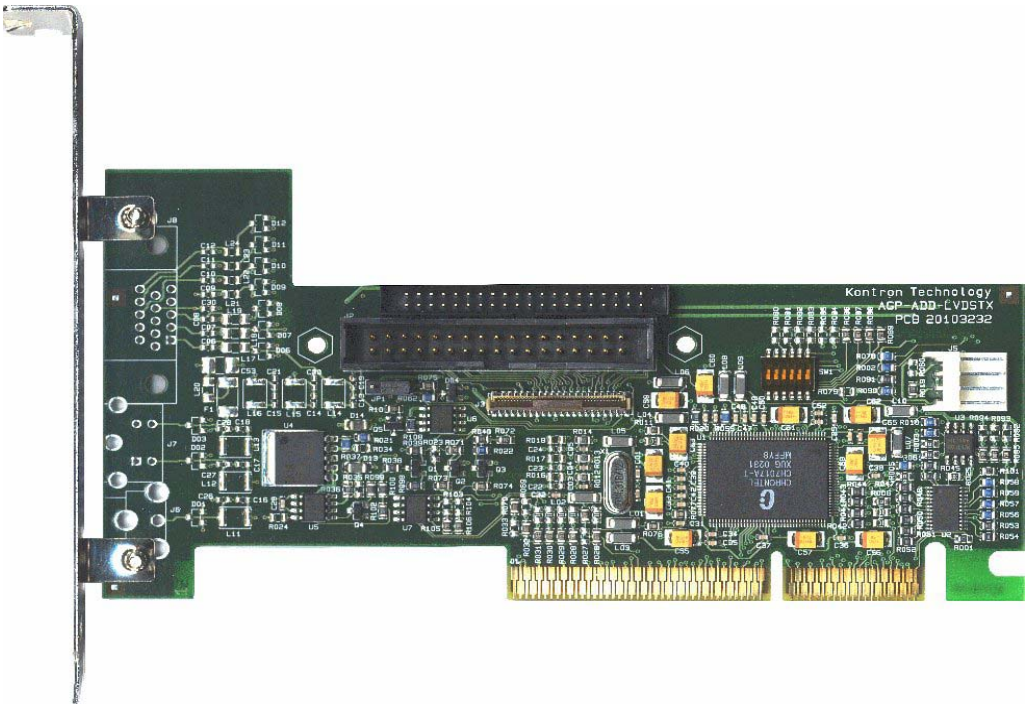
User Manual

ADD-LVDS and ADD-LVDS/OEM

AGP **D**igital **D**isplay card with **L**ow **V**oltage **D**ifferential **S**ignalling **T**ransmitter
Designed primarily for **886LCD/ATX** series of motherboards



	ADD-LVDS	ADD-LVDS/OEM
Part no.	720935	720936
PCB no.	20103232	20103232
Ass. no.	57220000	57220101
Note		

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A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Content:

Revision History

Revision	Release Date	By	Comment
E	June 17th 2004	MLA	Chapter 6, SW1 settings changed. JILI40 mating connector changed.
D	March 19th	MLA	New document layout
C	January 20th 2004	MLA	New front page picture and display added
B	August 19th 2003	MLA	Mechanical measurements added to chap. 4
A	August 15th 2003	MLA	Many corrections
0	July 10th 2003	MLA	Initial release

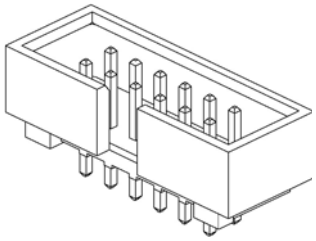
1. Introduction

The ADD-LVDS and the ADD-LVDS/OEM are AGP cards designed for implementing single - and dual pixel LVDS transmitter function to Intel 845 based motherboards via the ADD interface (AGP Digital Display interface). The modules support Flat Panel Displays with resolution up to QXGA (2048x1536 pixels), 24 bits of colours and cable length up to 10 meter. Both OpenLDI and SPWG colour coding are supported. See appendix A for more info on OpenLDI and SPWG.

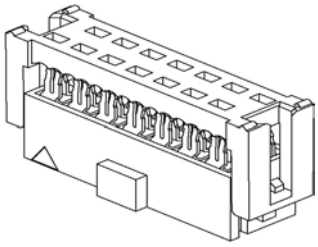
The circuit on the ADD-LVDS (-/OEM) is based on the Chrontel CH7017A chip, which receives display data signals via two DVO ports, driven by the host Intel 845 graphics controller. The CH7017 converts the DVO signals to LVDS signals depending on the driver selected colour coding (OpenLDI or SPWG). The LVDS signals are transmitted to the LVDS receiver via 4 - 10 pairs of twisted wires depending on the resolution of the selected display (number of pixels and number of colours). The LVDS signals are available from different types of connectors: 34-pole connector, JILI and JILI40.

The 34-pole connector is a standard 2x17-pin, 2,54mm spacing connector (like used on the old fashion FDD). The mating connector is cheap and easy to use (twisted pair (2x17) flat cable is available and discrete wires can be mounted without special tools). The 34-pole connector is also used on the LVDSTX-JPLCD products, so that same cable kit can be used on Kontron Technology IPC's.

34-pole connector signals:
- LVDS signals (1 or 2 pixel/clk)
- LVDS colour coding (OpenLDI & SPWG)
- Display power (3,3V, 5V or 12V)
- Backlight power (5V or 12V)
- Backlight on/off control signal.



2x17 pin 2.54 mm pitch
34-pole connector

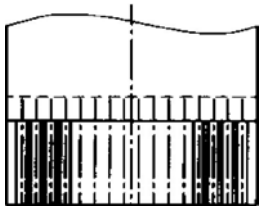


34-pole mating connector

The JILI interface (ADD-LVDS/OEM only) is based on FFC (Flat Foil Cable). JILI is a standard with many cable kits and LVDS receivers available.

JILI connector signals:
- LVDS signals (1 or 2 pixel/clk)
- LVDS colour coding (SPWG)
- Power available (5V or 12V)
- Enable LCDVCC control signal
- Backlight on/off control signal.
- DDC signals
- Display detect signal

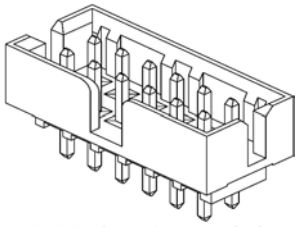
40-pole 0.5 mm pitch
JILI connector



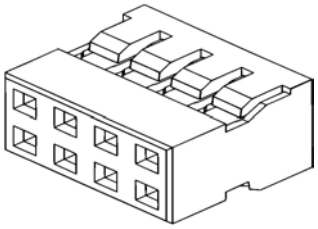
JILI cable (FFC)

The JILI40 interface (ADD-LVDS/OEM only) is based on a 2x20-pin 2.0 mm spacing connector. Several cable kits are available.

JILI40 connector signals:
- LVDS signals (1 or 2 pixel/clk)
- LVDS colour coding (SPWG)
- Display power (3,3Vor 5V)
- Backlight power (5V or 12V)
- Backlight on/off control signal.
- Backlight intensity control signal.
- DDC signals



2x20 pin 2.0 mm pitch
JILI40 connector



JILI40 mating connector

The ADD-LVDS/OEM contains all 3 types of above connectors but the ADD-LVDS only contains the 34-pole connector.

Kontron Technology has adapted several displays and more displays will be added in the future. A document called “List of display for 886LCD/ATX” is available on homepage and contains information about all approved displays and optionally cable kits and other information. On the homepage, also BIOS with driver support for all approved displays and BIOS programming tools can be found.

Kontron Technology do not support software for the backlight intensity control, the DDC signals and Display Detect signal (Hot Plug function), this is up to the customer to implement this support.

Display adaptation for the ADD-LVDS (-/OEM) is only supported by Kontron Technology for use in combination with Kontron 886LCD/ATX family of motherboards.

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KONTRON Technology A/S is a company that keeps up with the latest development and concentrate on developing and manufacturing embedded SBC and Add ON’s.
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2. Functional highlights

- Based on Chrontel CH7017A compatible with LVDS used in DS90CF364/DS90CF384/DS90CF388.
- Supports both OpenLDI - and SPWG standard
- Single - or dual pixel output up to 2 x 24-bit colors.
- JILI standard *, JILI40 standard * and 34-pole Connector supported
- 34-pole Connector supports 3.3V or 5V LCDVCC, selectable by DIP switch.
- 34-pole Connector supports +12V as LCDVCC, selectable by display cable kit.
- 34-pole Connector supports Backlight On signal inverted, selectable by DIP switch
- 34-pole Connector supports both 5V and 12V Backlight inverters
- Dual pin row 2.54 mm connector for LVDS cable based on twisted pair flat cable.

(*) = JILI and JILI40 connectors etc. are supported on the ADD-LVDS/OEM only. More information on JILI and JILI40 standards are available at www.dr-berghaus.de

3. Supported Configurations

The product is supported in 2 main configurations:

886LCD
In this case the ADD-LVDS module is used together with the Kontron Technology Industrial motherboards. Along with the module will follow a BIOS configured specifically for the customer Display setup. This configuration is made by a VBIOS with specific settings, which is merged into the motherboard basic BIOS. The ADD module is in this case generic (not configured).

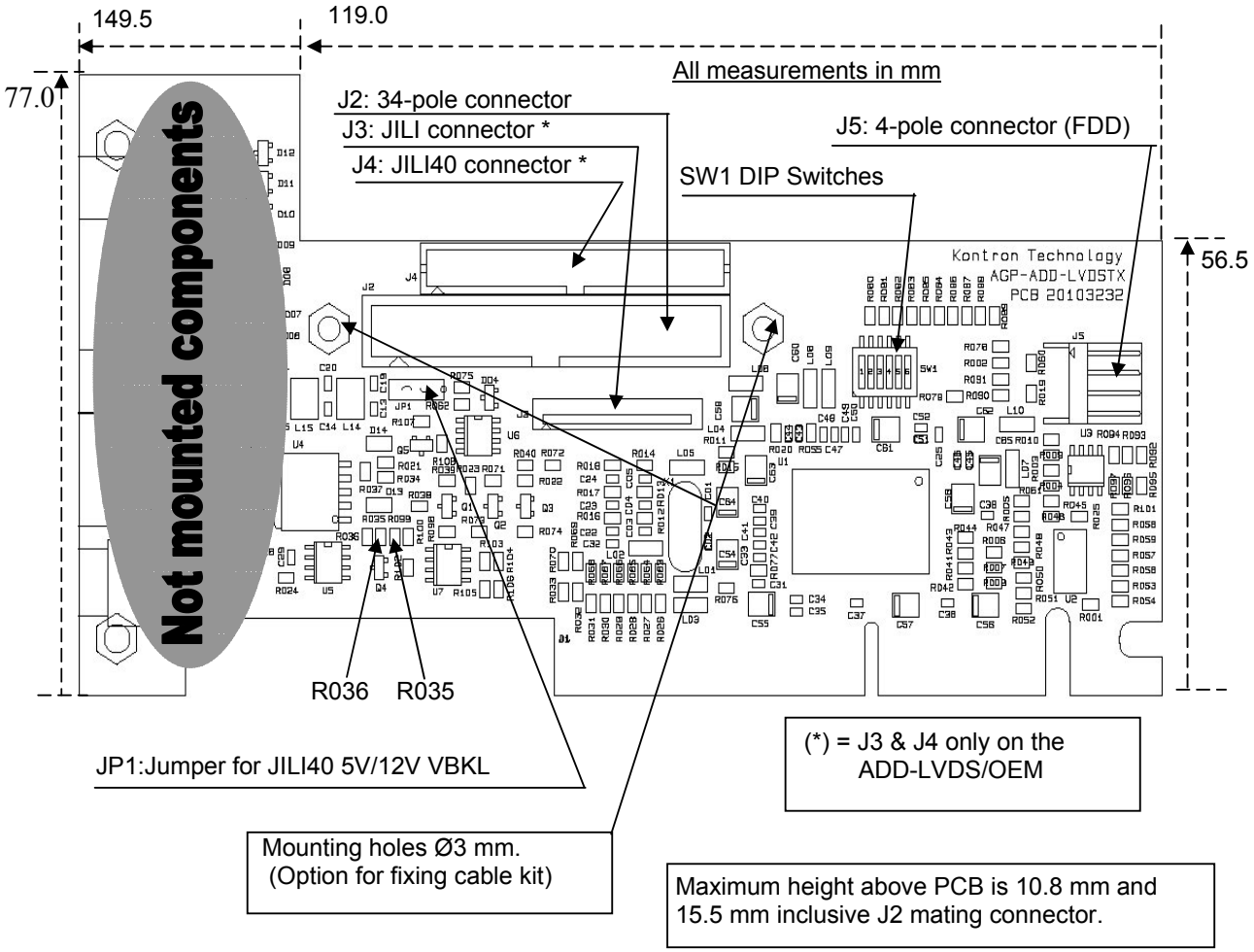
OEM
In this case the ADD-LVDS/OEM module is used. The motherboard type is (maybe) not Kontron Technology Industrial motherboards. In this case it is the responsibility of the OEM partner to configure the product.

Other optional configurations are not supported as default.

Type of ADD board	Type of motherboard	
	886LCD/ATX family	Unspecified (OEM selected)
ADD-LVDS	**886LCD** configuration 886LCD/ATX dedicated single display BIOS Display support services by KT	Optional configuration OEM defined dedicated single display BIOS Display support services by OEM
ADD-LVDS/OEM	Optional configuration 886LCD/ATX default BIOS Display support services by KT Note that DDC is not supported	**OEM** configuration OEM defined BIOS Display support services by OEM

4. ADD-LVDS (-/OEM) Layout

Front side:



"LCDVCC>2A" option can be implemented by moving the resistor R036 to the position R035. See later for more explanation.

5. Cable kit components

JILI and JILI40:

JILI always involves a dedicated display JILI receiver.
Find more information on www.dr-berghaus.de

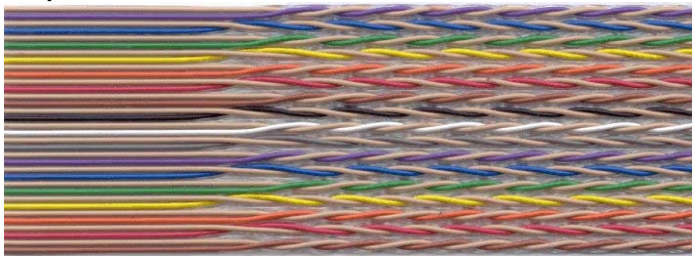
JILI40 mating connectors:
FCI Minitek housing 90311-040 w. crimp terminals 77138-101
Tarng Yu housing TU2003HNO-2x20R

34-pole connector:

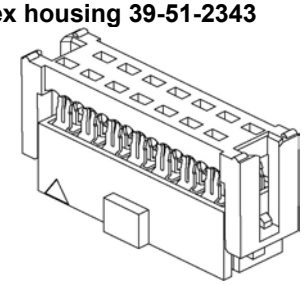
Can be used for display with integrated LVDS Receiver and for dedicated display LVDS Receiver.

The J2 mating connector is a standard 2 x17 pole, 2,54 mm pitch Floppy cable connector, Molex housing 39-51-2343 specified to 1A maximum per terminal. The twisted pair flat cable from 3M part no. 1700/34, fits the above J2 mating connector.

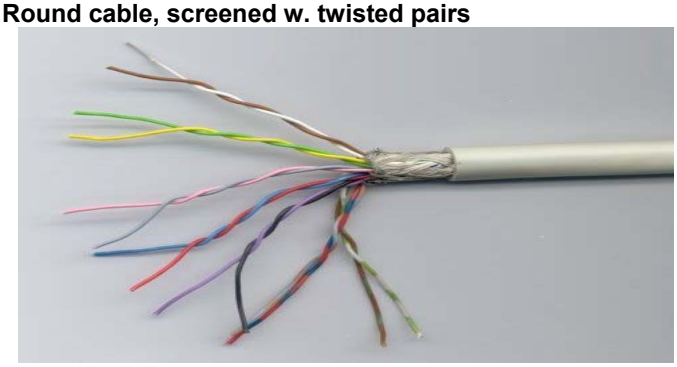
3M part no. 1700/34



Molex housing 39-51-2343

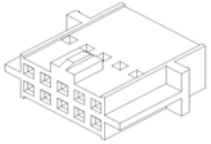


Round cable, screened w. twisted pairs

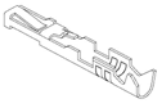


As an alternative the Molex housing 90160-0134 (and crimp terminals) can manage 2A maximum per terminal

Molex housing 90160-0134



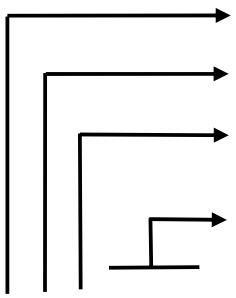
90119 crimp terminal



For more information please see appendix B.

6. SW1 settings

Dip-Switch1 (SW1) is used to configure Backlight control signal, LCDVCC and to select a display type. In order to select the display type the ADD card shall be of a version that has SPD (Serial Programmable Device). The ADD-LVDS card do not have SPD and therefore the requested display shall be defined by the VGA BIOS of the motherboard. The ADD-LVDS-OEM has SPD which can contain 5 different display settings (Display #1 - Display #5). On request the SPD code can be modified by Kontron Technology in order to make a single SPD code have support for 5 selected displays. The standard SPD code is SPD001.

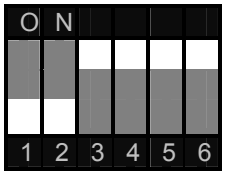
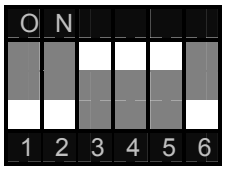
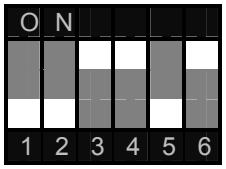
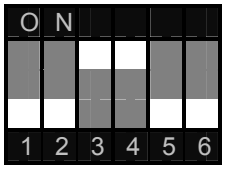
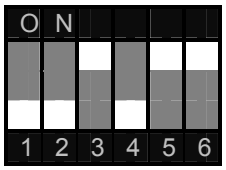


Off/On => BKLON signal active high/low

Off/On => LCDVCC power = 3.3V/5V

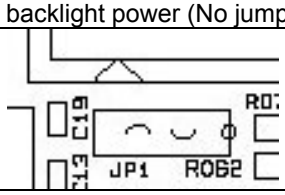
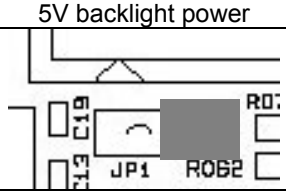
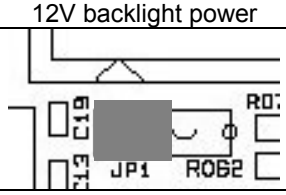
If ADD-LVDS card then position don't care.
For other cards position shall always be ON

If ADD-LVDS card then position don't care.
For other cards the combination of settings is used to select requested display in according to SPD version

		SPD001	SPD010 (TBD)
Display # 1 (Default)		800x600 18 bit 40 MHz	
		Unipac UB084S01 NEC NL8060BC31-17D Sharp LQ12S41	
Display # 2		1024x768 24 bit 2 pix./clk OpenLDI 65 MHz	
		CPT CLAA150XA03	
Display # 3		1024x768 24 bit 1 pix./clk SPWG 65 MHz	1024x768 24 bit 1 pix./clk OpenLDI 65 MHz
		LG.Philips LC151X01 (C3) Samsung LTM150XH-L04 Sharp LQ150X1LW71 Toshiba LTM15C458T	NEC NL10276BC30-10
Display # 4		1280x1024 24 bit 2 pix./clk SPWG 135 MHz	1280x768 24 bit 1 pix./clk OpenLDI 65MHz
		LG.Philips LM181E06-A4M1	Samsung LTA260W1
Display # 5		1280x1024 24 bit 2 pix./clk OpenLDI 135 MHz	1600x1200 24 bit 2 pix./clk SPWG 125 MHz
			LG.Philips LM201U03

7. JP1 settings

The JP1 (3-pin row connector) is used to select either 5V or 12V as backlight power on JILI40 (J4).

No backlight power (No jumper)	5V backlight power	12V backlight power
		

Note that 4-pole power plug (J5) must be connected.

8. LCDVCC>2A option

Today all known LCD's requires less than 2A (Ampere) (average) on the LCDVCC, normally lower than 1A, anyway if in future a display requires more than 2A, then the LCDVCC>2A option can be used. Another situation could be that a system has to drive more than one display.

The LCDVCC>2A option can only be used for LCDVCC = 5V. In case 3.3V is required for LCDVCC, then it is recommended to use LCDVCC = 5V and then use 3.3V voltage regulator(s) near the display(s).

If the resistor (0 Ohm) in position R036 is moved to the position R035, then the LCDVCC will no longer be supplied via the AGP connector with the limitation of the 2A (average). In stead the LCDVCC = 5V is supplied via the 4-pole connector (J5) and the maximum average current is increased to 3A on J2 and on J4 (in total).

9. Installation procedure

1. If using the 34-pole Connector (J2), then select 3.3V or 5V on the dip switch no. 2, depending on the display, see display datasheet. If display supply voltage shall be +12V, then use the +12V available on the J2 pin 1-2.
2. If inverter is using the Backlight Control signal from 34-pole Connector, then select requested polarity by dip switch no. 1. (OFF => backlight active on high level).
3. If ADD-LVDS/OEM then select requested display type via the dip switch no. 3-6.
4. If ADD-LVDS/OEM is used on 886LCD family of motherboards, then load default BIOS into the 886LCD.
5. If ADD-LVDS is used on 886LCD family of motherboards, then load BIOS with support for the requested display, into the 886LCD.
6. If JILI shall be used or if +12V shall be used for display voltage supply or if backlight inverter shall be supported, then connect FDD power to J5. Please notice that if the JILI connector is used (J3) then you don't have to think about the display power, it will be programmed in the JILI receiver module.
7. If JILI40 (J4) is used then select +5V or +12V as backlight support (if required).
8. Make sure power is turned off and then insert the ADD-LVDS (-/OEM) into the AGP connector on the motherboard.
9. Connect cable kit for display, optionally for inverter and for power (J5) and turn on power. See *Appendix B: Cable kit design* for information on how to design a cable kit based on the Twisted Pair Flat Cable.
10. Verify that the display turns on. It is recommended to enter the BIOS setup menu and verify that the picture is stabile and colours are correct.
11. Enter the OS and install the graphic drivers (if not already done). (886LCD/ATX drivers are available on www.inside.dk).
12. Select display resolution, select number of colour bits and enable the panel. Please notice that the Intel 845 Graphic driver support expanded mode only when CRT is disabled.

10. Connectors

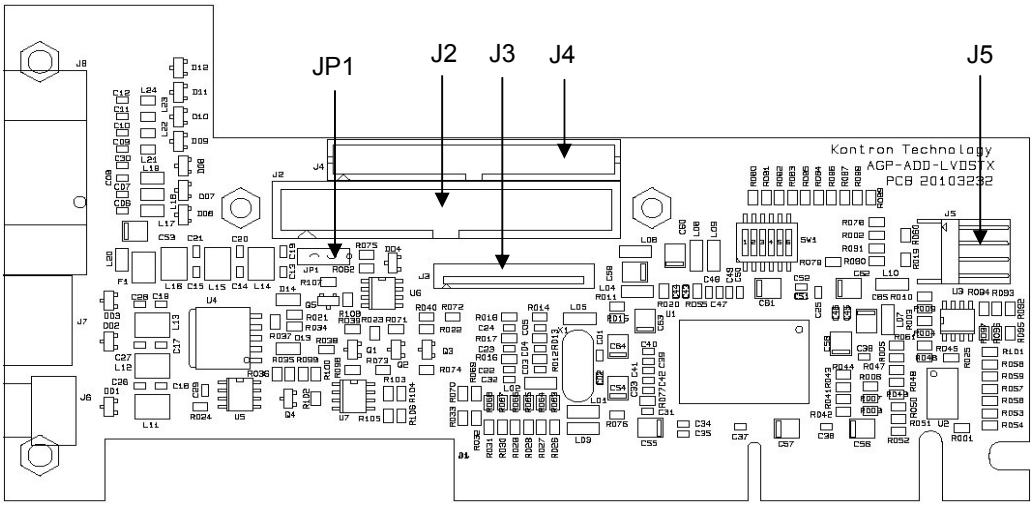
J2 (**34-pole Connector**) Aptos XPHS-34R1-B. Mating connector Molex 39-51-2343 (max 1A per terminal) or Molex 90160-0134 with crimp terminals 90119 (max 2A per terminal).

J3 (**JILI**) FH12-40S-0.5SH, Mating FFC with 40 poles 0,5 mm pitch (max. 0,4A per terminal).

J4 (**JILI40**) Molex connector 87331-4020. Mating connector FCI Minitek housing 90311-040 w. crimp terminals 77138-101 (max 2A per terminal)

J5 (**FDD power**) AMP 2-171826-4 for power connection, 4-pole pin row.
Mating connector “standard FDD power mating connector”.

JP1 (**3-pole Connector**) Aptos XHY-03S-B-A/B. Mating Jumper Aptos PHJ-MA-B



J2 connector (34-pole connector)

Pin	Function	Signal type	Note
1	+12V	Power-out	+12V total load on pin 1-2: Max 4 A
2	+12V	Power-out	(Only if J5 is supplied by power and LCDVCC is on)
3	GNDBKL	Power-out	GNDBKL total current on pin 3-4: Max 4 A
4	GNDBKL	Power-out	(Only if J5 is supplied by power)
5	+5V	Signal-out	+5V total load on pin 5-6: Max 4A
6	+5V	Power-out	(Only if J5 is supplied by power)
7	ENBKL, /ENBKL	Signal-out	High level 4V/0,8mA (Pullup 1K2 to J5 +5V), Low level 0,8V/1,8mA (Select ENBKL or /ENBKL on SW1-1)
8	GND	Power-out	GND total current on pin 8, 19-20, 31-32: Max 4A
9	A7-	LVDS-out	
10	A7+	LVDS-out	
11	CLK2-	LVDS-out	
12	CLK2+	LVDS-out	
13	A6-	LVDS-out	
14	A6+	LVDS-out	
15	A5-	LVDS-out	
16	A5+	LVDS-out	
17	A4-	LVDS-out	
18	A4+	LVDS-out	
19	GND	Power-out	GND total current on pin 8, 19-20, 31-32: Max 4A
20	GND	Power-out	
21	A3-	LVDS-out	
22	A3+	LVDS-out	
23	CLK1-	LVDS-out	
24	CLK1+	LVDS-out	
25	A2-	LVDS-out	
26	A2+	LVDS-out	
27	A1-	LVDS-out	
28	A1+	LVDS-out	
29	A0-	LVDS-out	
30	A0+	LVDS-out	
31	GND	Power-out	GND total current on pin 8, 19-20, 31-32: Max 4A
32	GND	Power-out	
33	LCDVCC	Power-out	+3.3V or +5V total load on pin 33-34: Max 2A *
34	LCDVCC	Power-out	(Select 3.3V or 5V on SW1-2)

* = If the LCDVCC>2A option is used, then the +5V available on pin 33 & 34 can deliver 3A maximum average if at the same time pin 5 & 6 are not loaded with more than 1A.

J3 connector (JILI)

Pin	Function	Signal type	Note
1	+12V	Power-out	+12V total load on pin 1-3: Max 1.2 A allowed
2	+12V	Power-out	(Only if J5 is supplied by power)
3	+12V	Power-out	
4	GNDBKL	Power-out	GNDBKL total current on pin 4-5: Max 0.8 A allowed
5	GNDBKL	Power-out	(Only if J5 is supplied by power)
6	ENBKL, /ENBKL	Signal-out	High level 4V/0,8mA (Pullup 1K2 to J5 +5V), low level 0,8V/1,8mA
7	+5V	Power-out	
8	+5V	Power-out	+5V total load on pin 7-10: Max 1.6 A allowed
9	+5V	Power-out	(Only if J5 is supplied by power)
10	+5V	Power-out	
11	A7+	LVDS-out	
12	A7-	LVDS-out	
13	GND	Power-out	
14	CLK2+	LVDS-out	
15	CLK2-	LVDS-out	
16	GND	Power-out	
17	A6+	LVDS-out	
18	A6-	LVDS-out	
19	GND	Power-out	
20	A5+	LVDS-out	
21	A5-	LVDS-out	
22	DDCCLK	I2C	
23	A4+	LVDS-out	
24	A4-	LVDS-out	
25	DDCDAT	I2C	
26	A3+	LVDS-out	
27	A3-	LVDS-out	
28	GND	Power-out	
29	CLK1+	LVDS-out	
30	CLK1-	LVDS-out	
31	GND	Power-out	
32	A2+	LVDS-out	
33	A2-	LVDS-out	
34	ENVEE	TTL out	
35	A1+	LVDS-out	
36	A1-	LVDS-out	
37	ENVCC	TTL-out	
38	A0+	LVDS-out	
39	A0-	LVDS-out	
40	DETECT	TTL in	

J4 connector (JILI40)

Pin	Function	Signal type	Note
1	ENBKL, /ENBKL	Signal-out	High level 4V/0,8mA (Pullup 1K2 to J5 +5V),
2	(Same as above)	Signal-out	Low level 0,8V/1,8mA
3	BLKADJ	Analogue out	Output from MAX517
4	A7+	LVDS-out	
5	A7-	LVDS-out	
6	VBKL	Power-out	Pin 6, 9, 12, 15 & 18 max 3A in total, JP1 selects 5V/12V (*)
7	CLK2+	LVDS-out	
8	CLK2-	LVDS-out	
9	VBKL	Power-out	Pin 6, 9, 12, 15 & 18 max 3A in total, JP1 selects 5V/12V (*)
10	A6+	LVDS-out	
11	A6-	LVDS-out	
12	VBKL	Power-out	Pin 6, 9, 12, 15 & 18 max 3A in total, JP1 selects 5V/12V (*)
13	A5+	LVDS-out	
14	A5-	LVDS-out	
15	VBKL	Power-out	Pin 6, 9, 12, 15 & 18 max 3A in total, JP1 selects 5V/12V (*)
16	A4+	LVDS-out	
17	A4-	LVDS-out	
18	VBKL	Power-out	Pin 6, 9, 12, 15 & 18 max 3A in total, JP1 selects 5V/12V (*)
19	A3+	LVDS-out	
20	A3-	LVDS-out	
21	GND	Power-out	
22	GND	Power-out	
23	DDCCLK	I2C-bus	
24	DDCDAT	I2C-bus	
25	GND	Power-out	
26	CLK1+	LVDS-out	
27	CLK1-	LVDS-out	
28	GND	Power-out	
29	A2+	LVDS-out	
30	A2-	LVDS-out	
31	GND	Power-out	
32	A1+	LVDS-out	
33	A1-	LVDS-out	
34	GND	Power-out	(ENVEE not supported)
35	A0+	LVDS-out	
36	A0-	LVDS-out	
37	GND	Power-out	
38	GND	Power-out	
39	LCDVCC	Power-out	+3.3V/5V total load on pin 39-40: Max 2A allowed **
40	LCDVCC	Power-out	

* = (Only if J5 is supplied by power)

** = If the LCDVCC>2A option is used, then the +5V available on pin 39 & 40 can deliver 4A maximum minus the possible +5V load from the pins 6, 9, 12, 15 & 18.

J5 connector (4-pole power)

Pin	Function	Note
1	+5V	Max 4 A
2	GND	Total current on
3	GND	pin 2-3: Max 8A
4	+12V	Max 4A

The power connector can be connected with a standard FDD power plug. It's necessary to connect the power plug if JILI or JILI40 is used or if 12V is required for backlight power and/or as LCDVCC.

11. Electrical specifications

LCDVCC output power available on J2 pin 33-34 and J4 pin 39-40

Voltage selected by DipSw no. 2: 3,3V in OFF-position (default) and 5V in ON-position

Voltage 3,3V, 2A maximum average, 3A peak
Voltage range:
3,45 +/-3% @ no load
3,35 +/-3% @ 2A load

Voltage +5V, 2A maximum average, 3A peak
Voltage range:
* @ no load,
* –2% @2A load

* = Voltage available from AGP connector pin 1-2

LCDVCC>2A option:
Voltage +5V, 4A maximum
Voltage range:
* @ no load,
* –2% @2A load
* –4% @4A load

* = Voltage available from via J5 connector

+12V output power available on J2 pin 1-2

Voltage supplied via J5. +12V is only enabled if LCDVCC is enabled.

Voltage +12V, 4A maximum average, 6A peak
Voltage range:
* @ no load,
* typical –2% @ 4 A load (max allowed via J2 pin 1-2, when Molex 90160-0134/90119 used)
* typical –1% @ 2 A load (max allowed via J2 pin 1-2, when Molex 39-51-2343 used)

* = Voltage available from J4 pin 4

+12V output power available on J3 pin 1-3

Voltage supplied via J5. +12V is only enabled if LCDVCC is enabled.

Voltage +12V, 1.2A maximum average, 1.8A peak
Voltage range:
* @ no load,
* typical –0,6% @ 1.2A load (max allowed via J3 pin 1-3)

* = Voltage available from J5 pin 4

+5V output power available on J2 pin 5-6

Voltage supplied via J5.

Voltage +5V, 4A maximum average, 6A peak

Voltage range:
* up to 4 A load (max allowed via J2 pin 5-6, when Molex 90160-0134/90119 used)
* up to 2 A load (max allowed via J2 pin 5-6, when Molex 39-51-2343 used)

* = Voltage available from J5 pin 1

+5V output power available on J3 pin 7-10

Voltage supplied via J5.

Voltage +5V, 1.6A maximum average, 2.4A peak
Voltage range:
* up to 1.6 A load (max allowed via J3 pin 7-10)

* = Voltage available from J5 pin 1

+5V or +12V (selectable by JP1) on J4 pin 6, 9, 12, 15 &18

Maximum average load is 3A.

ENVCC output signal available on J3 pin 37

TTL-output signal.

ENVEE output signal available on J3 pin 34

TTL-output signal.

ENBKL output signal available on J2 pin 7, J3 pin 6 & J4 pin 1-2

High-level 4V/0,8mA (Pull-up resistor 1K2), low-level -0,8V/1,8mA

All LVDS signals available on J2, J3 & J4

See Chrontel datasheet CH7017A for detailed information.

DDCDAT and DDCCLK, (DDC signals) available on J3 and J4

I2C signals.

DETECT, available on J3

TTL-input.

LCDVCC input power (+5V and 3.3V) requirements

Voltage supplied via the AGP.

Voltage +5V, 2A maximum average, 3A peak
Voltage range: 4,85V – 5.25V

LCDVCC input power (+5V only) (when LCDVCC>2A option) requirements

Voltage supplied via J5.

Voltage +5V, 4A maximum average
Voltage range: 4,85V – 5.25V

BLKADJ (Backlight adjustment) J4 pin 3

Please see MAX517 datasheet.

All remaining input signals available via AGP

DVO inputs, for more information see Intel 845 datasheet.

Operating temperature: 0-60ºC

12. Trouble shooting

A little bit of pixel noise can be seen.
Have you used twisted pair cable and 1 pair of wires for each LVDS pair?
Are all the pairs of the same length within a few mm?
Is cable long (> 5m)? Try with a shorter cable and check if the noise disappears.
If using cable > 5 m., then optionally a resistor R055 can be replaced for adjusting the DC swing.
Bad connections or cable kit consisting of more than one piece of cable and involving several connectors, might introduce noise.

Some shadows can be seen.
These shadows have typically a stable colour (red, blue or green) no matter on which part of the display it is present. Display driver has to be adjusted, possibly clock phase adjustment (by Kontron Technology)

Colours are wrong all over the picture but picture size is ok and colours are stabile.
The driver has most likely to be modified (or replaced) in order to change from OpenLDI to SPWG (or the other way around).

The colours are stabile but wrong all over the picture and picture size is not ok.
Have you selected a driver for 1-pixel/clock instead of 2-pixel/clock or vice versa?

Backlight is on, but no picture is present and CRT Monitor do not turn on.
Have you (in BIOS) enabled the On-Chip VGA?
Have you in BIOS selected Boot Display = Auto?
Have you loaded correct BIOS to support the actual display?
Have you on the ADD-LVDS (-/OEM) selected the correct LCDVCC 3,3V, 5V, or 12V?
In case the display requires LCDVCC = 12V via J2, then verify that J2 pin 1-2 is used for LCDVCC.

No backlight, if you enter BIOS you might be able to recognise a very dark picture.
Is J5 supplied by FDD power?
Is SW1.1 in the wrong position?
Can you measure +12V and/or +5V at the inverter and is the BKLON signal ok (if used)?
Otherwise the inverter must be defect?

No backlight and no picture and CRT Monitor do not turn on.
Have you in BIOS enabled the On-Chip VGA?
Have you in BIOS selected Boot Display = Auto?
Have you loaded correct BIOS to support the actual display?
Have you on the ADD-LVDS (-/OEM) selected the correct LCDVCC 3,3V, 5V, or 12V?
In case the display has LCDVCC = 12V and using J2 to interface to the display, remember to connect the 4-pole power plug and to use J2 pin 1-2 for LCDVCC.
Can you measure LCDVCC on the display?
Can you measure LCDVCC (3,3V or 5V) on J2 pin 33-34 or alternatively +12V on J2 pin 1-2 if display requires +12V for LCDVCC?

Bad picture only after starting up the OS
If you have a bad picture quality after starting up the OS, then please make sure the OS display driver is installed correctly and that the selected resolution is the same as for the actual display and that the number of colours is selected as requested.

Appendix A. Colour bit reference table

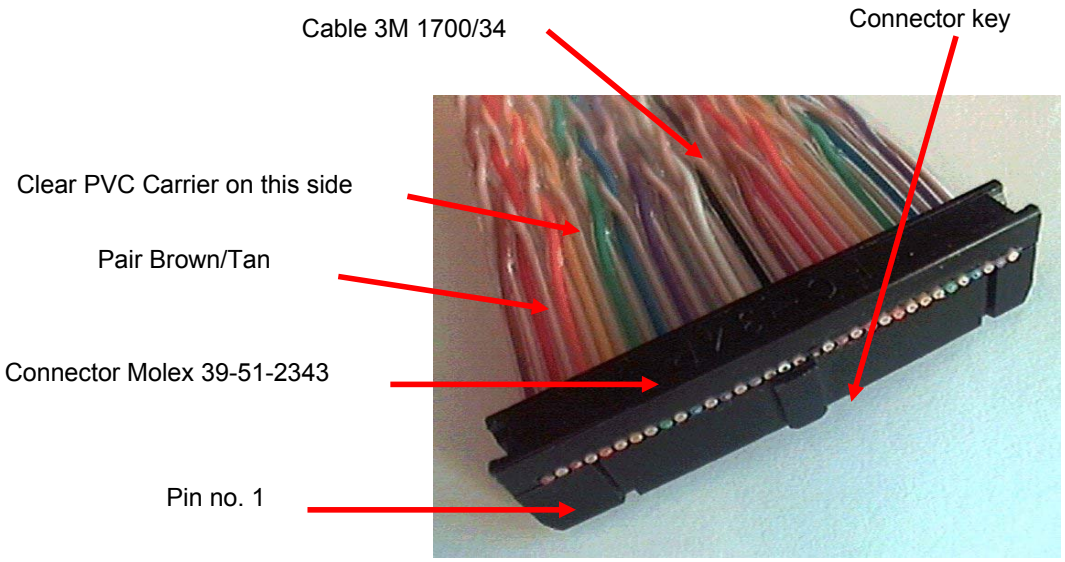
ADD-LVDS			Display, colours		
Channel.Bit	**(SPWG)**	**(OpenLDI)**	**24-bit (SPWG)**	**24-bit (OpenLDI)**	**18-bit (OpenLDI)**
A0.1	R10	R12	R10	R12	R10
A0.2	R11	R13	R11	R13	R11
A0.3	R12	R14	R12	R14	R12
A0.4	R13	R15	R13	R15	R13
A0.5	R14	R16	R14	R16	R14
A0.6	R15	R17	R15	R17	R15
A3.1	R16	R10	R16	R10	-
A3.2	R17	R11	R17	R11	-
A0.7	G10	G12	G10	G12	G10
A1.1	G11	G13	G11	G13	G11
A1.2	G12	G14	G12	G14	G12
A1.3	G13	G15	G13	G15	G13
A1.4	G14	G16	G14	G16	G14
A1.5	G15	G17	G15	G17	G15
A3.3	G16	G10	G16	G10	-
A3.4	G17	G11	G17	G11	-
A1.6	B10	B12	B10	B12	B10
A1.7	B11	B13	B11	B13	B11
A2.1	B12	B14	B12	B14	B12
A2.2	B13	B15	B13	B15	B13
A2.3	B14	B16	B14	B16	B14
A2.4	B15	B17	B15	B17	B15
A3.5	B16	B10	B16	B10	-
A3.6	B17	B11	B17	B11	-
A2.5	Hsync	Hsync	Hsync	Hsync	Hsync
A2.6	Vsync	Vsync	Vsync	Vsync	Vsync
A2.7	DE	DE	DE	DE	DE
A3.7	RES	RES	RES	RES	-

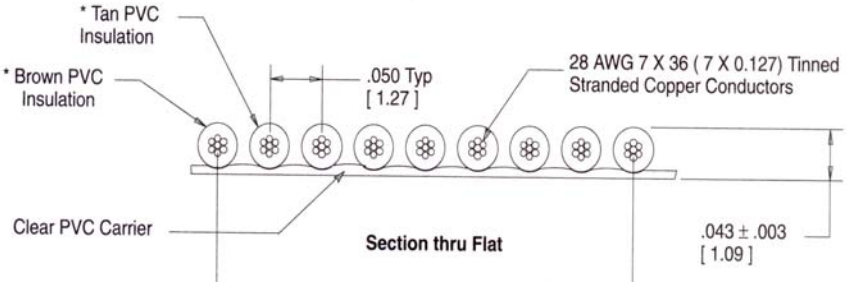
Appendix B: Cable kit design

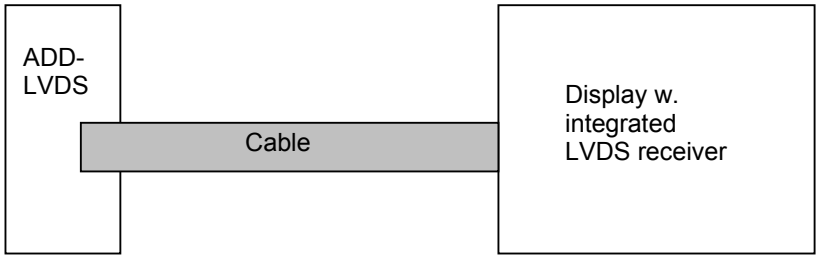
Cable kits for JILI and JILI40, please see www.dr-berghaus.de.

Cable kits for low cost and prototypes (Do it your self type) for the 34-pole pin row connector can be based on the 34-polede 0.50" Twisted pair Cable from 3M, type no. 1700/34.

The connector that fit's the cable and the mating connector on the ADD-LVDS –(/OEM) can be the Molex 39-51-2343 (Max 1 Amp per terminal).







Cable for Panel with integrated LVDS receiver

On the next page you will find example of Interface Specification.

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CPT CLAA150XA03-A for LVDSTX-JPLCD & ADD-LVDS

KTD-00430-B Public Interface Specification Date: 2004-03-19 Page 1 of 1

Display type: CPT CLAA150XA03-A
Cable no.: not available
System: LVDSTX-JPLCD on 786LCD/S-/MG-/ST-/5.25 or GX1LCD/S- /S-Plus
ADD-LVDSTX (-/OEM) on 886LCD/ATX family or similar

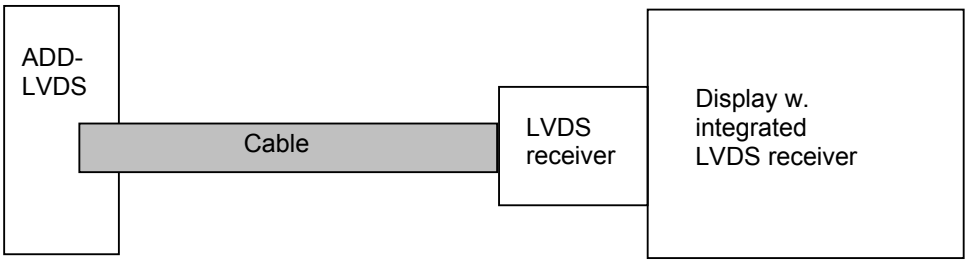
786LCD/S-/MG-/ST-/5.25 or GX1LCD/S- /S-Plus:
Display driver: CPT CLAA150XA03-A, 5V
LVDSTX-JPLCD settings: SW1(1,2,3,4,5,6)= (off,off,off,off,on,off)

ADD-LVDSTX: BIOS *GX203XGA2P24O*, SW1(1,2,3,4,5,6)= (off,on,x,x,x,x)
ADD-LVDSTX (-/OEM): BIOS *GX203*, SW1(1,2,3,4,5,6)= (off,on,on,on,on,off)

Display	(30-pole conn.)	34-pole connector		Remarks
Pin no.	Function	Pin	Function	
1	VDD	34	LCDVCC	+5V
2	VDD	33	LCDVCC	+5V
3	VSS	32	GND	
4	VSS	31	GND	
5	1Link, Rx0-	29	A0-	Pair no 1
6	1Link, Rx0+	30	A0+	Pair no 1
7	VSS	-	GND	
8	1Link, Rx1-	27	A1-	Pair no 2
9	1Link, Rx1+	28	A1+	Pair no 2
10	VSS	-	GND	
11	1Link, Rx2-	25	A2-	Pair no 3
12	1Link, Rx2+	26	A2+	Pair no 3
13	VSS	20	GND	
14	1Link, CLK-	23	CLK1-	Pair no 4
15	1Link, CLK+	24	CLK1+	Pair no 4
16	VSS	19	GND	
17	1Link, Rx3-	21	A3-	Pair no 5
18	1Link, Rx3+	22	A3+	Pair no 5
19	VSS	8	GND	
20	VDD	-	LCDVCC	+5V
21	2Link, Rx0-	17	A4-	Pair no 6
22	2Link, Rx0+	18	A4+	Pair no 6
23	2Link, Rx1-	15	A5-	Pair no 7
24	2Link, Rx1+	16	A5+	Pair no 7
25	2Link, Rx2-	13	A6-	Pair no 8
26	2Link, Rx2+	14	A6+	Pair no 8
27	2Link, CLK-	11	CLK2-	Pair no 9
28	2Link, CLK+	12	CLK2+	Pair no 9
29	2Link, Rx3-	9	A7-	Pair no 10
30	2Link, Rx3+	10	A7+	Pair no 10

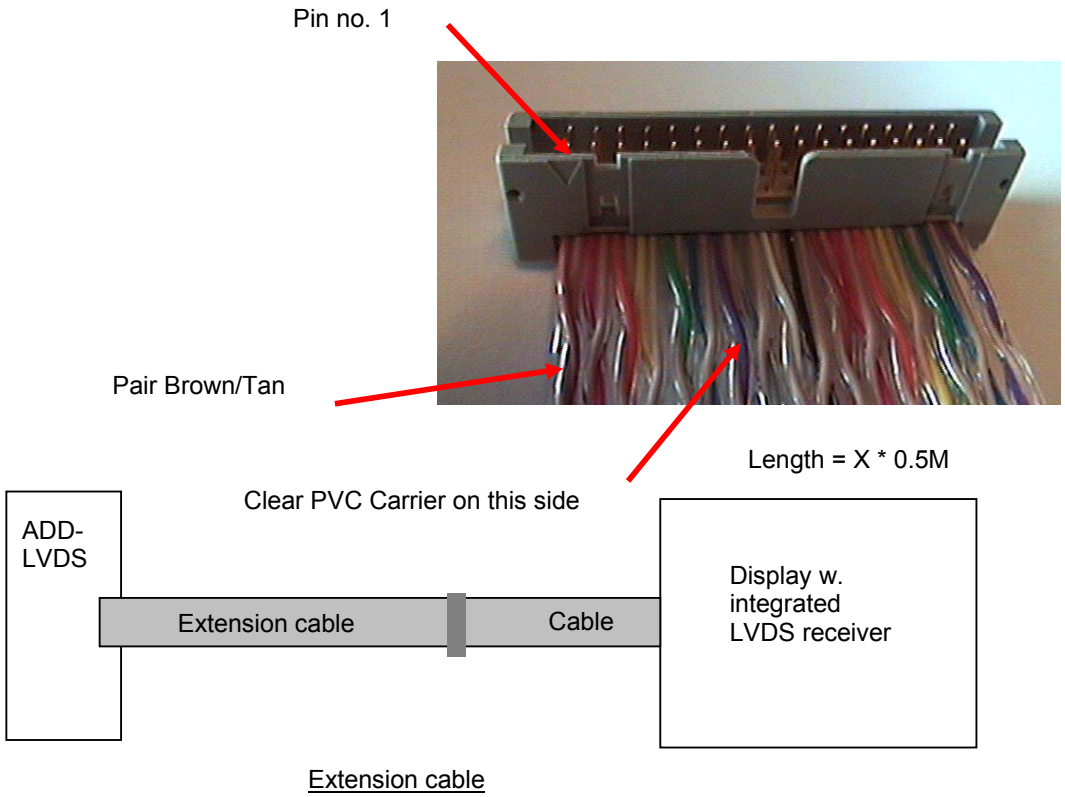
Inverter	type ?	34-pole connector	Remarks
Pin no.	Function	Pin	
1	+12V	1+2	
2	GND	3	
3	GND	4	GND => max intensity
4	NC	-	
5	BLKON	7	Back Light On *

Instead of using a display with integrated LVDS receiver, a dedicated LVDS receiver can be designed for a specific display. In this case it's most likely possible that a cable kit between the receiver and the display is not needed. The LVDS receiver can have a connector for the LVDS cable that makes it possible to make a one to one cable kit based on the twisted pair flat cable.



Cable for LVDS receiver

In case an extension cable is required, it can be made the same way as described above, but the connector for the display is replaced by 3M 4634-6001 or similar. See picture below.



Extension cable

Alternative to the Molex 39-51-2343 is the Molex housing 90160-0134 and 90119 crimp terminal for AWG28. This will make up to 2 Amp. per terminal possible.