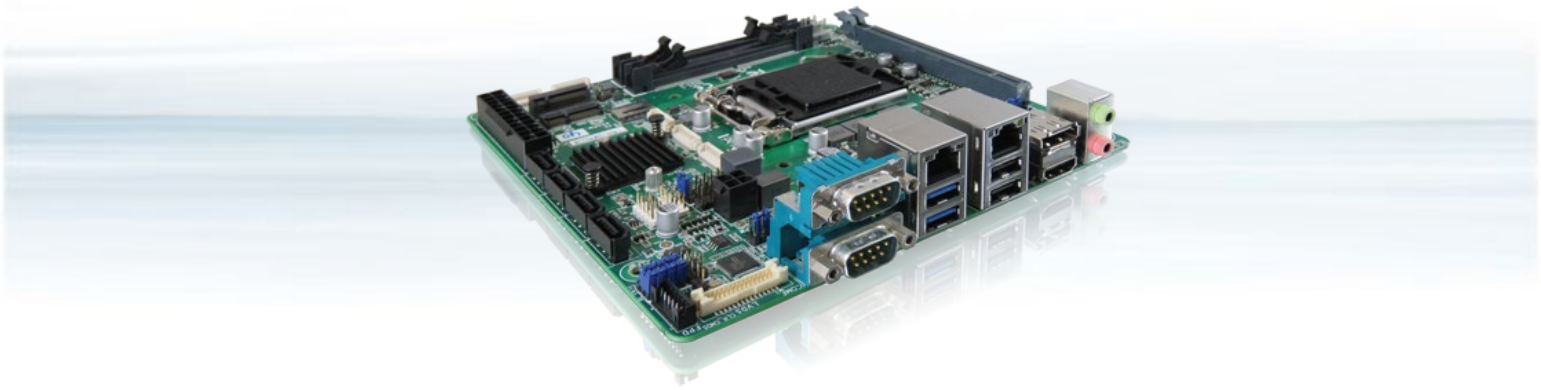
USER GUIDE



# MITX-CFL0 Series

Doc. User Guide, Rev. 1.2

Doc. ID: [To be Determined]

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# MITX-CFL0 SERIES - USER GUIDE

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## Revision History

| Revision | Brief Description of Changes | Date of Issue | Author/ Editor |
|---|---|---|---|
| 1.0 | Initial Issue | 2021-Jan-13 | YS |
| 1.1 | Update COM naming | 2021-Mar-11 | YS |
| 1.2 | Modify COME_PW & COMF_PW jumper position | 2022-Jan-17 | YS |

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# Symbols

The following symbols may be used in this user guide

| | |
|---|---|
| **⚠DANGER** | DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury. |
| **⚠WARNING** | WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury. |
| ***NOTICE*** | NOTICE indicates a property damage message. |
| **⚠CAUTION** | CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury. |
|  | Electric Shock!<br>This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material. |
|  | ESD Sensitive Device!<br>This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times. |
|  | HOT Surface!<br>Do NOT touch! Allow to cool before servicing. |
|  | Laser!<br>This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing. |
|  | This symbol indicates general information about the product and the user guide.<br>This symbol also indicates detail information about the specific product configuration. |
|  | This symbol precedes helpful hints and tips for daily use. |

# For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

## High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

**⚠CAUTION**

Warning

**All operations on this product must be carried out by sufficiently skilled personnel only.**

**⚠CAUTION**

Electric Shock!

**Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.**

**Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.**

## Special Handling and Unpacking Instruction

***NOTICE***

ESD Sensitive Device!

**Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.**

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

### Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

**⚠CAUTION**

**Danger of explosion if the battery is replaced incorrectly.**

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

## General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

## Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit http://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

### Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

### WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

**Environmental protection is a high priority with Kontron.**

**Kontron follows the WEEE directive**

**You are encouraged to return our products for proper disposal.**

# Table of Contents

# List of Tables

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# 1/ Introduction

This user guide describe the MITX-CFL0 Series board made by Kontron. This board will also be denoted MITX-CFL0 Series within this user guide.

Use of this user guide implies a basic knowledge of PC-AT hardware and software. This user guide focuses on describing the MITX-CFL0 Series board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching on the power.

All configuration and setup of the CPU board is either carried out automatically or manually by the user via the BIOS setup menus.

Latest revision of this user guide, datasheet, thermal simulations, BIOS, drivers, BSP's (Board Support Packages), mechanical drawings (2D and 3D) can de download from Kontron's Web Page.

# 2/ Installation Procedures

## 2.1. Installing the Board

**NOTICE**

**ESD Sensitive Device**

**Electrostatic discharge (ESD) can damage equipment and impair electrical circuitry.**

- Wear ESD-protective clothing and shoes
- Wear an ESD-preventive wrist strap attached to a good earth ground
- Check the resistance value of the wrist strap periodically (1 MΩ to 10 MΩ)
- Transport and store the board in its antistatic bag
- Handle the board at an approved ESD workstation
- Handle the board only by the edges

To get the board running follow these steps. If the board shipped from Kontron already has components like RAM and CPU cooler mounted, then skip the relevant steps below.

1. **Turn off the PSU (Power Supply Unit)**

**NOTICE**

**Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected while configuring the board. Otherwise, components (RAM, LAN cards etc.) might get damaged. Make sure to use a standard ATX PSU and a standard ATX12V PSU with suitable cable kits and PS-ON# active.**

**NOTICE**

**The power supply unit shall comply with the requirements as defined in IEC 62368-1 according Clause 6.2.2 to power source category PS2 "Limited Power Source".**

2. **Insert the DDR4 SO-DIMM 260-pin module(s)**
   Be careful to push the memory module(s) in the slot(s) before locking the tabs. For a list of approved SO-DIMMs contact your Distributor or FAE. See also chapter "System Memory Support". Use SO-DIMM with the same memory density in both sockets!
3. **Cooler installation**
   You can connect the cooler fan electrically to the CPU FAN connector.
4. **Connecting interfaces**
   Insert all external cables for hard disk, keyboard etc. A monitor must be connected in order to change BIOS settings.
5. **Connect and turn on PSU**
   Connect PSU to the board by the 2x12-pin ATX wafer connector and 2x2-pin ATX wafer connector.
6. **BIOS setup**
   Enter the BIOS setup by pressing the <DEL> key during boot up.

   Enter "Exit Menu" and Load Setup Defaults.

   Refer to the "BIOS Configuration / Setup" section of this manual for details on BIOS setup.

**To clear all BIOS setting, including Password protection, activate "Clear CMOS Jumper" for 10 sec (without power connected).**

7. Mounting the board in chassis

**NOTICE**

**When mounting the board to chassis etc. please note that the board contains components on both sides of the PCB that can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.**

When fixing the board on a chassis, it is recommended to use screws with an integrated washer and a diameter of > 7 mm. Do not use washers with teeth, as they can damage the PCB and cause short circuits.

## 2.2. Chassis Safety Standards

Before installing the MITX-CFL0 Series in the chassis, users must evaluate the end product to ensure compliance with the requirements of the IEC60950-1 safety standard:

- The board must be installed in a suitable mechanical, electrical and fire enclosure.
- The system, in its enclosure, must be evaluated for temperature and airflow considerations.
- The board must be powered by a CSA or UL approved power supply that limits the maximum input current.
- For interfaces having a power pin such as external power or fan, ensure that the connectors and wires are suitably rated. All connections from and to the product shall be with SELV circuits only.
- Wires have suitable rating to withstand the maximum available power.
- The peripheral device enclosure fulfils the IEC60950-1 fire protecting requirements.

## 2.3. Lithium Battery Replacement

If replacing the lithium battery follow the replacement precautions stated in the notification below:

**⚠CAUTION**

**Danger of explosion if the lithium battery is incorrectly replaced.**

- Replace only with the same or equivalent type recommended by the manufacturer
- Dispose of used batteries according to the manufacturer's instructions

**VORSICHT! Explosionsgefahr bei unsachgemäßem Austausch der Batterie.**

- Ersatz nur durch denselben oder einen vom Hersteller empfohlenen gleichwertigen Typ
- Entsorgung gebrauchter Batterien nach Angaben des Herstellers

**ATTENTION! Risque d'explosion avec l'échange inadéquat de la batterie.**

- Remplacement seulement par le même ou un type équivalent recommandé par le producteur
- L'évacuation des batteries usagées conformément à des indications du fabricant

**PRECAUCION! Peligro de explosión si la batería se sustituye incorrectamente.**

- Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante

- Disponga las baterías usadas según las instrucciones del fabricante

**ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering.**

- Udskiftning må kun ske med batteri af samme fabrikat og type
- Levér det brugte batteri tilbage til leverandøren

**ADVARSEL! Eksplosjonsfare ved feilaktig skifte av batteri.**

- Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten
- Brukte batterier kasseres i henhold til fabrikantens instruksjoner

**VARNING! Explosionsfara vid felaktigt batteribyte.**

- Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren
- Kassera använt batteri enligt fabrikantens instruktion

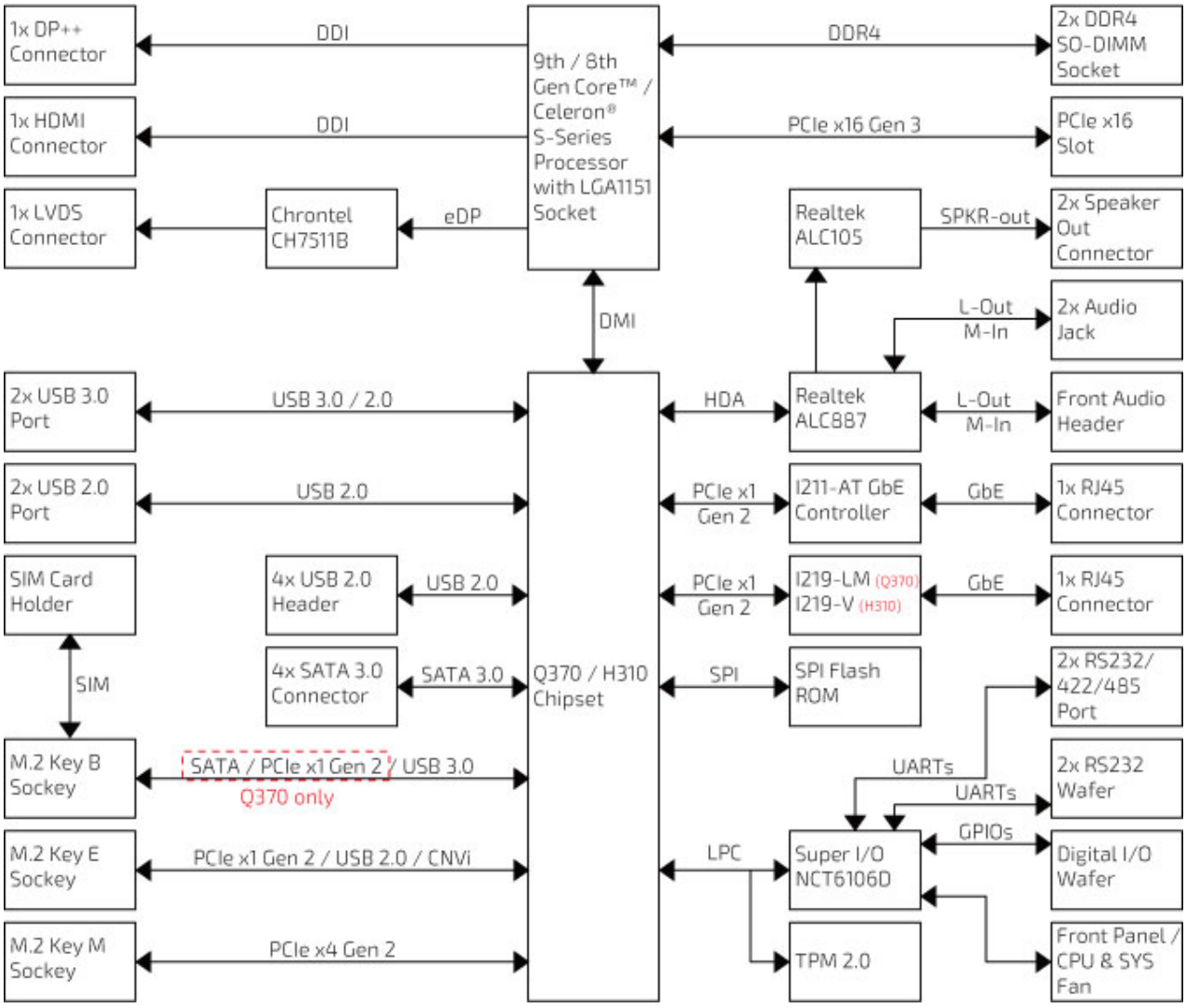
**VAROITUS! Paristo voi räjähtää, jos se on virheellisesti asennettu.**

- Vaihda paristo ainoastaan lalteval- mistajan suosittelemaan tyyppiln
- Hävitä käytetty paristo valmistajan ohjeiden mukaisesti

# 3/ System Specifications

## 3.1. System Block Diagram

Figure 1: System Block Diagram MITX-CFL0 Series



## 3.2. Scope of Delivery

The table below summarizes the features of the MITX-CFL0 Series motherboard.

**Table 1: Component Main Data**

| | |
|---|---|
| **System** | |
| **Processor** | ▶ 9th Generation Intel® Core™ S-Series (LGA1151 socket, up to 65 W TDP)<br>▶ 8th Generation Intel® Core™ S-Series (LGA1151 socket, up to 65 W TDP)<br>▶ Intel® Celeron® G4900 Series (LGA1151 socket, up to 65 W TDP) |
| **Chipset** | ▶ Intel® Q370<br>▶ Intel® H310 |
| **Memory** | ▶ 2x DDR4 SO-DIMM memory socket |
| **Video** | |
| **Display Interface** | ▶ 1x LVDS<br>▶ 1x DP++ (on rear)<br>▶ 1x HDMI 2.0 (on rear) |
| **Multiple Display** | ▶ Triple (Q370)<br>▶ Dual (H310) |
| **Audio** | |
| **Audio Codec** | ▶ Realtek ALC887 |
| **Audio Interface** | ▶ 2x Speaker-out (3 W, by header)<br>▶ 2x Line-out (1x on rear, 1x by header)<br>▶ 2x Mic-in (1x on rear, 1x by header) |
| **Network Connection** | |
| **Ethernet** | ▶ 2x GbE LAN (RJ45 on rear, 1x Intel® I211-AT, 1x Intel® I219-LM (Q370) / I219-V (H310)) |
| **Peripheral Connection** | |
| **USB** | ▶ 2x USB 3.0 (Type A on rear)<br>▶ 6x USB 2.0 (2x Type A on rear, 4x by header) |
| **Serial Port** | ▶ 2x RS232/422/485 (DB9 on rear)<br>▶ 4x RS232 (by header) |
| **Other I/Os** | ▶ 8-bit DIO (by header)<br>▶ 1x I2C (by header) |
| **Storage & Expansion** | |
| **Storage & Expansion** | ▶ 4x SATA 3.0<br>▶ 1x M.2 Key B (type 2242 / 3042 / 2280, w/ SATA / PCIe x1 / USB 3.0 for Q370)<br>▶ 1x M.2 Key B (type 2242 / 3042 / 2280, w/ USB 3.0 for H310)<br>▶ 1x M.2 Key E (type 2230, w/ PCIe x1 / USB 2.0, CNVi support)<br>▶ 1x M.2 Key M (type 2242 / 2280, mixed w/ PCIe x4)<br>▶ 1x PCIe x16 (one x16 signal for H310 / one x16 or two x8 signal for Q370)<br>▶ 1x Micro SIM Card Cage (connected to M.2 Key B) |
| **Power** | |

| System | |
|---|---|
| Input Voltage | DC +5 V / +12 V / -12 V / +3.3 V / 5 VSB<br>DC 12 V |
| Connector | 2x12-pin ATX connector (DC +5 V / +12 V / -12 V / +3.3 V / 5 VSB)<br>2x2-pin ATX connector (DC 12 V) |
| **Firmware** | |
| BIOS | AMI uEFI BIOS w/ 128 Mb SPI Flash |
| Watchdog | Programmable WDT to generate system reset event |
| H/W Monitor | Input & Core Voltages<br>CPU & System Temperatures |
| Real Time Clock | Chipset integrated RTC |
| TPM | TPM 2.0 support (Infineon SLB 9665) |
| **System Control & Monitoring** | |
| Button, Switch & Indicator | 1x Standby LED (onboard)<br>1x Boot LED (onboard) |
| Front Panel Header | 1x Header for Reset button, HDD LED & External Speaker<br>1x Header for Power button, Power LED & SM bus<br>1x Header for Volume Control<br>1x Header for Chassis Intrusion Detection |
| **Cooling** | |
| Cooling Method | 1x Wafer for CPU Smart Fan<br>1x Wafer for System Smart Fan |
| **Software** | |
| OS Support | Windows 10 |
| **Mechanical** | |
| Dimension (L x W) | Mini-ITX (170 mm x 170 mm / 6.70" x 6.70") |

## 3.3. Environmental Conditions

The MITX-CFL0 Series is compliant with the following environmental conditions. It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within the allowed temperature range.

Table 2: Environmental Conditions

| | |
|---|---|
| Operating Temperature | 0 °C ~ 60 °C / 32 °F ~ 140 °F |
| Storage Temperature | -20 °C ~ 80 °C / -4 °F ~ 176 °F |
| Humidity | 0 % ~ 95 % |

## 3.4. Standards and Certifications

The MITX-CFL0 Series meets the following standards and certification tests.

**Table 3: Standards and Certifications**

| | |
|---|---|
| **CE Class A** | TBD |
| **FCC Class A** | TBD |

## 3.5. Processor Support

The MITX-CFL0 Series is designed to support the following processors which are connected to a discrete Intel® Q370 or H310 Chipset Platform Controller Hub on the motherboard.

- 9th Generation Intel® Core™ S-Series (FCLGA1151 socket, up to 65 W TDP)
- 8th Generation Intel® Core™ S-Series (FCLGA1151 socket, up to 65 W TDP)
- Intel® Celeron® G4900 Series (FCLGA1151 socket, up to 65 W TDP)

Sufficient cooling must be applied to the APU in order to remove the effect defined as TDP (Thermal Design Power). The sufficient cooling is also depending on the worst case maximum ambient operating temperature and the actual worst case load of processor.

## 3.6. System Memory Support

The MITX-CFL0 Series has two DDR4 SO-DIMM sockets. The sockets support the following memory features:

- 2x DDR4 SO-DIMM, 1.2 V
- Up to 32 GB (2x 16 GB)
- Dual channel, 260-pin, 2666 MT/s (Core™ i9 / i7 / i5) or 2400 MT/s (Core™ i3 / Celeron®)
- SPD timing supported
- ECC not supported

The installed DDR4 SO-DIMM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted, or the board may not be able to boot totally.

### 3.6.1. Memory Operating Frequencies

In all modes, the frequency of system memory is the lowest frequency of all the memory modules placed in the system. Each memory module's frequency can be determined through the SPD registers on the memory modules.

The table below lists the resulting operating memory frequencies based on the combination of SO-DIMMs and processor.

Table 4: Memory Operating Frequencies

| SO-DIMM Type | Module Name | Memory Data Transfer (MT/s) | Processor System Bus Frequency (MHz) | Resulting Memory Clock Frequency (MHz) | Peak Transfer Rate (MB/s) |
|---|---|---|---|---|---|
| DDR4 2666 | PC4-21333 | 2667 | 1333 | 333 | 21333 |
| DDR4 2400 | PC4-19200 | 2400 | 1200 | 300 | 19200 |

Memory modules have in general a much lower longevity than embedded motherboards, and therefore EOL of modules can be expected several times during lifetime of the motherboard.

As a minimum it is recommend using Kontron memory modules for prototype system(s) in order to prove stability of the system and as for reference.

For volume production you might request to test and qualify other types of RAM. In order to qualify RAM it is recommend configuring 3 systems running RAM Stress Test program in heat chamber at 60° C for a minimum of 24 hours.

## 3.7. On-board Graphics Subsystem

The MITX-CFL0 Series supports Intel® UHD Graphics technology for high quality graphics capabilities. The model with Intel® Q370 chipset supports three displays pipes while that with Intel® H310 chipset supports two displays pipes.

Up to three displays can be used simultaneously and be used to implement independent or cloned display configuration.

Table 5: Three-displays Configurations

| Display 1 | Display 2 | Display 3 | Max. Resolution (Px) at 60 Hz | | |
|---|---|---|---|---|---|
| | | | Display 1 | Display 2 | Display 3 |
| LVDS | DP++ | HDMI 2.0 | 1920 x 1200 | 4096 x 2304 | 3840 x 2160 |

## 3.8. Power Supply Voltage

In order to ensure safe operation of the board, the input power supply must monitor the supply voltage and shut down if the supply is out of range – refer to the actual power supply specification. Please note, in order to keep the power consumption to a minimal level, boards do not implement a guaranteed minimum load. In some cases, this can lead to compatibility problems with ATX power supplies that require a minimum load to stay in regulation. The MITX-CFL0 Series board must be powered through the ATX-24p (24-pole) connector using standard ATX power supply and through the ATX+12V-4p (4-pole) connector using standard ATX12V power supply.

**ATX supply: ATX-24p connector must be used in according to the ATX PSU standard.**

**ATX12V supply: ATX+12V-4p connector must be used in according to the ATX12V PSU standard.**

***NOTICE***

**Hot Plugging power supply is not supported. Hot plugging might damage the board.**

The requirements to the voltages of ATX power supply are as follows:

Table 6: Supply Voltages

| Supply | Min. | Max. | Note |
|---|---|---|---|
| +3.3 V | 3.135 V | 3.265 V | Should be ±5 % for compliance with the ATX specification |
| +5 V | 4.75 V | 5.25 V | Should be ±5 % for compliance with the ATX specification.<br>Should be minimum 5.00 V measured at USB connectors in order to meet the requirements of USB standard. |
| +12 V | 11.4 V | 12.6 V | Should be ±5 % for compliance with the ATX specification |
| -12 V | -13.2 V | -10.8 V | Should be ±10 % for compliance with the ATX specification |
| 5 VSB | 4.75 V | 5.25 V | Should be ±5 % for compliance with the ATX specification |

# 4/ Connector Locations

## 4.1. Top Side

Figure 2: Top Side

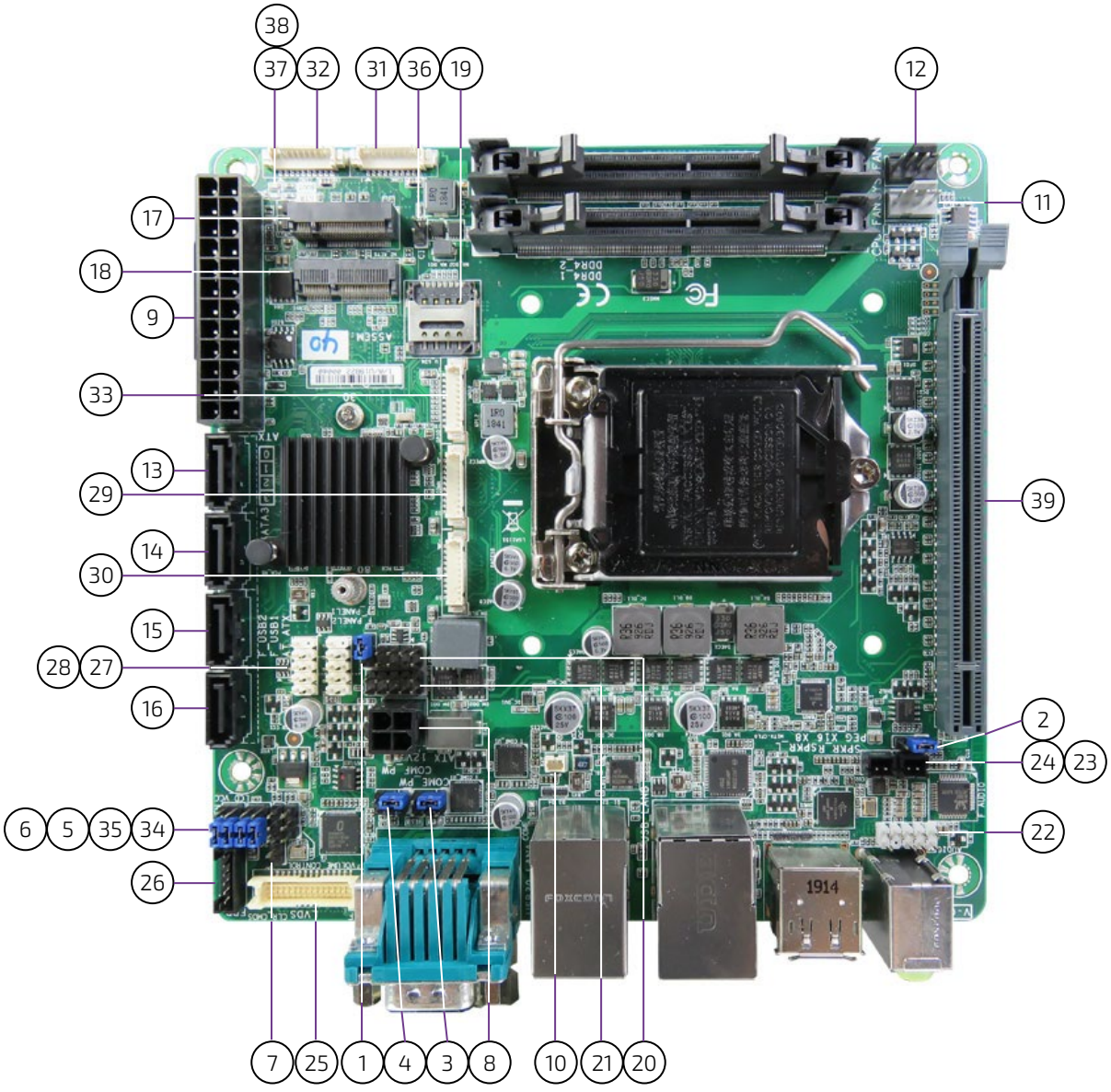



Table 7: Jumper List

| Item | Designation | Description | See Chapter |
|---|---|---|---|
| 1 | AT_ATX | AT / ATX Power Mode Selection | 7.21.1 |
| 2 | PEG_X16_X8 | PCIe Configuration Setting for PCIEX16 | 7.21.2 |
| 3 | COME_PW | Pin-9 Power Selection for COM 5 | 7.21.3 |
| 4 | COMF_PW | Pin-9 Power Selection for COM 6 | 7.21.3 |
| 5 | LCD_VCC | Panel & Backlight Power Selection for LVDS | 7.21.4 |

| Item | Designation | Description | See Chapter |
|---|---|---|---|
| 6 | BL_EN | Backlight Power Enable Selection for LVDS | 7.21.5 |
| 7 | CLR_CMOS | Clear CMOS Selection | 7.21.6 |

**Table 8: Top Side Internal Connector Pin Assignment**

| Item | Designation | Description | See Chapter |
|---|---|---|---|
| 8 | ATX_12V | 2x2-pin ATX Power Supply Wafer | 7.1.2 |
| 9 | ATX | 2x12-pin ATX Power Supply Wafer | 7.1.1 |
| 10 | BAT | RTC Power Input Wafer | 7.1.3 |
| 11 | CPU_FAN | CPU FAN Wafer | 7.2 |
| 12 | SYS_FAN | System FAN Wafer | 7.2 |
| 13 | SATA3_0 | Serial ATA 3.0 Port-0 Connector | 7.3 |
| 14 | SATA3_1 | Serial ATA 3.0 Port-1 Connector | 7.3 |
| 15 | SATA3_2 | Serial ATA 3.0 Port-2 Connector | 7.3 |
| 16 | SATA3_3 | Serial ATA 3.0 Port-3 Connector | 7.3 |
| 17 | M2_KEYB | M.2 Key B Socket | 7.12 |
| 18 | - | M.2 Key E Socket | 7.13 |
| 19 | U_SIM | Micro SIM Interface Slot for M.2 Key B | 7.15 |
| 20 | F_PANEL1 | Front Panel 1 Pin Header | 7.7 |
| 21 | F_PANEL2 | Front Panel 2 Pin Header | 7.7 |
| 22 | F_AUDIO | Front Panel Audio Pin Header | 7.6 |
| 23 | SPKR_R | Right Channel 3W Audio AMP Output Wafer | 7.5 |
| 24 | SPKR_L | Left Channel 3W Audio AMP Output Wafer | 7.5 |
| 25 | LVDS | Primary 24-bit, 2-channel LVDS Panel Connector | 7.9 |
| 26 | FPD | Panel Backlight Wafer for LVDS | 7.10 |
| 27 | F_USB1 | USB 2.0 Port 4 & Port 5 Pin Header | 7.4 |
| 28 | F_USB2 | USB 2.0 Port 6 & Port 7 Pin Header | 7.4 |
| 29 | COMA | RS232 Port 1 Wafer | 7.8 |
| 30 | COMB | RS232 Port 2 Wafer | 7.8 |
| 31 | COMC | RS232 Port 3 Wafer | 7.8 |
| 32 | COMD | RS232 Port 4 Wafer | 7.8 |
| 33 | GPIO | Digital Input / Output Wafer | 7.11 |
| 34 | VOLUME_CONTROL | Volume Control Pin Header | 7.17 |
| 35 | I2C | I2C (Inter-Integrated Circuit) Pin Header | 7.18 |
| 36 | CI | Chassis Intrusion Pin Header | 7.19 |
| 37 | STB | Standby Status LED | 7.20 |
| 38 | BOOT | Boot Status LED | 7.20 |
| 39 | PCIEX16 | PCI Express x16 Slot | 7.16 |

## 4.2. Bottom Side

Figure 3: Bottom Side

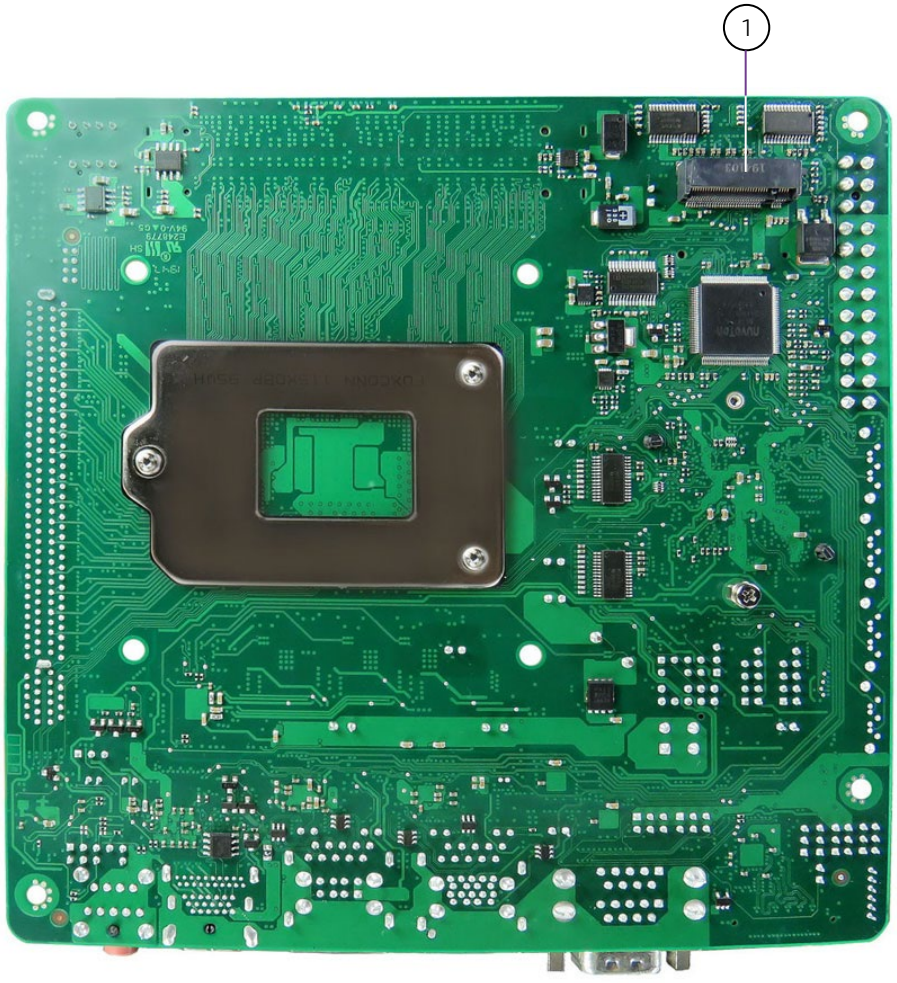



Table 9: Bottom Side Internal Connector Pin Assignment

| Item | Designation | Description | See Chapter |
|---|---|---|---|
| 1 | - | M.2 Key M Socket | 7.14 |

## 4.3. Connector Panel Side

Figure 4: Connector Panel Side

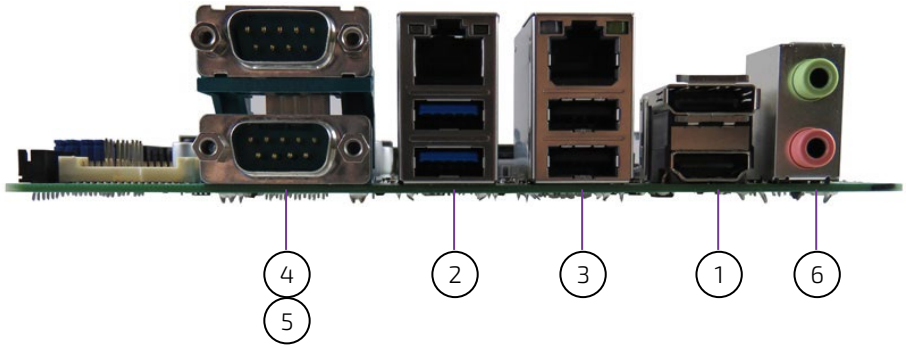



Table 10: Connector Panel Side Connector List

| Item | Designation | Description | See Chapter |
|---|---|---|---|
| 1 | DP_HDMI | DP++ & HDMI 2.0 Connector | 6.1 & 6.2 |
| 2 | USB30_LANA | GbE LAN A & USB 3.0 Port-0, 1 Connector | 6.3 & 6.4 |
| 3 | USB_LANB | GbE LAN B & USB 2.0 Port-2, 3 Connector | 6.3 & 6.4 |
| 4 | COME | RS232/422/485 COM 5 Connector | 6.5 |
| 5 | COMF | RS232/422/485 COM 6 Connector | 6.5 |
| 6 | AUDIO | Line-Out & Mic-In Audio Jacks | 6.6 |

# 5/ Connector Definitions

The following defined terms are used within this user guide to give more information concerning the pin assignment and to describe the connector's signals.

| Defined Term | Description |
|---|---|
| **Pin** | Shows the pin numbers in the connector |
| **Signal** | The abbreviated name of the signal at the current pin<br>The notation "XX#" states that the signal "XX" is active low |
| **Note** | Special remarks concerning the signal |
| **Designation** | Type and number of item described |
| **See Chapter** | Number of the chapter within this user guide containing a detailed description |

The abbreviation TBD is used for specifications that are not available yet or which are not sufficiently specified by the component vendors.

# 6/ I/O-Area Connectors

## 6.1. DP++ Connector (DP_HDMI Top)

The DP++ (Dual-mode DisplayPort) connector is based on standard DP female port. The port allows users to use a passive adapter to convert DP signals to single-link DVI or HDMI.

**Figure 5: DP++ Connector DP_HDMI Top**

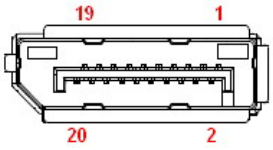



**Table 11: Pin Assignment DP++ Connector DP_HDMI Top**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | TX0+ | DisplayPort Lane 0 transmitter differential pair (+) | |
| 2 | GND | Ground | |
| 3 | TX0- | DisplayPort Lane 0 transmitter differential pair (-) | |
| 4 | TX1+ | DisplayPort Lane 1 transmitter differential pair (+) | |
| 5 | GND | Ground | |
| 6 | TX1- | DisplayPort Lane 1 transmitter differential pair (-) | |
| 7 | TX2+ | DisplayPort Lane 2 transmitter differential pair (+) | |
| 8 | GND | Ground | |
| 9 | TX2- | DisplayPort Lane 2 transmitter differential pair (-) | |
| 10 | TX3+ | DisplayPort Lane 3 transmitter differential pair (+) | |
| 11 | GND | Ground | |
| 12 | TX3- | DisplayPort Lane 3 transmitter differential pair (-) | |
| 13 | GND | Ground | |
| 14 | GND | Ground | |
| 15 | AUX+ | DisplayPort Auxiliary channel differential pair (+) | |
| 16 | GND | Ground | |
| 17 | AUX- | DisplayPort Auxiliary channel differential pair (-) | |
| 18 | HPD | DisplayPort hot plug detect | |
| 19 | GND | Ground | |
| 20 | PWR | Power for connector | |

## 6.2. HDMI Connector (DP_HDMI Bottom)

The HDMI connector is based on standard HDMI type A and compliant with HDMI 2.0.

**Figure 6: HDMI Connector DP_HDMI Bottom**

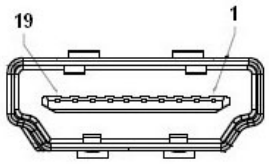



**Table 12: Pin Assignment HDMI Connector DP_HDMI Bottom**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | TMD_Data2+ | HDMI Lane 2 differential pair (+) | |
| 2 | GND | Ground | |
| 3 | TMD_Data2- | HDMI Lane 2 differential pair (-) | |
| 4 | TMD_Data1+ | HDMI Lane 1 differential pair (+) | |
| 5 | GND | Ground | |
| 6 | TMD_Data1- | HDMI Lane 1 differential pair (-) | |
| 7 | TMD_Data0+ | HDMI Lane 0 differential pair (+) | |
| 8 | GND | Ground | |
| 9 | TMD_Data0- | HDMI Lane 0 differential pair (-) | |
| 10 | TMD_CLK+ | HDMI Clock differential pair (+) | |
| 11 | GND | Ground | |
| 12 | TMD_CLK- | HDMI Clock differential pair (-) | |
| 13 | Reserved | | |
| 14 | Reserved | | |
| 15 | DDC_CLK | DDC based control signal (clock) | |
| 16 | DDC_DATA | DDC based control signal (data) | |
| 17 | GND | Ground | |
| 18 | 5V | +5 V power supply | |
| 19 | HPET | Hot Plug Detect | |

## 6.3. Ethernet Connectors (USB30_LANA LAN A & USB_LANB LAN B)

The MITX-CFL0 Series supports two channels of 10/100/1000 Mbit Ethernet, which are based Intel® I211-AT and Intel® I219-LM (model with Q370 chipset) / Intel® I219-LM (model with H310 chipset) controllers.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100 MByte and Category 5E, 6 or 6E with 1 Gbit LAN networks.

The signals for the Ethernet ports are as follows:

**Figure 7: Ethernet Connectors USB30_LANA LAB A, USB_LANB LAN B**

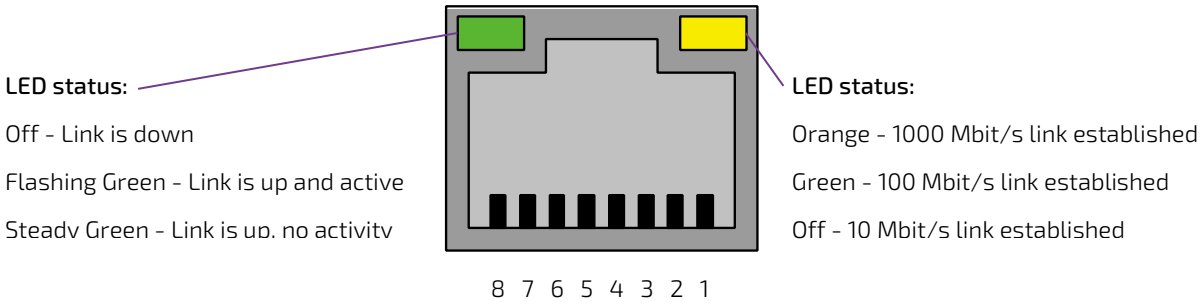



**Table 13: Pin Assignment Ethernet Connectors USB30_LANA LAN A, USB30_LANB LAN B**

| Pin | Signal | Note |
|---|---|---|
| 1 | TX1+ | |
| 2 | TX1- | |
| 3 | TX2+ | |
| 4 | TX3+ | |
| 5 | TX3- | |
| 6 | TX2- | |
| 7 | TX4+ | |
| 8 | TX4- | |

### Signal Description

| Signal | Description |
|---|---|
| **TX1+ / TX1-** | In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. |
| **TX2+ / TX2-** | In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. |
| **TX3+ / TX3-** | In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair. |
| **TX4+ / TX4-** | In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair.In MDI crossover mode, this pair acts as the BI_DC+/- pair. |

'MDI' – media dependent Interface

## 6.4. USB Connectors (I/O Area)

The external I/O connector panel supports two USB 2.0 connectors and two USB 3.0 connectors.

**USB 3.0 ports are backward compatible with USB 2.0.**

Figure 8: USB 2.0 Connectors USB_LANB USB 2.0 Port 2 / 3

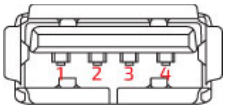



Table 14: Pin Assignment USB 2.0 Connectors USB_LANB USB 2.0 Port 2 / 3

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | +USBVCC | +5 V power supply for USB device | |
| 2 | USB_D- | USB 2.0 differential pair (-) | |
| 3 | USB_D+ | USB 2.0 differential pair (+) | |
| 4 | GND | Ground | |

Figure 9: USB 3.0 Connector USB30_LANA USB 3.0 Port 0 / 1

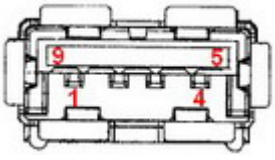
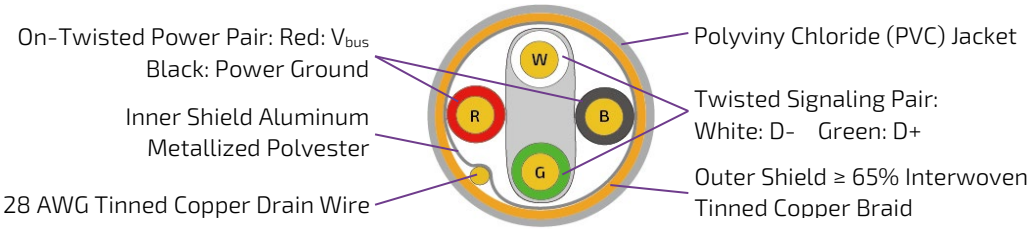



Table 15: Pin Assignment USB 3.0 Connector USB30_LANA USB 3.0 Port 0 / 1

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | +USBVCC | +5 V power supply for USB device | |
| 2 | USB_D- | USB 2.0 differential pair (-) | |
| 3 | USB_D+ | USB 2.0 differential pair (+) | |
| 4 | GND | Ground | |
| 5 | USB3_SSRX- | USB 3.0 receiver differential pair (-) | |
| 6 | USB3_SSRX+ | USB 3.0 receiver differential pair (+) | |
| 7 | GND | Ground | |
| 8 | USB3_SSTX- | USB 3.0 transmitter differential pair (-) | |
| 9 | USB3_SSTX+ | USB 3.0 transmitter differential pair (+) | |

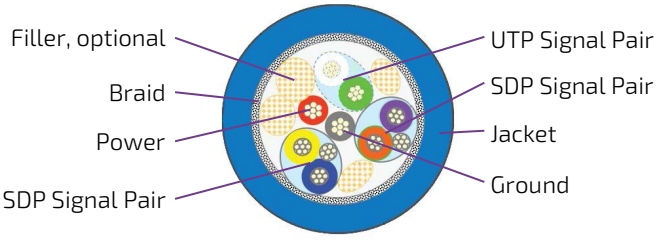
For HiSpeed rates it is required to use a USB cable, which is specified in USB 2.0 standard:

**Figure 10: USB 2.0 High Speed Cable**




For USB 3.0 cabling it is required to use only HiSpeed USB cable, specified in USB3.0 standard:

**Figure 11: USB 3.0 High Speed Cable**



## 6.5. Serial COM 5 & COM 6 Ports (COME & COMF)

The external I/O connector panel supports one dual DB-9 RS232/422/485 COM male ports.

Figure 12: Serial COM 5 & COM 6 Ports COME, COMF

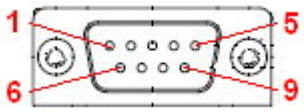



Table 16: Pin Assignment COM 5 & COM 6 Ports COME, COMF

| Pin | RS232 Signal | RS422 Signal | Half Duplex RS485 Signal | Full Duplex RS485 Signal | Note |
|---|---|---|---|---|---|
| 1 | DCD | TX- | DATA- | TX- | |
| 2 | RXD | RX+ | N/A | RX+ | |
| 3 | TXD | TX+ | DATA+ | TX+ | |
| 4 | DTR | RX- | N/A | RX- | |
| 5 | GND | GND | GND | GND | |
| 6 | DSR | N/A | N/A | N/A | |
| 7 | RTS | N/A | N/A | N/A | |
| 8 | CTS | N/A | N/A | N/A | |
| 9 | RI* | N/A | N/A | N/A | |

*: Pin configuration can be selected by Jumper COME_PW (for COM 5) and COMF_PW (for COM 6).

RS232, RS422 and RS485 can be selected in BIOS setup.

Table 17: Signal Description

| Signal | Description |
|---|---|
| TXD | Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12 V) on hardware reset when the transmitter is empty or when loop mode operation is initiated. |
| RXD | Received Data, receives data from the communications link. |
| DTR | Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to establish communication link. |
| DSR | Data Set Ready, indicates that the modem etc. is ready to establish a communications link. |
| RTS | Request To Send, indicates to the modem etc. that the on-board UART is ready to exchange data. |
| CTS | Clear To Send, indicates that the modem or data set is ready to exchange data. |
| DCD | Data Carrier Detect, indicates that the modem or data set has detected the data carrier. |

| Signal | Description |
|---|---|
| RI | Ring Indicator, indicates that the modem has received a ringing signal from the telephone line. |
| TX+/- | Transmitted data differential pair sends data to the communications link. |
| RX+/- | Received data differential pair receives data from the communications link. |
| Data+/- | Transmitted / received data differential pair either sends or receives data to the communications link at a time. |
| GND | Power Supply GND signal |

## 6.6. Audio Jack (AUDIO)

The external I/O connector panel supports one 3.5 mm dual-port Azalia audio phone jack for headset and microphone. The audio output signals are shared with those of the speaker connectors SPKR_R & SPKR_L.

Figure 13: Audio Jack Audio

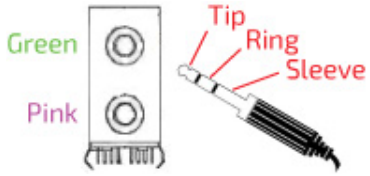



Table 18: Pin Assignment Audio Jack Audio

| Pin | Signal | Description | Note |
|---|---|---|---|
| **Top (Green)** | | | |
| Tip | Line-Out_L | Audio output left channel signal | |
| Ring | Line-Out_R | Audio output right channel signal | |
| Sleeve | GND | Ground | |
| **Bottom (Pink)** | | | |
| Tip | Mic-In_L | Microphone input left channel signal | |
| Ring | Mic-In_R | Microphone input right channel signal | |
| Sleeve | GND | Ground | |

# 7/ Internal Connectors

## 7.1. Power Connector

The MITX-CFL0 Series is designed to be supplied from a 2x12-pin ATX power supply and a 2x2-pin +12 VDC power supply.

**NOTICE**

**Hot plugging any of the power connector is not allowed.**

**Hot plugging might damage the board. In other words, turn off main supply etc. to make sure all the power lines are turned off when connecting to the motherboard.**

### 7.1.1. 2x12-pin ATX Power Supply Wafer (ATX)

The 2x12-pin ATX power supply wafer provides +5 V, +12 V, -12 V, +3.3 V and 5 VSB DC to the board.

**Figure 14: 2x12-pin ATX Power Supply Wafer ATX**

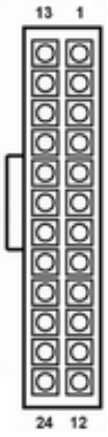



**Table 19: Pin Assignment ATX**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | +3.3V | Power +3.3 V | |
| 2 | +3.3V | Power +3.3 V | |
| 3 | GND | Ground | |
| 4 | +5V | Power +5 V | |
| 5 | GND | Ground | |
| 6 | +5V | Power +5 V | |
| 7 | GND | Ground | |
| 8 | Power Good | Power Good Signal | |
| 9 | +5VSB | +5 V Standby | |
| 10 | +12V | Power +12 V | |
| 11 | +12V | Power +12 V (only for 2x12-pin ATX) | |
| 12 | +3.3V | Power +3.3 V (only for 2x12-pin ATX) | |
| 13 | +3.3V | Power +3.3 V | |

| Pin | Signal | Description | Note |
|---|---|---|---|
| 14 | -12V | Power -12 V | |
| 15 | GND | Ground | |
| 16 | PS_ON | Soft Power On / Off | |
| 17 | GND | Ground | |
| 18 | GND | Ground | |
| 19 | GND | Ground | |
| 20 | NC | | |
| 21 | +5V | Power +5 V | |
| 22 | +5V | Power +5 V | |
| 23 | +5V | Power +5 V (only for 2x12-pin ATX) | |
| 24 | GND | Ground (only for 2x12-pin ATX) | |

### 7.1.2. 2x2-pin ATX Power Supply Wafer (ATX_12V)

The 2x2-pin ATX power supply wafer provides +12 V DC to the board.

**Figure 15: 2x2-pin ATX Power Supply Wafer ATX_12V**

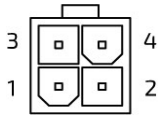



**Table 20: Pin Assignment ATX_12V**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | GND | Ground | |
| 2 | GND | Ground | |
| 3 | +12V | Power +12 V | |
| 4 | +12V | Power +12 V | |

### 7.1.3. RTC Power Input Wafer (BAT)

The 1x2-pin 1.25 mm pitch RTC power input wafer is intended to be connected to the battery. The battery provides power to the system clock to retain the time when power is turn off.

**Figure 16: RTC Power Input Wafer BAT**

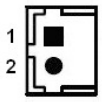



**Table 21: Pin Assignment BAT**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | RTC Power | Real-time clock backup battery input | |
| 2 | GND | Ground reference | |

## 7.2. Fan Wafers (CPU_FAN & SYS_FAN)

The CPU FAN Wafer (CPU_FAN) is used for the connection of the FAN for the CPU while the System FAN Wafer (SYS_FAN) for the connection of the FAN for the system.

**Figure 17: Fan Wafer CPU_FAN, SYS_FAN**

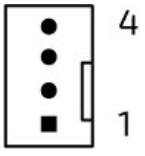



**Table 22: Pin Assignment CPU_FAN, SYS_FAN**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | GND | Power supply ground signal | |
| 2 | Voltage Speed Control | +12 V power supply for fan | |
| 3 | SENSE | Sense input signal from the fan, for rotation speed supervision RPM (Rotations Per Minute). | |
| 4 | PWM Speed Control | PWM output signal for FAN speed control | |

## 7.3. SATA 3.0 Port 0, Port 1, Port 2 & Port 3 Connectors (SATA3_0, SATA3_1, SATA3_2 & SATA3_3)

The SATA connectors (SATA3_0, SATA3_1, SATA3_2 & SATA3_3) supply the data connection for the SATA hard disk and are SATA 3.0 compatible. For power connection, users shall connect an adequate sata power cable from the power supply to the hard drive(s).

**Figure 18: SATA 3.0 Connector SATA3_0, SATA3_1, SATA3_2, SATA3_3**

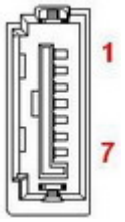



**Table 23: Pin Assignment SATA3_0, SATA3_1, SATA3_2, SATA3_3**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | GND | Ground | |
| 2 | TXP | Host transmitter differential signal pair (+) | |
| 3 | TXN | Host transmitter differential signal pair (-) | |
| 4 | GND | Ground | |
| 5 | RXN | Host receiver differential signal pair (-) | |
| 6 | RXP | Host receiver differential signal pair (+) | |
| 7 | GND | Ground | |

## 7.4. USB Connectors (Internal) (F_USB1 & F_USB2)

The USB port pin headers F_USB1 and F_USB2 support two USB 2.0 ports each.

**Figure 19: USB 2.0 Port Pin Header F_USB1, F_USB2**

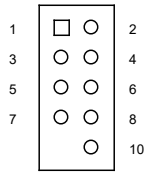



**Table 24: Pin Assignment F_USB1, F_USB2**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | Power (5V) | 5 V supply | |
| 2 | Power (5V) | 5 V supply | |
| 3 | USB DXA- | USB 2.0 differential pair (-) for channel X | |
| 4 | USB DY- | USB 2.0 differential pair (-) for channel Y | |
| 5 | USB DX+ | USB 2.0 differential pair (+) for channel X | |
| 6 | USB DY+ | USB 2.0 differential pair (+) for channel Y | |
| 7 | GND | Ground | |
| 8 | GND | Ground | |
| 9 | No Pin | | |
| 10 | NC | No connection | |

## 7.5. Speaker Connector (SPKR_R & SPKR_L)

The Speaker audio-out interface is available through the wafers SPKR_R and SPKR_L. These outputs are shared with the audio output (Line-out) signals of the audio jack AUDIO and the front panel audio pin header F_AUDIO.

**Figure 20: 3W Audio AMP Output Wafer SPKR_R (Right Channel), SPKR_L (Left Channel)**

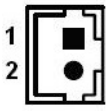



**Table 25: Pin Assignment SPKR_R, SPKR_L**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | Speaker+ | Speaker output (+) | |
| 2 | Speaker- | Speaker output (-) | |

## 7.6. Front Panel Audio Pin Header (F_AUDIO)

The front panel audio pin header F_AUDIO provides audio output (Line-Out) and microphone (Mic-In) signals. The audio output signals are shared with those of the speaker connectors SPKR_R & SPKR_L.

**Figure 21: Front Panel Audio Pin Header F_AUDIO**

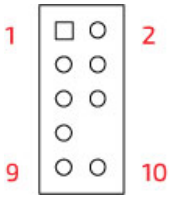



**Table 26: Pin Assignment F_AUDIO**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | MIC2-L | Microphone input left channel signal | |
| 2 | GND | Audio ground | |
| 3 | MIC2-R | Microphone input right channel signal | |
| 4 | -ACZ_DET | Active low when an Intel® HD Audio dongle is connected | |
| 5 | LINE2-R | Audio output right channel signal | |
| 6 | Sense | Jack detection for front panel microphone | |
| 7 | FAUDIO_JD | Front panel jack detect | |
| 8 | No Pin | | |
| 9 | LINE2-L | Audio output left channel signal | |
| 10 | Sense | Jack detection for front panel headphone | |

## 7.7. Front Panel Pin Header (F_PANEL1 & F_PANEL2)

The front panel connector F_PANEL1 supplies signals for the reset button, storage LED and system warning speaker.

The front panel connector F_PANEL2 supplies signals for the power button, power LED and SM Bus.

**Figure 22: Front Panel 1 Pin Header F_PANEL1**

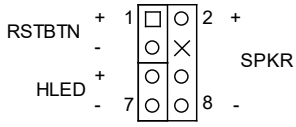



**Table 27: Pin Assignment F_PANEL1**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | Reset Button + | System reset button (+) | |
| 2 | Speaker + | External system warning speaker (+) | |
| 3 | Reset Button - | System reset button (-) | |
| 4 | No Pin | | |
| 5 | HDD LED + | HDD activity LED (+). The LED lights up or flashes when data is ready from or written to the HDD. | |
| 6 | NC | No connection | |
| 7 | HDD LED - | HDD activity LED (-). | |
| 8 | Speaker - | External system warning speaker (-) | |

**Figure 23: Front Panel 2 Pin Header F_PANEL2**

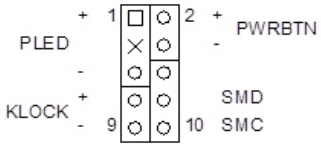



**Table 28: Pin Assignment F_PANEL2**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | Power LED + | System Power LED (+). The LED lights up when users turn on the system power, and blinks when the system is in sleep mode. | |
| 2 | Power Button + | System power button (+). Pressing the power button turns the system on or puts the system in sleep or soft-off mode depending on the operating system settings. Pressing the power switch for more than four seconds while the system turns from ON to OFF. | |
| 3 | No Pin | | |
| 4 | Power Button - | System power button (-). | |
| 5 | Power LED - | System Power LED (-). | |
| 6 | SMB_ALERT# | System management bus alert | |
| 7 | BATLOW# | Battery low input. This signal may be driven low by external | |

| Pin | Signal | Description | Note |
|---|---|---|---|
| | | circuitry to signal that the system battery is low. It also can be used to signal some other external power management event. | |
| 8 | SMBus Data | System management bus bidirectional data line | |
| 9 | GND | Ground | |
| 10 | SMBus Clock | System management bus bidirectional clock line | |

## 7.8. Serial COM 1 - COM 4 Ports (COMA, COMB, COMC & COMD)

The serial connections COMA, COMB, COMC and COMD provide RS232 connections.

Figure 24: Serial COM COMA, COMB, COMC, COMD

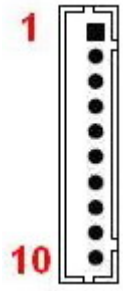



Table 29: Pin Assignment COMA, COMB, COMC, COMD

| Pin | RS232 Signal | Note |
|---|---|---|
| 1 | DCD | |
| 2 | DSR | |
| 3 | RXD | |
| 4 | RTS | |
| 5 | TXD | |
| 6 | CTS | |
| 7 | DTR | |
| 8 | RI | |
| 9 | GND | |
| 10 | +5V | |

The COM ports need to install an OS patch from ITE. The patch is only available for Windows and is not available Linux.

Table 30: Serial COM Signal Description

| Signal | Description |
|---|---|
| TXD | Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12 V) on hardware reset when the transmitter is empty or when loop mode operation is initiated. |
| RXD | Received Data, receives data from the communications link. |
| DTR | Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to establish communication link. |
| DSR | Data Set Ready, indicates that the modem etc. is ready to establish a communications link. |
| RTS | Request To Send, indicates to the modem etc. that the on-board UART is ready to exchange data. |
| CTS | Clear To Send, indicates that the modem or data set is ready to exchange data. |
| DCD | Data Carrier Detect, indicates that the modem or data set has detected the data carrier. |

| Signal | Description |
|---|---|
| **RI** | Ring Indicator, indicates that the modem has received a ringing signal from the telephone line. |
| **GND** | Power Supply GND signal |

## 7.9. LVDS Panel Connector (LVDS)

The 24-bit, 2-channel LVDS connector is based on 2x15-pin 1.25 mm pitch connector.

**Figure 25: LVDS Connector LVDS**

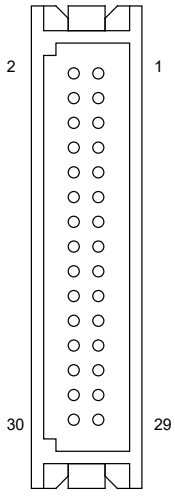



**Table 31: Pin Assignment LVDS**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | VDDEN | Output Display Enable | |
| 2 | GND | Ground | |
| 3 | +3.3V / +5V * | +3.3 V / +5 V power supply | |
| 4 | +3.3V / +5V * | +3.3 V / +5 V power supply | |
| 5 | TxclkA- | LVDS Channel A clock differential pair (-) | |
| 6 | TxclkB- | LVDS Channel B clock differential pair (-) | |
| 7 | TxclkA+ | LVDS Channel A clock differential pair (+) | |
| 8 | TxclkB+ | LVDS Channel B clock differential pair (+) | |
| 9 | GND | Ground | |
| 10 | GND | Ground | |
| 11 | TxoutA0- | LVDS Channel A Data 0 differential pair (-) | |
| 12 | TxoutB0- | LVDS Channel B Data 0 differential pair (-) | |
| 13 | TxoutA0+ | LVDS Channel A Data 0 differential pair (+) | |
| 14 | TxoutB0+ | LVDS Channel B Data 0 differential pair (+) | |
| 15 | TxoutA1- | LVDS Channel A Data 1 differential pair (-) | |
| 16 | TxoutB1- | LVDS Channel B Data 1 differential pair (-) | |
| 17 | TxoutA1+ | LVDS Channel A Data 1 differential pair (+) | |
| 18 | TxoutB1+ | LVDS Channel B Data 1 differential pair (-) | |
| 19 | TxoutA2- | LVDS Channel A Data 2 differential pair (-) | |
| 20 | TxoutB2- | LVDS Channel B Data 2 differential pair (-) | |
| 21 | TxoutA2+ | LVDS Channel A Data 2 differential pair (+) | |
| 22 | TxoutB2+ | LVDS Channel B Data 2 differential pair (+) | |

| Pin | Signal | Description | Note |
|---|---|---|---|
| 23 | TxoutA3- | LVDS Channel A Data 3 differential pair (-) | |
| 24 | TxoutB3- | LVDS Channel B Data 3 differential pair (-) | |
| 25 | TxoutA3+ | LVDS Channel A Data 3 differential pair (+) | |
| 26 | TxoutB3+ | LVDS Channel B Data 3 differential pair (+) | |
| 27 | GND | Ground | |
| 28 | GND | Ground | |
| 29 | DDC_SDA | DDC channel Data | |
| 30 | DDC_SCL | DDC Channel Clock | |

* **Panel power can be selected by Jumper LCD_VCC.**

## 7.10. Panel Backlight Wafer for LVDS (FPD)

The wafer FPD provides power supply for flat panel and its backlight inverter.

**Figure 26: Panel Backlight Wafer FPD**

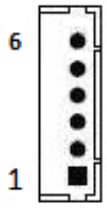



**Table 32: Pin Assignment FPD**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | BL_EN** | Backlight Enable signal | |
| 2 | BL_ADJ_PWM | Backlight Adjustment PWM (Pulse Width Modulation) signal | |
| 3 | +5V / +12V* | +5 V / +12 V power supply | |
| 4 | +5V / +12V* | +5 V / +12 V power supply | |
| 5 | GND | Ground | |
| 6 | GND | Ground | |

* Backlight Power can be selected by Jumper LCD_VCC.

** BL_EN can be selected by Jumper BL_EN.

## 7.11. Digital Input / Output Wafer (GPIO)

The wafer GPIO supports 8-bit digital input / output signals to provide powering-on function of the connected devices.

**Figure 27: Digital Input / Output Wafer GPIO**

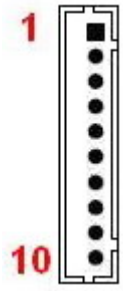



**Table 33: Pin Assignment GPIO**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | +5V | +5 V power supply | |
| 2 | DIO_0 | Digital input / output channel 0 | |
| 3 | DIO_1 | Digital input / output channel 1 | |
| 4 | DIO_2 | Digital input / output channel 2 | |
| 5 | DIO_3 | Digital input / output channel 3 | |
| 6 | DIO_4 | Digital input / output channel 4 | |
| 7 | DIO_5 | Digital input / output channel 5 | |
| 8 | DIO_6 | Digital input / output channel 6 | |
| 9 | DIO_7 | Digital input / output channel 7 | |
| 10 | GND | Ground | |

## 7.12. M.2 Key B Socket (M2_KEYB)

The MITX-CFL0 Series has an M.2 socket for a Type 2242 / 3042 / 2280 module. The M.2 Key B socket supports SATA 3.0, PCIe x1 and USB 3.0 signals for the model with Intel® Q370 chipset, and only USB 3.0 signals for the model with Intel® H310 chipset. The socket also supports USIM signals routed to the Micro SIM Interface Slot U_SIM, which makes it possible to use a WWAN wireless modem in this M.2 socket. For the model with SATA 3.0 / PCIe x1 signals support, it can be used for M.2 SSD installation as well.

Figure 28: M.2 Key B Socket M2_KEYB

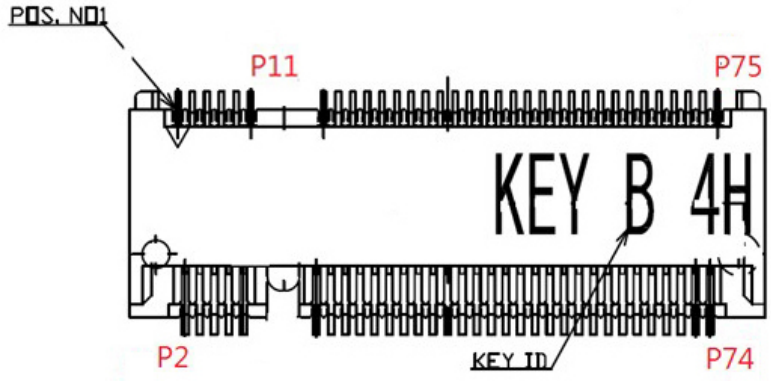



Table 34: Pin Assignment M2_KEYB

| Pin | Signal | Description |
|---|---|---|
| 1 | CONFIG3 | Define module type |
| 2 | +3.3V | 3.3 V power supply |
| 3 | GND | Ground |
| 4 | +3.3V | 3.3 V power supply |
| 5 | GND | Ground |
| 6 | FULL CARD PWR OFF | M.2 module power enable |
| 7 | USB-D+ | USB 2.0 differential pair (+) |
| 8 | W DISABLE#1 | Wireless disable 1 |
| 9 | USB-D- | USB 2.0 differential pair (-) |
| 10 | GPIO9 | |
| 11 | GND | Ground |
| 12 | KEY B | |
| 13 | KEY B | |
| 14 | KEY B | |
| 15 | KEY B | |
| 16 | KEY B | |
| 17 | KEY B | |
| 18 | KEY B | |
| 19 | KEY B | |
| 20 | NC | |
| 21 | CONFIG0 | Define module type |
| 22 | NC | |

| Pin | Signal | Description |
|---|---|---|
| 23 | NC | |
| 24 | NC | |
| 25 | NC | |
| 26 | NC | |
| 27 | GND | Ground |
| 28 | NC | |
| 29 | USB3.0_RX- | USB 3.0 receiver differential pair (-) |
| 30 | UIM RESET* | SIM card reset |
| 31 | USB3.0_RX+ | USB 3.0 receiver differential pair (+) |
| 32 | UIM CLK* | SIM card clock |
| 33 | GND | Ground |
| 34 | UIM DATA* | SIM card data |
| 35 | USB3.0_TX- | USB 3.0 transmitter differential pair (-) |
| 36 | UIM PWR* | SIM card power |
| 37 | USB3.0_TX+ | USB 3.0 transmitter differential pair (+) |
| 38 | DEVSLP | Device sleep |
| 39 | GND | Ground |
| 40 | NC | |
| 41 | PETn0/SATAB+/NC** | PCIe Lane 0 transmitter pair (-) / SATA transmitter differential pair (+) |
| 42 | NC | |
| 43 | PETp0/SATAB-/NC** | PCIe Lane 0 transmitter pair (+) / SATA transmitter differential pair (-) |
| 44 | NC | |
| 45 | GND | Ground |
| 46 | NC | |
| 47 | PERn0/SATAA-/NC** | PCIe Lane 0 receiver pair (-) / SATA receiver differential pair (-) |
| 48 | NC | |
| 49 | PERp0/SATAA+/NC** | PCIe Lane 0 receiver pair (+) / SATA receiver differential pair (+) |
| 50 | PERST | PCIe reset |
| 51 | GND | Ground |
| 52 | CLKREQ | Reference clock request signal |
| 53 | REFCLKN | PCIe reference clock pair (-) |
| 54 | PEWAKE | PCIe wake |
| 55 | REFCLKP | PCIe reference clock pair (+) |
| 56 | NC | |
| 57 | GND | Ground |
| 58 | NC | |
| 59 | NC | |
| 60 | NC | |
| 61 | NC | |
| 62 | NC | |
| 63 | NC | |
| 64 | NC | |

| Pin | Signal | Description |
|---|---|---|
| 65 | NC | |
| 66 | SIM DETECT | SIM card detect |
| 67 | NC | |
| 68 | SUSCLK | 32.768 kHz clock supply input |
| 69 | CONFIG1 | Define module type |
| 70 | +3.3V | 3.3 V power supply |
| 71 | GND | Ground |
| 72 | +3.3V | 3.3 V power supply |
| 73 | GND | Ground |
| 74 | +3.3V | 3.3 V power supply |
| 75 | CONFIG2 | Define module type |

* These pins are connected to SIM card connector U_SIM directly.

* NC for the model with Intel® H310 chipset.

## 7.13. M.2 Key E Socket

The MITX-CFL0 Series has an M.2 Key E socket for a Type 2230 module. The M.2 Key E socket supports PCIe x1, USB 2.0 and Intel® CNVi signals, allowing users to install a wireless module or an Intel® Wireless Companion RF module.

Figure 29: M.2 Key E Socket

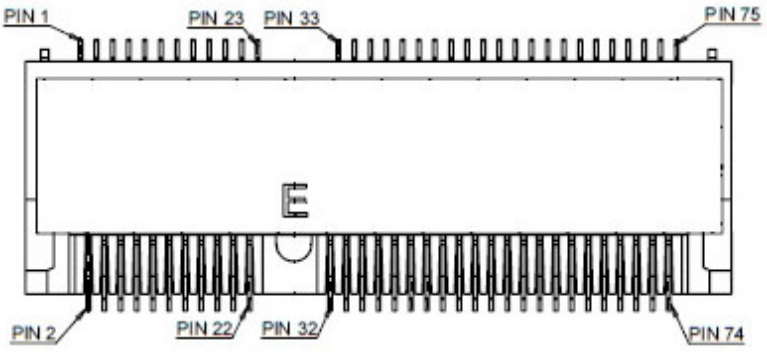



Table 35: Pin Assignment M.2 Key E Socket

| Pin | Key E* | | CNVi* | | Note |
|---|---|---|---|---|---|
| | Signal | Description | Signal | Description | |
| 1 | GND | Ground | GND | Ground | |
| 2 | +3.3V | 3.3 V power supply | +3.3V | 3.3 V power supply | |
| 3 | USB_D+ | USB 2.0 data diff. pair (+) | - | | |
| 4 | +3.3V | 3.3 V power supply | +3.3V | 3.3 V power supply | |
| 5 | USB_D- | USB 2.0 data diff. pair (-) | - | | |
| 6 | LED1# | Device active signal 1 | LED1# | Device active signal 1 | |
| 7 | GND | Ground | GND | Ground | |
| 8 | PCM_CLK | PCM synchronous data clock | - | | |
| 9 | - | | WGR_D1N | CNVio bus Rx Lane 1 (-) | |
| 10 | PCM_SYNC | PCM synchronous data sync | LCP_RSTN | RF companion (CRF) reset | |
| 11 | - | | WGR_D1P | CNVio bus Rx Lane 1 (+) | |
| 12 | PCM_IN | PCM synchronous data input | - | | |
| 13 | GND | Ground | GND | Ground | |
| 14 | PCM_OUT | PCM synchronous data output | CLKREQ0 | Clock request | |
| 15 | - | | WGR_D0N | CNVio bus Rx Lane 0 (-) | |
| 16 | LED2# | Device active signal 2 | LED2# | Device active signal 2 | |
| 17 | - | | WGR_D0P | CNVio bus Rx Lane 0 (+) | |
| 18 | GND | Ground | GND | Ground | |
| 19 | GND | Ground | GND | Ground | |
| 20 | UART_WAKE# | UART wake-up | - | | |
| 21 | - | | WGR_CLKN | CNVio bus Rx clock (-) | |
| 22 | UART_RX | UART data input | BRI_RSP | BRI bus Rx | |
| 23 | - | | WGR_CLKP | CNVio bus Rx clock (+) | |
| 24 | Key | | Key | | |

| Pin | Key E* | | CNVi* | | Note |
|---|---|---|---|---|---|
| | Signal | Description | Signal | Description | |
| 25 | Key | | Key | | |
| 26 | Key | | Key | | |
| 27 | Key | | Key | | |
| 28 | Key | | Key | | |
| 29 | Key | | Key | | |
| 30 | Key | | Key | | |
| 31 | Key | | Key | | |
| 32 | UART_TX | UART data output | RGI_DT | RGI bus Tx | |
| 33 | GND | Ground | GND | Ground | |
| 34 | UART_CTS | UART clear to send | RGI_RSP | RGI bus Rx | |
| 35 | PET0+ | PCIe Lane 0 Tx pair (+) | - | | |
| 36 | UART_RTS | UART request to send | BRI_DT | BRI bus Tx | |
| 37 | PET0- | PCIe Lane 0 Tx pair (-) | - | | |
| 38 | Clink_RST | Wi-Fi CLINK host bus reset | - | | |
| 39 | GND | Ground | GND | Ground | |
| 40 | Clink_DATA | Wi-Fi CLINK host bus data | - | | |
| 41 | PER0+ | PCIe Lane 0 Rx pair (+) | - | | |
| 42 | Clink_CLK | Wi-Fi CLINK host bus clock | - | | |
| 43 | PER0- | PCIe Lane 0 Rx pair (-) | - | | |
| 44 | - | | - | | |
| 45 | GND | Ground | GND | Ground | |
| 46 | - | | - | | |
| 47 | REFCLK0+ | PCIe reference clock pair (+) | - | | |
| 48 | - | | - | | |
| 49 | REFCLK0- | PCIe reference clock pair (-) | - | | |
| 50 | SUSCLK | 32.768 kHz clock supply input | USUCLK | 32.768 kHz clock supply input | |
| 51 | GND | Ground | GND | Ground | |
| 52 | PERST0# | PCIe reset | - | | |
| 53 | CLKREQ0# | Reference clock request signal | - | | |
| 54 | W_DISABLE2# | Wireless disable 2 | W_DISABLE2# | Wireless disable 2 | |
| 55 | PEWAKE0# | PCIe wake | - | | |
| 56 | W_DISABLE1# | Wireless disable 1 | W_DISABLE1# | Wireless disable 1 | |
| 57 | GND | Ground | GND | Ground | |
| 58 | - | | - | | |
| 59 | - | | WT_D1N | CNVio bus Tx Lane 1 (-) | |
| 60 | - | | - | | |
| 61 | - | | WT_D1P | CNVio bus Tx Lane 1 (+) | |
| 62 | - | | - | | |
| 63 | GND | Ground | GND | Ground | |
| 64 | - | | REFCLK0 | Reference clock | |
| 65 | - | | WT_D0N | CNVio bus Tx Lane 0 (-) | |

| Pin | Key E* | | CNVi* | | Note |
|---|---|---|---|---|---|
| | Signal | Description | Signal | Description | |
| 66 | - | | - | | |
| 67 | - | | WT_D0P | CNVio bus Tx Lane 0 (+) | |
| 68 | - | | - | | |
| 69 | GND | Ground | GND | Ground | |
| 70 | - | | - | | |
| 71 | - | | WT_CLKN | CNVio bus Tx clock (-) | |
| 72 | +3.3V | 3.3 V power supply | +3.3V | 3.3 V power supply | |
| 73 | - | | WT_CLKP | CNVio bus Tx clock (+) | |
| 74 | +3.3V | 3.3 V power supply | +3.3V | 3.3 V power supply | |
| 75 | GND | Ground | GND | Ground | |

## 7.14. M.2 Key M Socket

The MITX-CFL0 Series has an M.2 Key M socket for a Type 2242 / 2280 module. The M.2 Key M socket supports PCIe x4 signals, allowing users to install an M.2 PCIe SSD.

Figure 30: M.2 Key M Socket

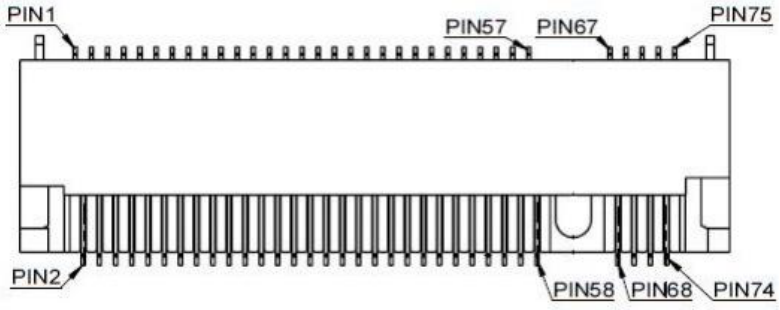



Table 36: Pin Assignment M.2 Key M Socket

| Pin | Signal | Description |
|---|---|---|
| 1 | GND | Ground |
| 2 | +3.3V | 3.3 V power supply |
| 3 | GND | Ground |
| 4 | +3.3V | 3.3 V power supply |
| 5 | PERn3 | PCIe Lane 3 receiver pair (-) |
| 6 | NC | |
| 7 | PERp3 | PCIe Lane 3 receiver pair (+) |
| 8 | NC | |
| 9 | GND | Ground |
| 10 | LED1# | Device active signal |
| 11 | PETn3 | PCIe Lane 3 transmitter pair (-) |
| 12 | +3.3V | 3.3 V power supply |
| 13 | PETp3 | PCIe Lane 3 transmitter pair (+) |
| 14 | +3.3V | 3.3 V power supply |
| 15 | GND | Ground |
| 16 | +3.3V | 3.3 V power supply |
| 17 | PERn2 | PCIe Lane 2 receiver pair (-) |
| 18 | +3.3V | 3.3 V power supply |
| 19 | PERp2 | PCIe Lane 2 receiver pair (+) |
| 20 | NC | |
| 21 | GND | Ground |
| 22 | NC | |
| 23 | PETn2 | PCIe Lane 2 transmitter pair (-) |
| 24 | NC | |
| 25 | PETp2 | PCIe Lane 2 transmitter pair (+) |
| 26 | NC | |

| Pin | Signal | Description |
|---|---|---|
| 27 | GND | Ground |
| 28 | NC | |
| 29 | PETn1 | PCIe Lane 1 transmitter pair (-) |
| 30 | NC | |
| 31 | PETp1 | PCIe Lane 1 transmitter pair (+) |
| 32 | NC | |
| 33 | GND | Ground |
| 34 | NC | |
| 35 | PERn1 | PCIe Lane 1 receiver pair (-) |
| 36 | NC | |
| 37 | PERp1 | PCIe Lane 1 receiver pair (+) |
| 38 | DEVSLP | Device sleep |
| 39 | GND | Ground |
| 40 | NC | |
| 41 | PETn0/SATAB+ | PCIe Lane 0 transmitter pair (-) / SATA transmitter differential pair (+) |
| 42 | NC | |
| 43 | PETp0/SATAB- | PCIe Lane 0 transmitter pair (+) / SATA transmitter differential pair (-) |
| 44 | NC | |
| 45 | GND | Ground |
| 46 | NC | |
| 47 | PERn0/SATAA- | PCIe Lane 0 receiver pair (-) / SATA receiver differential pair (-) |
| 48 | NC | |
| 49 | PERp0/SATAA+ | PCIe Lane 0 receiver pair (+) / SATA receiver differential pair (+) |
| 50 | PERST | PCIe reset |
| 51 | GND | Ground |
| 52 | CLKREQ | Reference clock request signal |
| 53 | REFCLKN | PCIe reference clock pair (-) |
| 54 | PEWAKE | PCIe wake |
| 55 | REFCLKP | PCIe reference clock pair (+) |
| 56 | NC | |
| 57 | GND | Ground |
| 58 | NC | |
| 59 | KEY M | |
| 60 | KEY M | |
| 61 | KEY M | |
| 62 | KEY M | |
| 63 | KEY M | |
| 64 | KEY M | |
| 65 | KEY M | |
| 66 | KEY M | |
| 67 | NC | |
| 68 | SUSCLK | 32.768 kHz clock supply input |

| Pin | Signal | Description |
|---|---|---|
| 69 | GND | Ground |
| 70 | +3.3V | 3.3 V power supply |
| 71 | GND | Ground |
| 72 | +3.3V | 3.3 V power supply |
| 73 | GND | Ground |
| 74 | +3.3V | 3.3 V power supply |
| 75 | GND | Ground |

## 7.15. Micro SIM Interface Slot for M.2 Key B (U_SIM)

The push-push type Micro SIM card cage U_SIM is connected to M.2 Key B socket for Micro SIM card installation.

Figure 31: Micro SIM Interface Slot U_SIM

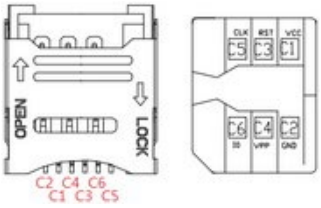



Table 37: Pin Assignment U_SIM

| Pin | Signal | Description | Note |
|---|---|---|---|
| C1 | VCC | Power +3.3 V | |
| C2 | GND | Ground | |
| C3 | RST | Reset signal | |
| C4 | VPP | Programming voltage input | |
| C5 | CLK | Clock signal | |
| C6 | IO | Input or Output for serial data | |

## 7.16. PCI Express x16 Slot (PCIEX16)

The MITX-CFL0 Series supports PCI Express x16 via slot PCIEX16. The model with Intel® Q370 Chipset supports PEG Bifurcation. PEG Bifurcation enables the PCI Expression lanes to be divided into:

- 2x PCIe x8

**The PEG Bifurcation can be configured by Jumper PEG_X16_X8**

**For PEG Bifurcation to function a PCIe Riser Card with bifurcation is required.**

The 16-lane (x16) PCI Express slot can be used for external PCI Express cards inclusive graphics card. The maximum theoretical bandwidth using 16 lane is 16 GB/s.

**Figure 32: PCIe x16 Slot Connector PCIEX16**

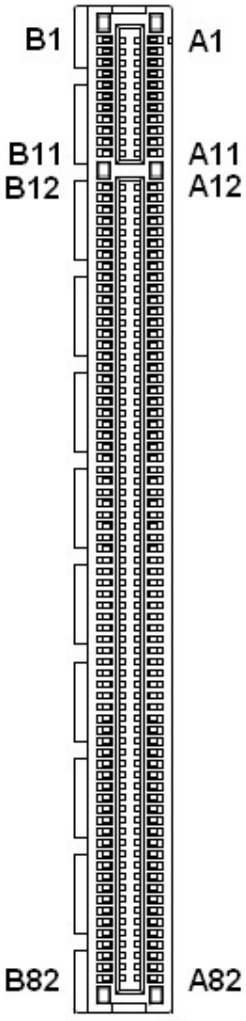


Table 38: Pin Assignment PCIEX16

| Pin | Side B | | Side A | |
|---|---|---|---|---|
| | Signal | Description | Signal | Description |
| 1 | +12V | +12 V power | PRSNT1# | Hot plug presence detect |
| 2 | +12V | +12 V power | +12V | +12 V power |
| 3 | Reserved | | +12V | +12 V power |
| 4 | Ground | | Ground | |
| 5 | SMCLK | SMBus clock | Reserved | |
| 6 | SMDAT | SMBus data | Reserved | |
| 7 | Ground | | Reserved | |
| 8 | +3.3V | +3.3 V power | Reserved | |
| 9 | Reserved | | +3.3V | +3.3 V power |
| 10 | +3.3VSB | +3.3 V standby power | +3.3V | +3.3 V power |
| 11 | WAKE# | Link reactivation | PERST# | PCI Express reser |
| Mechanical Key | | | | |
| 12 | Reserved | | Ground | |
| 13 | Ground | | REFCLK+ | Reference clock differential pair (+) |
| 14 | HSOP0 | Lane 0 transmitter differential pair (+) | REFCLK- | Reference clock differential pair (-) |
| 15 | HSON0 | Lane 0 transmitter differential pair (-) | Ground | |
| 16 | Ground | | HSIP0 | Lane 0 receiver differential pair (+) |
| 17 | PRSNT2# | Hot plug presence detect | HSIN0 | Lane 0 receiver differential pair (-) |
| 18 | Ground | | Ground | |
| 19 | HSOP1 | Lane 1 transmitter differential pair (+) | Reserved | |
| 20 | HSON1 | Lane 1 transmitter differential pair (-) | Ground | |
| 21 | Ground | | HSIP1 | Lane 1 receiver differential pair (+) |
| 22 | Ground | | HSIN1 | Lane 1 receiver differential pair (-) |
| 23 | HSOP2 | Lane 2 transmitter differential pair (+) | Ground | |
| 24 | HSON2 | Lane 2 transmitter differential pair (-) | Ground | |
| 25 | Ground | | HSIP2 | Lane 2 receiver differential pair (+) |
| 26 | Ground | | HSIN2 | Lane 2 receiver differential pair (-) |
| 27 | HSOP3 | Lane 3 transmitter differential pair (+) | Ground | |
| 28 | HSON3 | Lane 3 transmitter differential pair (-) | Ground | |
| 29 | Ground | | HSIP3 | Lane 3 receiver differential pair (+) |
| 30 | Reserved | | HSIN3 | Lane 3 receiver differential pair (-) |
| 31 | PRSNT2# | Hot plug presence detect | Ground | |
| 32 | Ground | | Reserved | |
| 33 | HSOP4 | Lane 4 transmitter differential pair (+) | Reserved | |
| 34 | HSON4 | Lane 4 transmitter differential pair (-) | Ground | |
| 35 | Ground | | HSIP4 | Lane 4 receiver differential pair (+) |
| 36 | Ground | | HSIN4 | Lane 4 receiver differential pair (-) |
| 37 | HSOP5 | Lane 5 transmitter differential pair (+) | Ground | |
| 38 | HSON5 | Lane 5 transmitter differential pair (-) | Ground | |

| Pin | Side B | | Side A | |
|---|---|---|---|---|
| | Signal | Description | Signal | Description |
| 39 | Ground | | HSIP5 | Lane 5 receiver differential pair (+) |
| 40 | Ground | | HSIN5 | Lane 5 receiver differential pair (-) |
| 41 | HSOP6 | Lane 6 transmitter differential pair (+) | Ground | |
| 42 | HSON6 | Lane 6 transmitter differential pair (-) | Ground | |
| 43 | Ground | | HSIP6 | Lane 6 receiver differential pair (+) |
| 44 | Ground | | HSIN6 | Lane 6 receiver differential pair (-) |
| 45 | HSOP7 | Lane 7 transmitter differential pair (+) | Ground | |
| 46 | HSON7 | Lane 7 transmitter differential pair (-) | Ground | |
| 47 | Ground | | HSIP7 | Lane 7 receiver differential pair (+) |
| 48 | PRSNT2# | Hot plug presence detect | HSIN7 | Lane 7 receiver differential pair (-) |
| 49 | Ground | | Ground | |
| 50 | NC | | Reserved | |
| 51 | NC | | Ground | |
| 52 | Ground | | NC | |
| 53 | Ground | | NC | |
| 54 | NC | | Ground | |
| 55 | NC | | Ground | |
| 56 | Ground | | NC | |
| 57 | Ground | | NC | |
| 58 | NC | | Ground | |
| 59 | NC | | Ground | |
| 60 | Ground | | NC | |
| 61 | Ground | | NC | |
| 62 | NC | | Ground | |
| 63 | NC | | Ground | |
| 64 | Ground | | NC | |
| 65 | Ground | | NC | |
| 66 | NC | | Ground | |
| 67 | NC | | Ground | |
| 68 | Ground | | NC | |
| 69 | Ground | | NC | |
| 70 | NC | | Ground | |
| 71 | NC | | Ground | |
| 72 | Ground | | NC | |
| 73 | Ground | | NC | |
| 74 | NC | | Ground | |
| 75 | NC | | Ground | |
| 76 | Ground | | NC | |
| 77 | Ground | | NC | |
| 78 | NC | | Ground | |
| 79 | NC | | Ground | |

| Pin | Side B | | Side A | |
|---|---|---|---|---|
| | Signal | Description | Signal | Description |
| 80 | Ground | | NC | |
| 81 | PRSNT2# | Hot plug presence detect | NC | |
| 82 | Reserved | | Ground | |

## 7.17. Volume Control Pin Header (VOLUME_CONTROL)

The pin header VOLUME_CONTROL is intended to connect to volume control button of the monitor to control the volume. This feature requires a software update to be enabled.

Figure 33: Volume Control Pin Header VOLUME_CONTROL

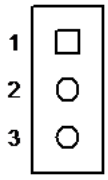



Table 39: Pin Assignment VOLUME_CONTROL

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | GPIO_VOL_DW | Volume down button | |
| 2 | GND | Ground | |
| 3 | GPIO_VOL_UP | Volume up button | |

## 7.18. I2C (Inter-Integrated Circuit) Pin Header (I2C)

The board reserves an I2C pin header for users to use the corresponding I2C channels for their own purpose within a system.

Figure 34: I2C Pin Header I2C

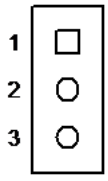



Table 40: Pin Assignment I2C

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | I2C_SCL | I2C serial clock | |
| 2 | I2C_SDA | I2C serial data | |
| 3 | GND | Ground | |

## 7.19. Chassis Intrusion Pin Header (CI)

The pin header CI provides a chassis detection feature that detects whether the chassis cover has been removed. This function requires a chassis with chassis intrusion detection design.

Figure 35: Chassis Intrusion Pin Header CI

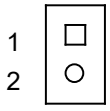



Table 41: Pin Assignment CI

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | Signal | Chassis intrusion signal | |
| 2 | GND | Ground | |

## 7.20. Status LEDs (STB & BOOT)

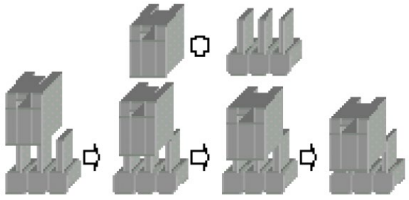
If the standby status LED STB is on, that means the system is in standby mode; if the boot status LED BOOT is on, that means the system is powered on.

Figure 36: Status LEDs STB, BOOT

## 7.21. Switches and Jumpers

The product has several jumpers which must be properly configured to ensure correct operation.

**Figure 37: Jumper Connector**



For a three-pin jumper (see Figure 37), the jumper setting is designated "1-2" when the jumper connects pins 1 and 2. The jumper setting is designated "2-3" when pins 2 and 3 are connected and so on. You will see that one of the lines surrounding a jumper pin is thick, which indicates pin No.1.

To move a jumper from one position to another, use needle-nose pliers or tweezers to pull the pin cap off the pins and move it to the desired position.

### 7.21.1. AT / ATX Power Mode Selection (AT_ATX)

The jumper AT_ATX can be used to select AT power mode or ATX power mode.

**Figure 38: AT / ATX Power Mode Selection AT_ATX**

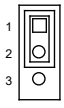



**Table 42: Pin Assignment AT_ATX**

| Jumper Position | | Description |
|---|---|---|
| Pin 1-2 | Pin 2-3 | |
| X | - | AT Mode |
| - | X | ATX Mode (Default) |

"X" = Jumper set (short) and "-" = jumper not set (open)

## 7.21.2. PCIe Configuration Setting for PCIEX16 (PEG_X16_X8)

The jumper PEG_X16_X8 can be set how to divide PCIe x16 lane..

**Figure 39: PCIe Configuration Setting for PCIEX16 PEG_X16_X8**

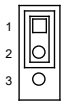



**Table 43: Pin Assignment PEG_X16_X8**

| Jumper Position | | Description |
|---|---|---|
| Pin 1-2 | Pin 2-3 | |
| X | - | PCIe x16 (Default) |
| - | X | PCIe x8 + PCIe x8 |

"X" = Jumper set (short) and "-" = jumper not set (open)

## 7.21.3. Pin-9 Power Selection for COM 5 & COM 6 (COME_PW & COMF_PW)

The jumper COME_PW and COMF_PW can be used to select the power voltage of Pin 9 of the serial COM port COM 5 and COM 6 respectively.

**Figure 40: Pin-9 Power Selection COME_PW, COMF_PW**

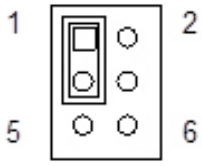



**Table 44: Pin Assignment COME_PW, COMF_PW**

| Jumper Position | | | Description |
|---|---|---|---|
| Pin 1-3 | Pin 3-5 | Pin 3-4 | |
| X | - | - | Pin-9 = 5V |
| - | X | - | Pin-9 = 12V |
| - | - | X | Pin-9 = RI |

"X" = Jumper set (short) and "-" = jumper not set (open)

## 7.21.4. Panel & Backlight Power Selection for LVDS (LCD_VCC)

The jumper LCD_VCC can be used to select LVDS panel and backlight power voltage for LVDS.

Figure 41: Panel & Backlight Power Selection LCD_VCC

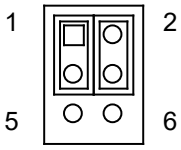



Table 45: Pin Assignment LCD_VCC

| Jumper 1 Position | | Description |
|---|---|---|
| Pin 1-3 | Pin 3-5 | |
| X | - | Backlight Power = +12 V (Default) |
| - | X | Backlight Power = +5 V |
| Jumper 2 Position | | Description |
| Pin 2-4 | Pin 4-6 | |
| X | - | Panel Power = +3.3 V (Default) |
| - | X | Panel Power = +5 V |

"X" = Jumper set (short) and "-" = jumper not set (open)

## 7.21.5. Backlight Power Enable Selection for LVDS (BL_EN)

The jumper BL_EN can be used to select voltage level of backlight enable signal for LVDS.

Figure 42: Backlight Enable Selection BL_EN

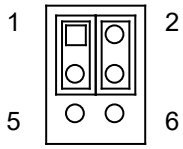



Table 46: Pin Assignment BL_EN

| Jumper 1 Position | | Description |
|---|---|---|
| Pin 1-3 | Pin 3-5 | |
| X | - | Backlight Enable Voltage = +3.3 V (Default) |
| - | X | Backlight Enable Level = +5 V |
| Jumper 2 Position | | Description |
| Pin 2-4 | Pin 4-6 | |
| X | - | Backlight Enable Active High (Default) |
| - | X | Backlight Enable Active Low |

“X" = Jumper set (short) and “-" = jumper not set (open)

## 7.21.6. Clear CMOS Selection (CLR_CMOS)

The jumper CLR_CMOS can be used to clear CMOS RTC content.

The jumper has one positions: Pin 1-2 non-mounted is the default configuration.

Figure 43: Clear CMOS Selection CLR_CMOS

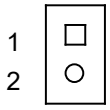



Table 47: Pin Assignment CLR_CMOS

| Jumper Position<br>Pin 1-2 | Description |
|---|---|
| - | Normal operation (default position) |
| X | Enable Clear CMOS RTC content<br>(board does not boot with the jumper in this position) |

“X" = Jumper set (short) and "-" = jumper not set (open)

**Do not leave the jumper in position 1-2, otherwise if the power is disconnected, the battery will fully deplete within a few weeks.**

# 8/ BIOS

## 8.1. Starting the uEFI BIOS

The MITX-CFL0 Series is provided with a Kontron-customized, pre-installed and configured version of AMI Aptio® V uEFI BIOS. AMI BIOS firmware is based on the Unified Extensible Firmware Interface (UEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the MITX-CFL0 Series.

The uEFI BIOS comes with a setup program that provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The setup program allows the accessing of various menus that provide functions or access to sub-menus with more specific functions of their own.

To start the uEFI BIOS setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <DEL> key.
4. If the uEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see Security menu), press <RETURN>, and proceed with step 5.
5. A setup menu will appear.

The MITX-CFL0 Series uEFI BIOS setup program uses a hot key-based navigation system. A hot key legend bar is located on the bottom of the setup screens.

The following table provides information concerning the usage of these hot keys.

**Table 48: Hotkeys Table**

| Signal | Description |
|---|---|
| <F1> | The <F1> key invokes the General Help window. |
| <-> | The <Minus> key selects the next lower value within a field. |
| <+> | The <Plus> key selects the next higher value within a field. |
| <F2> | The <F2> key loads the previous values. |
| <F3> | The <F3> key loads the standard default values. |
| <F4> | The <F4> key saves the current settings and exit the uEFI BIOS setup. |
| <→> or <←> | The <Left/Right> arrows selects major setup menus on the menu bar. For example: Main, Advanced, Security, etc. |
| < ↑ > or < ↓ > | The <Up/Down> arrows selects fields in the current menu. For example: A setup function or a sub-screen. |
| <ESC> | The <ESC> key exits a major setup menu and enter the Exit setup menu.<br>Pressing the <ESC> key in a sub-menu displays the next higher menu level. |
| <RERURN> | The <RETURN> key executes a command or select a submenu. |

## 8.2. Starting the uEFI BIOS

The Setup utility features shows six menus in the selection bar at the top of the screen:

- Main
- Advanced
- Power
- Boot
- Security
- Save & Exit

The Setup menus are selected via the left and right arrow keys. The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white. Each Setup menu provides two main frames. The left frame displays all available functions. Functions that can be configured are displayed in blue. Functions displayed in gray provide information about the status or the operational configuration. The right frame displays an Item Specific Help window providing an explanation of the respective function.

### 8.2.1. Main Setup Menu

Upon entering the uEFI BIOS Setup program, the Main Setup menu is displayed. This screen lists the Main Setup menu sub-screens and provides basic system information. Additionally functions for setting the system time and date are offered.

**Table 49: Main Setup Menu Sub-Screens and Functions**

| Function | Description |
|---|---|
| Product Information | Read only field.<br>Displays information about the product name, system BIOS and ME firmware |
| CPU Information | Read only field.<br>Displays information about processor |
| Memory Information | Read only field.<br>Displays information about total memory |
| System Date | Set System Date |
| System Time | Set System Time |

Figure 44: BIOS Main Menu Screen System Data and Time

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Product Information | | | | | |
| Product Name | | MITX-CFL1 | | | |
| BIOS Version | | R1.00 (x64) | | | |
| BIOS Build Date | | 01/07/2021 | | | |
| ME Firmware SKU | | Corporate SKU | | | |
| ME Firmware Version | | 12.0.71.1681 | | | |
| CPU Information | | | | | |
| Intel® Core™ i7-8700 CPU @ 3.20 GHz | | | | | |
| Microcode Revision | | DE | | | |
| Processor Cores | | 6 Core(s) / 12 Thread(s) | | | |
| Memory Information | | | | → ←: Select Screen<br>↑ ↓: Select Item | |
| Total Size | | 16384 MB (DDR4) | | Enter: Select | |
| Frequency | | 2667 MHz | | +/-: Change Opt. | |
| | | | | F1: General Help | |
| System Date | | [Tue 01/12/2021] | | F2: Previous Values | |
| System Time | | [08:58:15] | | F3: Optimized Defaults | |
| | | | | F4: Save & Exit | |
| Access Level | | Administrator | | ESC: Exit | |
| Version 2.20.1275. Copyright (C) 2021, American Megatrends, Inc. | | | | | |

| Feature | Option | Description |
|---|---|---|
| System Date | [dd/mm/yyyy] | Set the Date. Use Tab to switch between Data elements.<br>Default Ranges:<br>Year: 2005 – 1099<br>Months: 1 – 12<br>Days: dependent on month |
| System Time | [hh:mm:ss] | Set the Time. Use Tab to switch between Time elements. |

## 8.2.2. Advanced Setup Menu

The Advanced setup menu provides sub-screens and functions for advanced configurations. The following sub-screen functions are included in the menu:

- LAN & Audio Configuration
- Display Configuration
- Super IO Configuration
- CPU Chipset Configuration
- NVMe Configuration
- SATA Configuration
- USB Configuration
- AMT Configuration
- Trusted Computing
- H/W Monitor
- DIO Configuration
- Network Stack Configuration

***NOTICE***

**Setting items on this screen to incorrect values may cause the system to malfunction.**

Figure 45: BIOS Advanced Menu

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Onboard LAN1 Controller | | [Enabled] | | | |
| Onboard LAN2 Controller | | [Enabled] | | | |
| Load I219 UNDI Driver(1) | | [Disabled] | | | |
| Load I211 UNDI Driver(2) | | [Disabled] | | | |
| Audio Controller | | [Enabled] | | | |
| > Display Configuration | | | | | |
| > Super IO Configuration | | | | | |
| > CPU Chipset Configuration | | | | | |
| > NVMe Configuration | | | | →←: Select Screen | |
| > SATA Configuration | | | | ↑ ↓: Select Item | |
| > USB Configuration | | | | Enter: Select | |
| > AMT Configuration | | | | +/-: Change Opt. | |
| > Trusted Computing | | | | F1: General Help | |
| > H/W Monitor | | | | F2: Previous Values | |
| > DIO Configuration | | | | F3: Optimized Defaults | |
| | | | | F4: Save & Exit | |
| > Network Stack Configuration | | | | ESC: Exit | |
| Version 2.20.1275. Copyright (C) 2021, American Megatrends, Inc. | | | | | |

(1) This item appears only when enabling Onboard LAN1 Controller.

(2) This item appears only when enabling Onboard LAN2 Controller.

| Feature | Option | Description |
|---|---|---|
| Onboard LAN1 Controller | [Disabled], [Enabled] | Select whether to enable or disable Onboard LAN1 Controller. Intel-i219. |
| Onboard LAN2 Controller | [Disabled], [Enabled] | Select whether to enable or disable Onboard LAN2 Controller. Intel-i210. |
| Load I219 UNDI Driver | [Disabled], [Enabled] | Select whether to load LAN UNDI Driver. |
| Load I211 UNDI Driver | [Disabled], [Enabled] | Select whether to load LAN UNDI Driver. |
| Audio Controller | [Disabled], [Enabled] | Select whether to enable or disable Audio Controller. |

Figure 46: BIOS Advanced Menu - Display Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Display Configuration | | | | | |
| Primary Display | | [IGFX] | | | |
| Internal Graphics | | [Enabled] | | | |
| Aperture Size | | [256MB] | | → ←: Select Screen | |
| DVMT Pre-Allocated | | [32M] | | ↑ ↓: Select Item | |
| DVMT Total Gfx Mem | | [256M] | | Enter: Select | |
| | | | | +/-: Change Opt. | |
| Active LVDS | | [Disabled] | | F1: General Help | |
| LVDS Panel Type(1) | | [1024x768 18Bit 1CH] | | F2: Previous Values | |
| PWM Backlight Control | | [By Internal] | | F3: Optimized Defaults | |
| LVDS Backlight Control – PWM(2) | | 127 | | F4: Save & Exit | |
| LVDS Backlight PWM FREQ SEL(2) | | [200 Hz] | | ESC: Exit | |
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(1) This item appears only when enabling Active LVDS.

(2) These items appear only when selecting By External for PWM Backlight Control.

| Feature | Option | Description |
|---|---|---|
| Primary Display | [IGFX],<br>[PEG] | Select which of IGFX / PEG Graphics device should be Primary Display. |
| Internal Graphics | [Enabled] | This field is not selectable. |
| Aperture Size | [128MB],<br>[256MB],<br>[512MB],<br>[1024MB],<br>[2048MB] | Select the Aperture Size.<br>Note: Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM Support. |
| DVMT Pre-Allocated | [32M],<br>[64M],<br>[4M],<br>[8M],<br>[12M],<br>[16M],<br>[20M],<br>[24M],<br>[28M],<br>[32M/F7],<br>[36M],<br>[40M],<br>[44M],<br>[48M],<br>[52M],<br>[56M], | Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device. |

| Feature | Option | Description |
|---|---|---|
| | [60M] | |
| DVMT Total Gfx Mem | [128M],<br>[256M],<br>[MAX] | Select DVMT 5.0 Total Graphic Memory size used by the Internal Graphics Device. |
| Active LVDS | [Disabled],<br>[Enabled] | Select the Active LVDS Configuration.<br>[Disabled]: VBIOS does not enable LVDS.<br>[Enabled]: VBIOS will enable LVDS. |
| LVDS Panel Type | [640x480 18Bit 1CH],<br>[800x480 18Bit 1CH],<br>[800x600 18Bit 1CH],<br>[1024x768 18Bit 1CH],<br>[1440x900 18Bit 2CH],<br>[1600x900 18Bit 2CH],<br>[1024x600 18Bit 1CH],<br>[1366x768 18Bit 1CH],<br>[1024x768 24Bit 1CH],<br>[1280x1024 24Bit 2CH],<br>[1366x768 24Bit 1CH],<br>[1366x768 24Bit 2CH],<br>[1440x900 24Bit 2CH],<br>[1600x1200 24Bit 2CH],<br>[1920x1080 24Bit 2CH],<br>[1920x1200 24Bit 2CH] | Select the appropriate setup item for LVDS panel type. |
| PWM Backlight Control | [By External],<br>[By Internal] | Select the appropriate setup item for PWM Backlight Control.<br>[By External]: Control by external HW circuit.<br>[By Internal]: Control by LBKLT_CTL on the Intel Chipset. |
| LVDS Backlight Control - PWM | Value Input | 0 – 255 PWM Duty |
| LVDS Backlight PWM FREQ SEL | [23.3 KHz],<br>[11.6 KHz],<br>[5.8 KHz],<br>[200 Hz] | Select an appropriate setup item for LVDS Backlight PWM FREQ SEL. |

Figure 47: BIOS Advanced Menu - Super IO Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Super IO Configuration | | | | | |
| > Serial Port 1 Configuration | | | | →←: Select Screen | |
| > Serial Port 2 Configuration | | | | ↑ ↓: Select Item | |
| > Serial Port 3 Configuration | | | | Enter: Select | |
| > Serial Port 4 Configuration | | | | +/-: Change Opt. | |
| > Serial Port 5 Configuration | | | | F1: General Help | |
| > Serial Port 6 Configuration | | | | F2: Previous Values | |
| | | | | F3: Optimized Defaults | |
| | | | | F4: Save & Exit | |
| | | | | ESC: Exit | |
| Version 2.20.1275. Copyright (C) 2021, American Megatrends, Inc. | | | | | |

Figure 48: BIOS Advanced Menu - Super IO Configuration - Serial Port 1 Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Super Port 1 Configuration | | | | | |
| Serial Port | | [Enabled] | | →←: Select Screen | |
| Device Settings* | | IO=3F8h; IRQ=4; | | ↑ ↓: Select Item | |
| | | | | Enter: Select | |
| Change Setting* | | [Auto] | | +/-: Change Opt. | |
| | | | | F1: General Help | |
| | | | | F2: Previous Values | |
| | | | | F3: Optimized Defaults | |
| | | | | F4: Save & Exit | |
| | | | | ESC: Exit | |
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* These items appear only when enabling Serial Port.

| Feature | Option | Description |
|---|---|---|
| Serial Port | [Disabled],<br>[Enabled] | Select whether to enable or disable Serial Port (COM). |
| Change Settings | [Auto],<br>[IO=3F8h; IRQ=4;],<br>[IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=3E8h; IRQ=3, 4, 5, 6, | Select an optional setting for Super IO device. |

| Feature | Option | Description |
|---|---|---|
| | 7, 9, 10, 11, 12;],<br>[IO=2E8h; IRQ=3, 4, 5, 6,<br>7, 9, 10, 11, 12;] | |

Figure 49: BIOS Advanced Menu - Super IO Configuration - Serial Port 2 Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Super Port 2 Configuration | | | | | |
| Serial Port | | [Enabled] | | → ←: Select Screen | |
| Device Settings* | | IO=2F8h; IRQ=3; | | ↑ ↓: Select Item | |
| | | | | Enter: Select | |
| Change Setting* | | [Auto] | | +/-: Change Opt. | |
| | | | | F1: General Help | |
| | | | | F2: Previous Values | |
| | | | | F3: Optimized Defaults | |
| | | | | F4: Save & Exit | |
| | | | | ESC: Exit | |
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* These items appear only when enabling Serial Port.

| Feature | Option | Description |
|---|---|---|
| Serial Port | [Disabled],<br>[Enabled] | Select whether to enable or disable Serial Port (COM). |
| Change Settings | [Auto],<br>[IO=2F8h; IRQ=3;],<br>[IO=3F8h; IRQ=3, 4, 5, 6,<br>7, 9, 10, 11, 12;],<br>[IO=2F8h; IRQ=3, 4, 5, 6,<br>7, 9, 10, 11, 12;],<br>[IO=3E8h; IRQ=3, 4, 5, 6,<br>7, 9, 10, 11, 12;],<br>[IO=2E8h; IRQ=3, 4, 5, 6,<br>7, 9, 10, 11, 12;] | Select an optional setting for Super IO device. |

Figure 50: BIOS Advanced Menu - Super IO Configuration - Serial Port 3 Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Super Port 3 Configuration | | | | | |
| Serial Port | | [Enabled] | | → ←: Select Screen | |
| Device Settings* | | IO=3E8h; IRQ=7; | | ↑ ↓: Select Item | |
| | | | | Enter: Select | |

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Change Setting* | | [Auto] | | +/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit | |
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* These items appear only when enabling Serial Port.

| Feature | Option | Description |
|---|---|---|
| Serial Port | [Disabled],<br>[Enabled] | Select whether to enable or disable Serial Port (COM). |
| Change Settings | [Auto],<br>[IO=3E8h; IRQ=7;],<br>[IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;] | Select an optional setting for Super IO device. |

Figure 51: BIOS Advanced Menu - Super IO Configuration - Serial Port 4 Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Super Port 4 Configuration | | | | | |
| Serial Port | | [Enabled] | | →←: Select Screen | |
| Device Settings* | | IO=2E8h; IRQ=5; | | ↑ ↓: Select Item | |
| | | | | Enter: Select | |
| Change Setting* | | [Auto] | | +/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit | |
| Version 2.20.1275. Copyright (C) 2021, American Megatrends, Inc. | | | | | |

* These items appear only when enabling Serial Port.

| Feature | Option | Description |
|---|---|---|
| Serial Port | [Disabled], | Select whether to enable or disable Serial Port (COM). |

| Feature | Option | Description |
|---|---|---|
| | [Enabled] | |
| Change Settings | [Auto],<br>[IO=2E8h; IRQ=7;],<br>[IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;] | Select an optional setting for Super IO device. |

**Figure 52: BIOS Advanced Menu - Super IO Configuration - Serial Port 5 Configuration**

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Super Port 5 Configuration | | | | | |
| Serial Port | | [Enabled] | | → ←: Select Screen | |
| Device Settings* | | IO=2F0h; IRQ=7; | | ↑ ↓: Select Item | |
| | | | | Enter: Select | |
| Change Setting* | | [Auto] | | +/-: Change Opt. | |
| Serial Port 5 Type* | | [RS232] | | F1: General Help | |
| Data Transfer Rate* | | [250Kbps, One Transmitter Switching] | | F2: Previous Values | |
| RS485 Duplex Mode*(2) | | [Half Duplex] | | F3: Optimized Defaults | |
| RS485 Auto Flow Termination*(3) | | [Disabled] | | F4: Save & Exit | |
| RS485/422 Receiver Termination*(1) | | [Enabled] | | ESC: Exit | |
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* These items appear only when enabling Serial Port.

(1) This item appears only when selecting RS485 or RS422 for the Serial Port 5 Type.

(2) This item appears only when selecting RS485 for the Serial Port 5 Type.

(3) This item appears only when selecting RS485 for the Serial Port 5 Type and Half Duplex for RS485 Duplex Mode.

| Feature | Option | Description |
|---|---|---|
| Serial Port | [Disabled], [Enabled] | Select whether to enable or disable Serial Port (COM). |
| Change Settings | [Auto],<br>[IO=2F0h; IRQ=7;],<br>[IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;] | Select an optional setting for Super IO device. |

| Feature | Option | Description |
|---|---|---|
| Serial Port 5 Type | [RS232],<br>[RS422],<br>[RS485] | Select an appropriate type for Serial Port 5. |
| Date Transfer Rate | [250Kbps, One Transmitter Switching],<br>[RS-422/RS-485 to 20Mbps] | Select an appropriate setup item for Data Transfer Rate. |
| RS485 Duplex Mode | [Half Duplex],<br>[Full Duplex] | Select an appropriate RS485 Duplex Mode. |
| RS485 Auto Flow Control | [Disabled],<br>[Enabled] | Select whether to enable or disable RS485 Auto Flow Control. |
| RS485/422 Receiver Termination | [Disabled],<br>[Enabled] | Select whether to enable or disable RS485/422 Receiver Termination. |

**Figure 53: BIOS Advanced Menu - Super IO Configuration - Serial Port 6 Configuration**

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Super Port 6 Configuration | | | | | |
| Serial Port | | [Enabled] | | → ←: Select Screen | |
| Device Settings* | | IO=2E0h; IRQ=7; | | ↑ ↓: Select Item | |
| | | | | Enter: Select | |
| Change Setting* | | [Auto] | | +/-: Change Opt. | |
| Serial Port 6 Type* | | [RS232] | | F1: General Help | |
| Data Transfer Rate* | | [250Kbps, One Transmitter Switching] | | F2: Previous Values | |
| RS485 Duplex Mode*(2) | | [Half Duplex] | | F3: Optimized Defaults | |
| RS485 Auto Flow Termination*(3) | | [Disabled] | | F4: Save & Exit | |
| RS485/422 Receiver Termination*(1) | | [Enabled] | | ESC: Exit | |
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* These items appear only when enabling Serial Port.

(1) This item appears only when selecting RS485 or RS422 for the Serial Port 6 Type.

(2) This item appears only when selecting RS485 for the Serial Port 6 Type.

(3) This item appears only when selecting RS485 for the Serial Port 6 Type and Half Duplex for RS485 Duplex Mode.

| Feature | Option | Description |
|---|---|---|
| Serial Port | [Disabled], [Enabled] | Select whether to enable or disable Serial Port (COM). |
| Change Settings | [Auto],<br>[IO=2E0h; IRQ=7;],<br>[IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2F0h; IRQ=3, 4, 5, 6, | Select an optional setting for Super IO device. |

| Feature | Option | Description |
|---|---|---|
| | 7, 9, 10, 11, 12;],<br>[IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;] | |
| Serial Port 6 Type | [RS232],<br>[RS422],<br>[RS485] | Select an appropriate type for Serial Port 6. |
| Date Transfer Rate | [250Kbps, One Transmitter Switching],<br>[RS-422/RS-485 to 20Mbps] | Select an appropriate setup item for Data Transfer Rate. |
| RS485 Duplex Mode | [Half Duplex],<br>[Full Duplex] | Select an appropriate RS485 Duplex Mode. |
| RS485 Auto Flow Control | [Disabled],<br>[Enabled] | Select whether to enable or disable RS485 Auto Flow Control. |
| RS485/422 Receiver Termination | [Disabled],<br>[Enabled] | Select whether to enable or disable RS485/422 Receiver Termination. |

Figure 54: BIOS Advanced Menu - CPU Chipset Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| CPU Chipset Configuration | | | | | |
| EIST | | [Enabled] | | →←: Select Screen | |
| Turbo Mode(1) | | [Enabled] | | ↑ ↓: Select Item | |
| Hyper-Threading | | [Enabled] | | Enter: Select | |
| VT-d | | [Enabled] | | +/-: Change Opt. | |
| Active Processor Cores | | [All] | | F1: General Help | |
| Intel (VMX) Virtualization Technology | | [Enabled] | | F2: Previous Values | |
| Intel Trusted Execution Technology(2) | | [Disabled] | | F3: Optimized Defaults | |
| | | | | F4: Save & Exit | |
| | | | | ESC: Exit | |
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(1) This item appears only when enabling EIST.

(2) This item is selectable only when enabling Intel (VMX) Virtualization Technology.

| Feature | Option | Description |
|---|---|---|
| EIST | [Disabled],<br>[Enabled] | Select whether to enable or disable Enhanced Intel SpeedStep Technology. |
| Turbo Mode | [Disabled],<br>[Enabled] | Select whether to enable or disable processor Turbo Mode (requires Intel Speed Step or Intel Speed Shift to be available and enabled). |
| Hyper-Threading | [Disabled],<br>[Enabled] | Select whether to enable or disable Hyper-Threading Technology. |
| VT-d | [Disabled],<br>[Enabled] | Select whether to enable or disable VT-d capability. |
| Active Processor Cores | [All],<br>[1],<br>[2],<br>[3],<br>[4],<br>[5] | Select number of cores to enable in each processor package. |
| Intel (VMX) Virtualization Technology | [Disabled],<br>[Enabled] | When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. |
| Intel Trusted Execution Technology | [Disabled],<br>[Enabled] | Enables utilization of additional hardware capabilities provided by Intel® Trusted Execution Technology.<br>Changes require a full power cycle to take effect. |

Figure 55: BIOS Advanced Menu - NVMe Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| NVMe Configuration | | | | | |
| No NVMe Device Found | | | | →←: Select Screen<br>↑ ↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit | |
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Figure 56: BIOS Advanced Menu - SATA Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| SATA Configuration | | | | | |
| SATA Controller(s) | | [Enabled] | | | |
| SATA Mode Selection* | | [AHCI] | | | |
| | | | | →←: Select Screen | |
| Serial ATA Port 1 | | Empty | | ↑ ↓: Select Item | |
| Port 1 | | [Enabled] | | Enter: Select | |
| Serial ATA Port 2 | | Empty | | +/-: Change Opt. | |
| Port 2 | | [Enabled] | | F1: General Help | |
| Serial ATA Port 3 | | Empty | | F2: Previous Values | |
| Port 3 | | [Enabled] | | F3: Optimized Defaults | |
| Serial ATA Port 4 | | Empty | | F4: Save & Exit | |
| Port 4 | | [Enabled] | | ESC: Exit | |
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* This item appears only when enabling SATA Controller(s).

| Feature | Option | Description |
|---|---|---|
| SATA Controller(s) | [Enabled],<br>[Disabled] | Select whether to enable or disable SATA Controller. |
| SATA Mode Selection | [AHCI],<br>[Intel RST Premium With Intel Optane System Acceleration] | Determines how SATA controller(s) operate. |
| Port 1…4 | [Disabled],<br>[Enabled] | Select whether to enable or disable SATA port 1…4. |

Figure 57: BIOS Advanced Menu - USB Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| USB Configuration | | | | | |
| USB Devices: | | | | → ←: Select Screen | |
| 1 Keyboard | | | | ↑ ↓: Select Item | |
| | | | | Enter: Select | |
| Legacy USB Support | | [Enabled] | | +/-: Change Opt. | |
| XHCI Hand-off | | [Disabled] | | F1: General Help | |
| USB Mass Storage Driver Support | | [Enabled] | | F2: Previous Values | |
| | | | | F3: Optimized Defaults | |
| | | | | F4: Save & Exit | |
| | | | | ESC: Exit | |
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| Feature | Option | Description |
|---|---|---|
| Legacy USB Support | [Enabled],<br>[Disabled],<br>[Auto] | Ensables Legacy USB support.<br>AUTO option disables legacy support if no USB devices are connected. |
| XHCI Hand-off | [Enabled],<br>[Disabled] | This is a workaround for OSes without XHCI hand-off support.<br>The XHCI ownership change should be claimed by XHCI driver. |
| USB Mass Storage Driver Support | [Disabled],<br>[Enabled] | Enable / disable USB Mass Storage Driver Support. |

Figure 58: BIOS Advanced Menu - AMT Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| AMT Configuration | | | | | |
| AMT BIOS Features | | [Enabled] | | → ←: Select Screen<br>↑ ↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit | |
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| Feature | Option | Description |
|---|---|---|
| AMT BIOS Features | [Disabled],<br>[Enabled] | When disabled AMT BIOS Features are no longer supported and user is no longer able to access MEBx Setup.<br>Note: This option does not disable Manageability Features in FW. |

Figure 59: BIOS Advanced Menu - Trusted Computing

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Configuration | | | | | |
| Security Device Support | | [Disabled] | | | |
| NO Security Device Found | | | | → ←: Select Screen<br>↑ ↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit | |
| Version 2.20.1275. Copyright (C) 2021, American Megatrends, Inc. | | | | | |

| Feature | Option | Description |
|---|---|---|
| Security Device Support | [Disable],<br>[Enable] | Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. |

Figure 60: BIOS Advanced Menu - H/W Monitor

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| PC Health Status | | | | | |
| > Smart FAN Configuration | | | | | |
| System Temperature | | : +32 C | | | |
| CPU Temperature | | : +43 C | | | |
| CPU Fan Speed | | : 2636 RPM | | → ←: Select Screen | |
| SYS Fan Speed | | : N/A | | ↑ ↓: Select Item | |
| | | | | Enter: Select | |
| +VCORE | | : +1.061 V | | +/-: Change Opt. | |
| +12V | | : +11.876 V | | F1: General Help | |
| +3.3V | | : +3.376 V | | F2: Previous Values | |
| +VMEM | | : +1.213 V | | F3: Optimized Defaults | |
| +5V | | : +5.175 V | | F4: Save & Exit | |
| +VRTC | | : +3.120 V | | ESC: Exit | |
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Figure 61: BIOS Advanced Menu - H/W Monitor - Smart FAN Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Smart FAN Configuration | | | | | |
| CPU FAN Setting | | [Manual] | | | |
| Manual Duty* | | 127 | | | |
| 1st Boundary Temperature** | | 30 | | | |
| 1st FAN Speed** | | 50 | | | |
| 2nd Boundary Temperature** | | 40 | | | |
| 2nd FAN Speed** | | 100 | | | |
| 3rd Boundary Temperature** | | 50 | | | |
| 3rd FAN Speed** | | 150 | | | |
| 4th Boundary Temperature** | | 60 | | | |
| 4th FAN Speed** | | 200 | | | |
| System FAN Setting | | [Manual] | | | |
| Manual Duty* | | 255 | | → ←: Select Screen | |
| 1st Boundary Temperature** | | 30 | | ↑ ↓: Select Item | |
| 1st FAN Speed** | | 50 | | Enter: Select | |
| 2nd Boundary Temperature** | | 40 | | +/-: Change Opt. | |
| 2nd FAN Speed** | | 100 | | F1: General Help | |

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| 3rd Boundary Temperature** | | 50 | | F2: Previous Values | |
| 3rd FAN Speed** | | 150 | | F3: Optimized Defaults | |
| 4th Boundary Temperature** | | 60 | | F4: Save & Exit | |
| 4th FAN Speed** | | 200 | | ESC: Exit | |
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* These items appear only when selecting Manual for the CPU / System FAN Setting.

** These items appear only when selecting Smart for the CPU / System FAN Setting.

| Feature | Option | Description |
|---|---|---|
| CPU FAN Setting | [Manual],<br>[Smart] | Select CPU smart FAN configuration. |
| System FAN Setting | [Manual],<br>[Smart] | Select system smart FAN configuration. |
| Manual Duty | Value Input | 0 – 255 PWM Duty |
| 1st / 2nd / 3rd / 4th Boundary Temperature | Value Input | 1 – 100 C |
| 1st / 2nd / 3rd / 4th FAN Speed | Value Input | 0 – 255 PWM Duty |

Figure 62: BIOS Advanced Menu - DIO Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| DIO Configuration | | | | | |
| User Configuration | | [Disabled] | | | |
| DIO_0* | | [Output High] | | | |
| DIO_1* | | [Output High] | | | |
| DIO_2* | | [Output High] | | | |
| DIO_3* | | [Output High] | | | |
| DIO_4* | | [Output High] | | | |
| DIO_5* | | [Output High] | | | |
| DIO_6* | | [Output High] | | | |
| DIO_7* | | [Output High] | | | |
| DIO_0 Value | | 1 | | →←: Select Screen<br>↑ ↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit | |
| DIO_1 Value | | 1 | | | |
| DIO_2 Value | | 1 | | | |
| DIO_3 Value | | 1 | | | |
| DIO_4 Value | | 1 | | | |
| DIO_5 Value | | 1 | | | |
| DIO_6 Value | | 1 | | | |
| DIO_7 Value | | 1 | | | |
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* These items appear only when enabling User Configuration.

| Feature | Option | Description |
|---|---|---|
| User Configuration | [Enabled],<br>[Disabled] | User can set the DO pin output value. |
| DIO_0…7 | [Output Low],<br>[Output High],<br>[Input] | Set the DO pin output value. |

Figure 63: BIOS Advanced Menu - Network Stack Configuration

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Network Stack | | [Disabled] | | | |
| Ipv4 PXE Support* | | [Disabled] | | | |
| Ipv4 HTTP Support* | | [Disabled] | | →←: Select Screen | |
| Ipv6 PXE Support* | | [Disabled] | | ↑ ↓: Select Item | |
| Ipv6 HTTP Support* | | [Disabled] | | Enter: Select | |
| IPSEC Certificate* | | [Enabled] | | +/-: Change Opt. | |
| PXE boot wait time* | | 0 | | F1: General Help | |
| Media detect count* | | 1 | | F2: Previous Values | |
| | | | | F3: Optimized Defaults | |
| | | | | F4: Save & Exit | |
| | | | | ESC: Exit | |
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* These items appear only when enabling Network Stack.

| Feature | Option | Description |
|---|---|---|
| Network Stack | [Disabled], [Enabled] | Enable / disable UEFI Network Stack. |
| Ipv4 PXE Support | [Disabled], [Enabled] | Enable / disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available. |
| Ipv4 HTTP Support | [Disabled], [Enabled] | Enable / disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available. |
| Ipv6 PXE Support | [Disabled], [Enabled] | Enable / disable IPv6 PXE Boot Support. If disabled, IPv6 PXE boot support will not be available. |
| Ipv6 HTTP Support | [Disabled], [Enabled] | Enable / disable IPv6 HTTP Boot Support. If disabled, IPv6 HTTP boot support will not be available. |
| IPSEC | [Disabled], [Enabled] | Support to enable / disable IPSEC certificate for Ikev. |
| PXE boot wait time | Value Input | Wait time in seconds to press ESC key to abort the PXE boot. Use either + / - or numeric keys to set the value. |
| Media detect count | Value Input | Number of times the presence of media will be checked. Use either + / - or numeric keys to set the value. |

## 8.2.3. Power Setup Menu

The Power setup menu provides functions and a sub-screen for power configurations. The following sub-screen function is included in the menu:

- WatchDog Timer Configuration

**Figure 64: BIOS Power Setup Menu**

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Power Configuration | | | | | |
| ACPI Sleep State | | [S3 (Suspend to RAM)] | | | |
| Restore AC Power Loss | | [Power Off] | | | |
| Power Saving Mode | | [Disabled] | | | |
| Resume Event Control | | | | →←: Select Screen | |
| Resume By LAN Device | | [Disabled] | | ↑ ↓: Select Item | |
| Resume By PCI-E Device | | [Disabled] | | Enter: Select | |
| Resume By RTC Alarm | | [Disabled] | | +/-: Change Opt. | |
| Date(Days)Alarm* | | 0 | | F1: General Help | |
| Time(hh)Alarm* | | 0 | | F2: Previous Values | |
| Time(mm)Alarm* | | 1 | | F3: Optimized Defaults | |
| Time(ss)Alarm* | | 0 | | F4: Save & Exit | |
| > WatchDog Timer Configuration | | | | ESC: Exit | |
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| Feature | Option | Description |
|---|---|---|
| ACPI Sleep State | [S3 (Suspend to RAM)] | This field is not selectable. |
| Restore AC Power Loss | [Power Off],<br>[Power On],<br>[Last State] | Select AC power state when power is re-applied after a power failure. |
| Power Saving Mode | [Disabled],<br>[EUP Enabled] | Configure the Power Saving Mode configuration. |
| Resume By LAN Device | [Disabled],<br>[Enabled] | Select whether to enable Wake from LAN Device. |
| Resume By PCI-E Device | [Disabled],<br>[Enabled] | Select whether to enable Wake from PCI-E Device. |
| Resume By RTC Alarm | [Disabled],<br>[Enabled] | Select whether to enable or disable Wake Up on Alarm, to turn on your system on a special day of the month. |
| Date(Days)Alarm | Value Input | 0 – 31, 0 stands for every day. |
| Time(hh)Alarm | Value Input | 0 - 23 |
| Time(mm)Alarm | Value Input | 0 - 59 |
| Time(ss)Alarm | Value Input | 0 - 59 |

**Figure 65: BIOS Power Setup Menu - WatchDog Timer Configuration**

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| WatchDog Timer Configuration | | | | | |
| WDT Function | | [Disabled] | | → ←: Select Screen | |
| WDT Count Unit* | | [1 Sec] | | ↑ ↓: Select Item | |
| WDT Timer* | | 30 | | Enter: Select | |
| | | | | +/-: Change Opt. | |
| | | | | F1: General Help | |
| | | | | F2: Previous Values | |
| | | | | F3: Optimized Defaults | |
| | | | | F4: Save & Exit | |
| | | | | ESC: Exit | |
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* These items appear only when enbling WDT Function.

| Feature | Option | Description |
|---|---|---|
| WDT Function | [Disabled],<br>[Enabled] | Select whether to enable or disable WatchDog Timer function. |
| WDT Count Unit | [0.25 Sec],<br>[1 Sec],<br>[2 Sec] | Select the WDT Count Unit. |
| WDT Timer | Value Input | Count 0 - 255 |

## 8.2.4. Boot Setup Menu

The boot setup menu lists the for boot device priority order, that is generated dynamically.

**Figure 66: BIOS Boot Setup Menu**

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Boot Configuration | | | | | |
| Full Screen LOGO Display | | [Disabled] | | | |
| Setup Prompt Timeout | | 1 | | → ←: Select Screen | |
| Bootup NumLock State | | [On] | | ↑ ↓: Select Item | |
| | | | | Enter: Select | |
| CSM Support | | [Disabled] | | +/-: Change Opt. | |
| Boot Option Filter | | [UEFI only] | | F1: General Help | |
| | | | | F2: Previous Values | |
| Boot Option Priorities | | | | F3: Optimized Defaults | |
| Boot Option #1 | | [UEFI: Built-in EFI Shell] | | F4: Save & Exit | |
| | | | | ESC: Exit | |
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| Feature | Option | Description |
|---|---|---|
| Full Screen LOGO Display | [Disabled],<br>[Enabled] | Select whether to enable or disable to display logo screen. |
| Setup Prompt Timeout | Value Input | Number of seconds to wait for setup activation key.<br>65535(0xFFFF) means indefinite waiting. |
| Bootup NumLock State | [On],<br>[Off] | This field indicates the state of the NumLock feature of the keyboard after Startup.<br>[On]: The keys on the keypad will act as numeric keys.<br>[Off]: The keys on the keypad will act as cursor keys. |
| CSM Support | [Enabled],<br>[Disabled] | Enable / disable CSM support. |
| Boot Option Filter | [UEFI and Legacy],<br>[Legacy only],<br>[UEFI only] | This option controls Legacy / UEFI ROMs priority.<br>Only 'UEFI only' when disabling CSM Support. |
| Boot Option #1 | [UEFI: Built-in EFI Shell],<br>[Disabled] | Select Boot option. |

## 8.2.5. Security Setup Menu

The Security setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive. The MITX-CFL0 Series provides no factory-set passwords.

**NOTICE**

**If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing <RETURN>. To set a password, enter it twice and acknowledge by pressing <RETURN>.**

Figure 67: BIOS Security Setup Menu

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Password Description | | | | | |
| If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup | | | | | |
| If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights | | | | | |
| The password length must be in the following range: | | | | | |
| Minimum Length | | 3 | | → ←: Select Screen | |
| Maximum length | | 20 | | ↑ ↓: Select Item | |
| | | | | Enter: Select | |
| Administrator Password | | | | +/-: Change Opt. | |
| User Password | | | | F1: General Help | |
| | | | | F2: Previous Values | |
| > Secure Boot | | | | F3: Optimized Defaults | |
| | | | | F4: Save & Exit | |
| | | | | ESC: Exit | |
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| Feature | Description |
|---|---|
| Administrator Password | Set administrator password |
| User Password | Set user password |

**If only the administrator's password is set, then only access to setup is limited. The password is only entered when entering setup.**

**If only the user's password is set, then the password is a power on password and must be entered to boot or enter setup. Within the setup menu the user has administrator rights.**

**Password length requirements are maximum 20 characters and minimum 3 characters.**

Figure 68: BIOS Security Setup Menu – Secure Boot

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| System Mode | | User | | | |
| Secure Boot | | [Disabled] | | → ←: Select Screen | |
| | | Not Active | | ↑ ↓: Select Item | |
| | | | | Enter: Select | |
| Secure Boot Mode | | [Standard] | | +/-: Change Opt. | |
| > Restore Factory Keys* | | | | F1: General Help | |
| > Reset To Setup Mode* | | | | F2: Previous Values | |
| | | | | F3: Optimized Defaults | |
| > Key Management* | | | | F4: Save & Exit | |
| | | | | ESC: Exit | |
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*These items are selectable only when selecting Custom for Secure Boot Mode.

| Feature | Option | Description |
|---|---|---|
| Secure Boot | [Disabled],<br>[Enabled] | Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset. |
| Secure Boot Mode | [Standard],<br>[Custom] | Secure Boot mode options: Standard or Custom.<br>In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication. |
| Restore Factory Keys | [Yes],<br>[No] | Force System to User Mode.<br>Install factory default Secure Boot key databases. |
| Reset to Setup Mode | [Yes],<br>[No] | Delete all Secure Boot key databases from NVRAM. |

Figure 69: BIOS Security Setup Menu – Secure Boot – Key Management

BIOS SETUP UTILITY

Main | Advanced | Power | Boot | Security | Save & Exit

Vendor Keys — Modified

Factory Key Provision — [Disabled]
> Restore Factory Keys
> Reset To Setup Mode
> Export Secure Boot variables
> Enroll Efi Image

Device Guard Ready
> Remove 'UEFI CA' from DB
> Restore DB defaults

| Secure Boot variable | Size | Keys | Key Source |
|---|---|---|---|
| > Platform Key (PK) | 862 | 1 | Test (AMI) |
| > Key Exchange Keys | 1560 | 1 | Factory |
| > Authorized Signatures | 3143 | 2 | Factory |
| > Forbidden Signatures | 3724 | 77 | Factory |
| > Authorized TimeStamps | 0 | 0 | No Keys |
| > OsRecovery Signatures | 0 | 0 | No Keys |

→ ←: Select Screen
↑ ↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

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| Feature | Option | Description |
|---|---|---|
| Factory Key Provision | [Disabled],<br>[Enabled] | Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode. |
| Reset Factory Keys | [Yes],<br>[No] | Force System to User Mode.<br>Install factory default Secure Boot key databases. |
| Reset to Setup Mode | [Yes],<br>[No] | Delete all Secure Boot key databases from NVRAM. |
| Export Secure Boot variables | Select a File system | Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device. |
| Enroll Efi Image | Select a File system | Allow the image to run in Secure Boot mode.<br>Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db). |
| Remove 'UEFI CA' from DB | [Yes],<br>[No] | Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db). |
| Restore DB defaults | [Yes],<br>[No] | Restore DB variable to factory defaults. |
| Platform Key (PK) | [Details],<br>[Export],<br>[Update],<br>[Delete] | Enroll Factory Defaults or load certificates from a file:<br>1. Public Key Certificate:<br>(a) EFI_SIGNATURE_LIST<br>(b) EFI_CERT_X509 (DER) |

| Feature | Option | Description |
|---|---|---|
| Key Exchange Keys | [Details],<br>[Export],<br>[Update],<br>[Append],<br>[Delete] | (c) EFI_CERT_RSA2048 (bin)<br>(d) EFI_CERT_SHAXXX<br>2. Authenticated UEFI Variable<br>3. EFI PE / COFF Image (SHA256)<br>Key Source: Factory, External, Mixed |
| Authorized Signatures | [Details],<br>[Export],<br>[Update],<br>[Append],<br>[Delete] | |
| Forbidden Signatures | [Details],<br>[Export],<br>[Update],<br>[Append],<br>[Delete] | |
| Authorized TimeStamps | [Update],<br>[Append] | |
| OsRecovery Signatures | [Update],<br>[Append] | |

#### 8.2.5.1. Remember the password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords results in being locked out of the system.

If the system cannot be booted because the User Password or the Supervisor Password are not know, contact Kontron Support for further assistance.

**HDD security passwords cannot be cleared using the above method.**

## 8.2.6. Save & Exit Setup Menu

The exit setup menu provides functions for handling changes made to the UEFI BIOS settings and the exiting of the setup program.

**Figure 70: BIOS Save & Exit Setup Menu**

| BIOS SETUP UTILITY | | | | | |
|---|---|---|---|---|---|
| Main | Advanced | Power | Boot | Security | Save & Exit |
| Save Changes and Reset<br>Discard Changes and Reset | | | | | |
| Save Options<br>Save Changes<br>Discard Changes<br><br>Restore Defaults | | | | →←: Select Screen<br>↑ ↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit | |
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| Feature | Option | Description |
|---|---|---|
| Save Changes and Reset | [Yes],<br>[No] | Reset the system after saving the changes. |
| Discard Changes and Reset | [Yes],<br>[No] | Reset system setup without saving any changes. |
| Save Changes | [Yes],<br>[No] | Save Changes done so far to any of the setup options. |
| Discard Changes | [Yes],<br>[No] | Discard Changes done so far to any of the setup options. |
| Restore Defaults | [Yes],<br>[No] | Restore / load Default values for all the setup options. |

# Appendix A: List of Acronyms

**The following table does not contain the complete acronyms used in signal names, signal type definitions or similar. A description of the signals is included in the I/O Connector and Internal connector chapters within this user guide.**

Table 50: List of Acronyms

| | |
|---|---|
| 2D | Two-Dimensional |
| 3D | Three-Dimensional |
| AT | Advanced Technology |
| ATX | Advanced Technology eXtended |
| BGA | Ball Grid Array |
| BIOS | Basic Input / Output System |
| BSP | Board Support Package |
| CMOS | Complementary Metal Oxide Semiconductor |
| CPU | Central Processing Unit |
| DC | Direct Current |
| DDC | Display Data Channel |
| DIO | Digital Input / Output |
| DP | DisplayPort |
| ECC | Error-Correcting Code |
| EEE | Electrical and Electronic Equipment |
| EOS | Electrical OverStress |
| ESD | ElectroStatic Discharge |
| GbE | Gigabit Ethernet |
| HDD | Hard Disk Drive |
| HDMI | High Definition Multimedia Interface |
| LAN | Local Area Network |
| LED | Light Emitting Device |
| LVDS | Low-Voltage Differential Signaling |
| ME F/W | Management Engine Firmware |
| mPCIe | mini Peripheral Component Interconnect express |
| NGFF | Next Generation Form Factor |
| PC-AT | Personal Computer - Advanced Technology |
| PCB | Printed Circuit Board |
| PSU | Power Supply Unit |
| PVC | PolyViny Chloride |
| PWM | Pulse Width Modulation |
| RAM | Random Access Memory |
| ROM | Read-Only Memory |
| RTC | Real-Time Clock |
| SATA | Serial Advanced Technology Attachment |
| SD | Secure Digital memory card |
| SDP | Serial Download Protocol |
| SELV | Safety Extra-Low Voltage |
| SIM | Subscriber Identity Module |
| SMBus | System Management Bus |
| SoC | System on Chip |
| SO-DIMM | Small Outline Dual In-line Memory Module |
| SPD | Serial Presence Detect |
| SPI | Serial Peripheral Interface |
| TDP | Thermal Design Power |
| TPM | Trusted Platform Module |
| UEFI | Unified Extensible Firmware Interface |
| USB | Universal Serial Bus |
| UTP | Update Transfer Protocol |
| VGA | Video Graphics Array |
| WDT | WatchDog Timer |
| WEEE | Waste Electrical and Electronic Equipment |
| | |
| | |
| | |
| | |
| | |

## About Kontron

Kontron is a global leader in Embedded Computing Technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall. For more information, please visit: **www.kontron.com**

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