

## 3.5"-SBC-TGL

Doc. User Guide, Rev. 2.5

Doc. ID: [To be Determined]

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 3.5"-SBC-TGL - USER GUIDE

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## Revision History

| Revision | Brief Description of Changes                 | Date of Issue | Author/<br>Editor |
|----------|----------------------------------------------|---------------|-------------------|
| 1.0      | Initial Issue                                | 2021-Dec-28   | YS                |
| 1.1      | Add extended temperature                     | 2022-May-06   | YS                |
| 1.2      | Modify CN9 Pin 1 voltage, GbE LED signal     | 2022-May-17   | YS                |
| 1.3      | Update LED2 color                            | 2022-Sep-05   | YS                |
| 1.4      | Update LAN1 controller                       | 2023-Mar-02   | YS                |
| 1.5      | Update Audio Codec                           | 2023-Jun-20   | YS                |
| 1.6      | Update CN19 & CN20 mating connector          | 2023-Jun-27   | YS                |
| 2.0      | Add power consumption                        | 2024-Mar-28   | YS                |
| 2.1      | Update Section 6.4 Description               | 2024-Jun-14   | YS                |
| 2.2      | Remove extended temperature                  | 2024-Aug-20   | YS                |
| 2.3      | Add a thermal design note for M.2 Key M NVMe | 2024-Dec-18   | YS                |
| 2.4      | Update CN19 & CN20 mating connector          | 2025-Feb-03   | YS                |
| 2.5      | Revise power consumption table               | 2025-Aug-15   | YS                |

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## Symbols

The following symbols may be used in this user guide

### **⚠ DANGER**

DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.

### **⚠ WARNING**

WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.

### **NOTICE**

NOTICE indicates a property damage message.

### **⚠ CAUTION**

CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.



#### Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.



#### ESD Sensitive Device!

This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.



#### HOT Surface!

Do NOT touch! Allow to cool before servicing.



#### Laser!

This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.



This symbol indicates general information about the product and the user guide.

This symbol also indicates detail information about the specific product configuration.



This symbol precedes helpful hints and tips for daily use.

## For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

### High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

#### ⚠ CAUTION

##### Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

#### ⚠ CAUTION



##### Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

### Special Handling and Unpacking Instruction

#### NOTICE



##### ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

## Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

### ⚠ CAUTION

**Danger of explosion if the battery is replaced incorrectly.**

- ▶ Replace only with same or equivalent battery type recommended by the manufacturer.
- ▶ Dispose of used batteries according to the manufacturer's instructions.

## General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

## Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit <https://www.kontron.com/about-kontron/corporate-responsibility/quality-management>.

## Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

## WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- ▶ Reduce waste arising from electrical and electronic equipment (EEE)
- ▶ Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- ▶ Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- ▶ Improve the environmental performance of all those involved during the lifecycle of EEE



**Environmental protection is a high priority with Kontron.**

**Kontron follows the WEEE directive**

**You are encouraged to return our products for proper disposal.**

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# 1/ Introduction

This user guide describes the 3.5"-SBC-TGL board made by Kontron. This board will also be denoted 3.5"-SBC-TGL within this user guide.

Use of this user guide implies a basic knowledge of PC-AT hardware and software. This user guide focuses on describing the 3.5"-SBC-TGL board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching on the power.

All configuration and setup of the CPU board is either carried out automatically or manually by the user via the BIOS setup menus.

Latest revision of this user guide, datasheet, thermal simulations, BIOS, drivers, BSP's (Board Support Packages), mechanical drawings (2D and 3D) can be downloaded from Kontron's Web Page.

## 2/ Installation Procedures

### 2.1. Installing the Board

#### NOTICE



#### ESD Sensitive Device!

Electrostatic discharge (ESD) can damage equipment and impair electrical circuitry.

- ▶ Wear ESD-protective clothing and shoes
- ▶ Wear an ESD-preventive wrist strap attached to a good earth ground
- ▶ Check the resistance value of the wrist strap periodically (1 MΩ to 10 MΩ)
- ▶ Transport and store the board in its antistatic bag
- ▶ Handle the board at an approved ESD workstation
- ▶ Handle the board only by the edges

To get the board running follow these steps. If the board shipped from KONTRON already has components like RAM and CPU cooler mounted, then skip the relevant steps below.

#### 1. Turn off the PSU (Power Supply Unit)

#### NOTICE

Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected while configuring the board. Otherwise, components (RAM, LAN cards etc.) might get damaged. Make sure to use +12 V DC single supply only with suitable cable kit and PS-ON# active.

#### NOTICE

The power supply unit shall comply with the requirements as defined in IEC 62368-1 according Clause 6.2.2 to power source category PS2 "Limited Power Source".

#### 2. Insert the DDR4 3200 module(s)

Be careful to push the memory module(s) in the slot(s) before locking the tabs.

#### 3. Connecting interfaces

Insert all external cables for hard disk, keyboard etc. A monitor must be connected in order to change BIOS settings.

#### 4. Connect and turn on PSU

Connect PSU to the board by the +12 V 3.0 mm pitch 1x4-pin wafer connector.

#### 5. BIOS setup

Enter the BIOS setup by pressing the <DEL> key during boot up.

Enter "Exit Menu" and Load Setup Defaults.



To clear all BIOS setting, including Password protection, activate "Clear CMOS Jumper" for 10 sec (without power connected).

#### 6. Mounting the board in chassis

#### NOTICE

When mounting the board to chassis etc. please note that the board contains components on both sides of the PCB that can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the board on a chassis, it is recommended to use screws with an integrated washer and a diameter of > 7 mm. Do not use washers with teeth, as they can damage the PCB and cause short circuits.

## 2.2. Chassis Safety Standards

Before installing the 3.5"-SBC-TGL in the chassis, users must evaluate the end product to ensure compliance with the requirements of the IEC60950-1 safety standard:

- ▶ The board must be installed in a suitable mechanical, electrical and fire enclosure.
- ▶ The system, in its enclosure, must be evaluated for temperature and airflow considerations.
- ▶ The board must be powered by a CSA or UL approved power supply that limits the maximum input current.
- ▶ For interfaces having a power pin such as external power or fan, ensure that the connectors and wires are suitably rated. All connections from and to the product shall be with SELV circuits only.
- ▶ Wires have suitable rating to withstand the maximum available power.
- ▶ The peripheral device enclosure fulfils the IEC60950-1 fire protecting requirements.

## 2.3. Lithium Battery Replacement

If replacing the lithium battery follow the replacement precautions stated in the notification below:

### **⚠ CAUTION**

**Danger of explosion if the lithium battery is incorrectly replaced.**

- ▶ Replace only with the same or equivalent type recommended by the manufacturer
- ▶ Dispose of used batteries according to the manufacturer's instructions

**VORSICHT! Explosionsgefahr bei unsachgemäßem Austausch der Batterie.**

- ▶ Ersatz nur durch denselben oder einen vom Hersteller empfohlenen gleichwertigen Typ
- ▶ Entsorgung gebrauchter Batterien nach Angaben des Herstellers

**ATTENTION! Risque d'explosion avec l'échange inadéquat de la batterie.**

- ▶ Remplacement seulement par le même ou un type équivalent recommandé par le producteur
- ▶ L'évacuation des batteries usagées conformément à des indications du fabricant

**PRECAUCION! Peligro de explosión si la batería se sustituye incorrectamente.**

- ▶ Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante
- ▶ Disponga las baterías usadas según las instrucciones del fabricante

**ADVARESEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering.**

- ▶ Udskiftning må kun ske med batteri af samme fabrikat og type
- ▶ Levér det brugte batteri tilbage til leverandøren

**ADVARESEL! Eksplosjonsfare ved feilaktig skifte av batteri.**

- ▶ Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten
- ▶ Brukte batterier kasseres i henhold til fabrikantens instruksjoner

**VARNING! Explosionsfara vid felaktigt batteribyte.**

- ▶ Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren
- ▶ Kassera använt batteri enligt fabrikantens instruktion

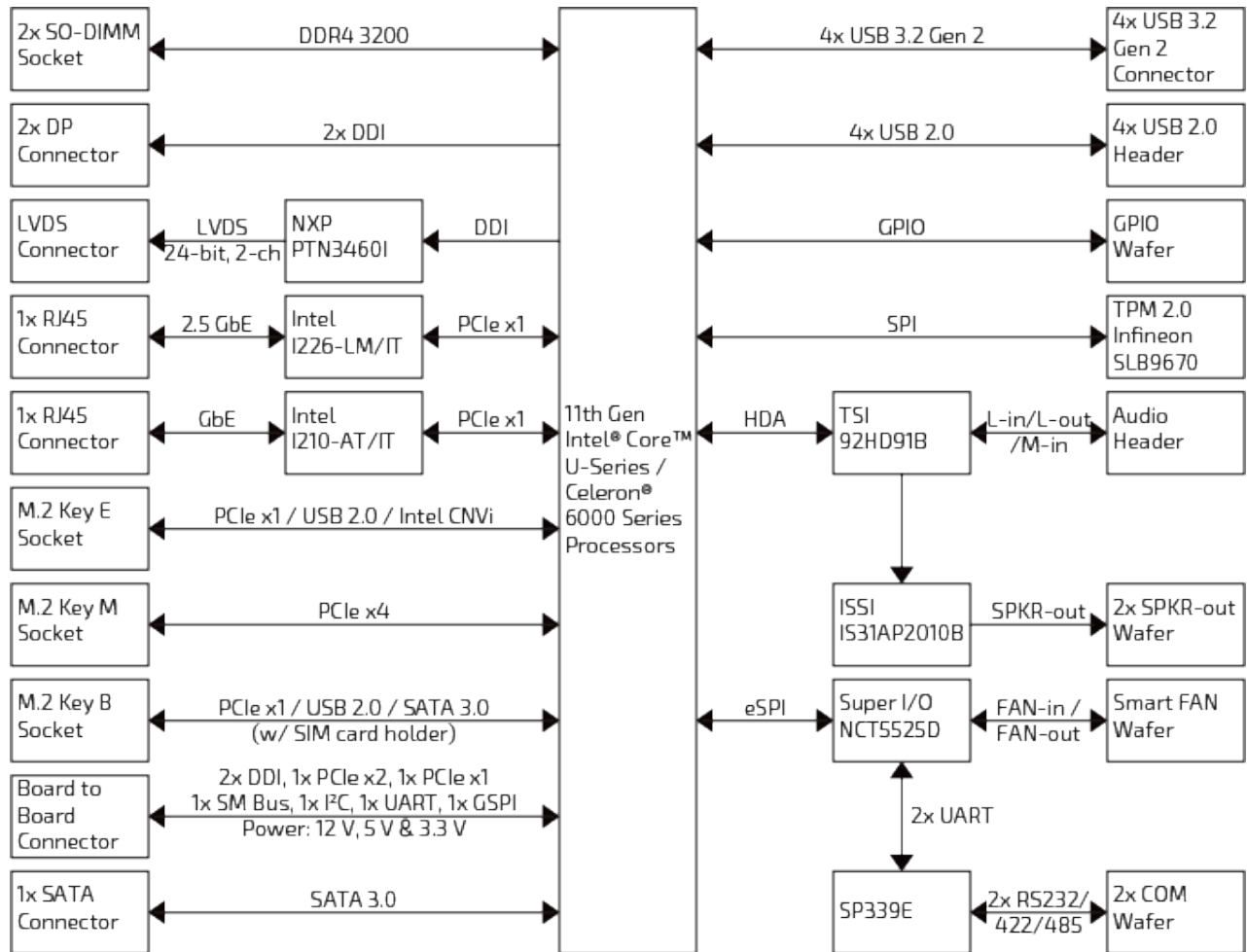
**VAROITUS! Paristo voi räjähtää, jos se on virheellisesti asennettu.**

- ▶ Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiä
- ▶ Hävitä käytetty paristo valmistajan ohjeiden mukaisesti

## 3/ System Specifications

### 3.1. System Block Diagram

Figure 1: System Block Diagram 3.5"-SBC-TGL



## 3.2. Component Main Data

The table below summarizes the features of the 3.5"-SBC-TGL single board computer.

Table 1: Component Main Data

| System                 |                                                                                                                                                                                                                                                                                           |
|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Processor              | <ul style="list-style-type: none"> <li>▶ 11th Generation Intel® Core™ U-Series Processors</li> <li>▶ Intel® Celeron® 6000 Series Processors</li> </ul>                                                                                                                                    |
| Memory                 | ▶ 2x DDR4 SO-DIMM                                                                                                                                                                                                                                                                         |
| Video                  |                                                                                                                                                                                                                                                                                           |
| Display Interface      | <ul style="list-style-type: none"> <li>▶ 1x LVDS</li> <li>▶ 2x DP (on rear)</li> </ul>                                                                                                                                                                                                    |
| Multiple Display       | ▶ Quadruple (more display I/Os supported via extended B2B connector)                                                                                                                                                                                                                      |
| Audio                  |                                                                                                                                                                                                                                                                                           |
| Audio Codec            | ▶ TSI 92HD91B                                                                                                                                                                                                                                                                             |
| Audio Display          | <ul style="list-style-type: none"> <li>▶ 2x Speaker-out (Right &amp; Left, 3 W)</li> <li>▶ 1x Line-in (by header)</li> <li>▶ 1x Line-out (by header)</li> <li>▶ 1x Mic-in (by header)</li> </ul>                                                                                          |
| Network Connection     |                                                                                                                                                                                                                                                                                           |
| Ethernet               | <ul style="list-style-type: none"> <li>▶ 1x 2.5 GbE LAN (RJ45 on rear, Intel® I226-LM/IT)</li> <li>▶ 1x GbE LAN (RJ45 on rear, Intel® I210-AT/IT)</li> </ul>                                                                                                                              |
| Peripheral Connection  |                                                                                                                                                                                                                                                                                           |
| USB                    | <ul style="list-style-type: none"> <li>▶ 4x USB 3.2 Gen 2 (Type A on rear)</li> <li>▶ 4x USB 2.0 (by header)</li> </ul>                                                                                                                                                                   |
| Serial Port            | ▶ 2x RS232/422/485 (by header)                                                                                                                                                                                                                                                            |
| Other I/Os             | ▶ 8-bit DIO (by header)                                                                                                                                                                                                                                                                   |
| Storage & Expansion    |                                                                                                                                                                                                                                                                                           |
| SATA                   | ▶ 1x SATA 3.0                                                                                                                                                                                                                                                                             |
| M.2                    | <ul style="list-style-type: none"> <li>▶ 1x M.2 Key B (Type 2242 / 3042 / 2280, mixed w/ PCIe x1 / USB 2.0 / SATA 3.0)</li> <li>▶ 1x M.2 Key E (Type 2230, mixed w/ PCIe x1 / USB 2.0 / UART / PCM, Intel® CNVi support)</li> <li>▶ 1x M.2 Key M (Type 2280, mixed w/ PCIe x4)</li> </ul> |
| SIM Card Holder        | ▶ 1x SIM Card Holder (Micro type, connected to M.2 Key B)                                                                                                                                                                                                                                 |
| Extended B2B Connector | <ul style="list-style-type: none"> <li>▶ 2x DDI (1x eDP / DP support, 1x DP support)</li> <li>▶ 1x PCIe x2</li> <li>▶ 1x PCIe x1</li> <li>▶ 1x SM Bus</li> <li>▶ 1x I2C</li> <li>▶ 1x UART</li> <li>▶ 1x GSPI</li> </ul>                                                                  |
| Power                  |                                                                                                                                                                                                                                                                                           |

|                                        |                                                                                                                                                                                              |
|----------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>System</b>                          |                                                                                                                                                                                              |
| <b>Input Voltage</b>                   | ▶ DC 12 V                                                                                                                                                                                    |
| <b>Connector</b>                       | ▶ 1x4-pin pitch 3.0 mm Wafer                                                                                                                                                                 |
| <b>Firmware</b>                        |                                                                                                                                                                                              |
| <b>BIOS</b>                            | ▶ AMI uEFI BIOS w/ 256 Mb SPI Flash                                                                                                                                                          |
| <b>Watchdog</b>                        | ▶ Programmable WDT to generate system reset event                                                                                                                                            |
| <b>H/W Monitor</b>                     | ▶ Voltages<br>▶ Temperatures                                                                                                                                                                 |
| <b>Real Time Clock</b>                 | ▶ Processor integrated RTC                                                                                                                                                                   |
| <b>Security</b>                        | ▶ TPM 2.0 (Infineon SLB 9670)                                                                                                                                                                |
| <b>System Control &amp; Monitoring</b> |                                                                                                                                                                                              |
| <b>Front Panel Header</b>              | ▶ 1x Header Reset Button, HDD LED & External Speaker<br>▶ 1x Header for Power Button, Power LED & SM bus<br>▶ 1x Header for M.2 Key B activity LED<br>▶ 1x Header for M.2 Key E activity LED |
| <b>Button, Switch &amp; Indicator</b>  | ▶ 1x Standby LED (Yellow, on rear)<br>▶ 1x Power LED (Green, on rear)<br>▶ 1x Power Button (on rear)                                                                                         |
| <b>Cooling</b>                         |                                                                                                                                                                                              |
| <b>Fan</b>                             | ▶ 1x Wafer for System Fan                                                                                                                                                                    |
| <b>Software</b>                        |                                                                                                                                                                                              |
| <b>OS Support</b>                      | ▶ Windows 10<br>▶ Linux                                                                                                                                                                      |
| <b>Mechanical</b>                      |                                                                                                                                                                                              |
| <b>Dimension (L x W)</b>               | ▶ ECX (146 mm x 105 mm / 5.75" x 4.13")                                                                                                                                                      |

### 3.3. Environmental Conditions

The 3.5"-SBC-TGL is compliant with the following environmental conditions. It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within the allowed temperature range.

Table 2: Environmental Conditions

|                              |                                              |
|------------------------------|----------------------------------------------|
| <b>Operating Temperature</b> | ▶ 0 °C ~ 60 °C / 32 °F ~ 140 °F (Standard)   |
|                              | ▶ -40 °C ~ 85 °C / -40 °F ~ 185 °F (Extreme) |
| <b>Storage Temperature</b>   | ▶ -20 °C ~ 80 °C / -4 °F ~ 176 °F (Standard) |
|                              | ▶ -55 °C ~ 85 °C / -67 °F ~ 185 °F (Extreme) |
| <b>Humidity</b>              | ▶ 0 % ~ 95 %                                 |

### 3.4. Standards and Certifications

The 3.5"-SBC-TGL meets the following standards and certification tests.

Table 3: Standards and Certifications

|                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>CE Class B</b>  | <ul style="list-style-type: none"> <li>▶ EN 55032: 2015 + A11: 2020, Class B</li> <li>▶ CISPR 32: 2015</li> <li>▶ EN 61000-3-2: 2014</li> <li>▶ EN 61000-3-3: 2013</li> <li>▶ EN 55024: 2010 + A1: 2015</li> <li>▶ IEC 61000-4-2: 2008</li> <li>▶ IEC 61000-4-3: 2006 + A1: 2007 + A2: 2010</li> <li>▶ IEC 61000-4-4: 2012</li> <li>▶ IEC 61000-4-5: 2014 + A1: 2017</li> <li>▶ IEC 61000-4-6: 2013</li> <li>▶ IEC 61000-4-8: 2009</li> <li>▶ IEC 61000-4-11: 2004 + A1: 2017</li> </ul> |
| <b>FCC Class B</b> | <ul style="list-style-type: none"> <li>▶ FCC CFR Title 47 Part 15 Subpart B, Class B</li> <li>▶ ICES-003 Issue 7: 2020 Class B</li> <li>▶ ANSI C63.4: 2014</li> <li>▶ ANSI C63.4a: 2017</li> </ul>                                                                                                                                                                                                                                                                                       |

### 3.5. Processor Support

The 3.5"-SBC-TGL is designed to support 11th Generation Intel® Core™ U-Series and Intel® Celeron® 6000 Series Processors. The BGA CPU is remounted from factory. Kontron has defined the board versions as listed in the following table, so far all based on Embedded CPUs. Other versions are expected at a later date.

**Table 4: Processor Support**

| Name             | Core # | Speed (GHz) | Turbo (GHz) | Embdd. | Cache | Socket  | TDP (W) | TDP-up (W) | TDP-down (W) | Tj (° C) |
|------------------|--------|-------------|-------------|--------|-------|---------|---------|------------|--------------|----------|
| Core™ i7-1185GRE | 4      | 1.80        | 4.40        | Yes    | 12M   | BGA1449 | 15      | 28         | 12           | 100      |
| Core™ i7-1185G7E | 4      | 1.80        | 4.40        | Yes    | 12M   | BGA1449 | 15      | 28         | 12           | 100      |
| Core™ i5-1145GRE | 4      | 1.50        | 4.10        | Yes    | 8M    | BGA1449 | 15      | 28         | 12           | 100      |
| Core™ i5-1145G7E | 4      | 1.50        | 4.10        | Yes    | 8M    | BGA1449 | 15      | 28         | 12           | 100      |
| Core™ i3-1115G4E | 2      | 2.20        | 3.90        | Yes    | 6M    | BGA1449 | 15      | 28         | 12           | 100      |
| Celeron® 6305E   | 2      | 1.80        | -           | Yes    | 4M    | BGA1449 | 15      | -          | -            | 100      |

Sufficient cooling must be applied to the CPU in order to remove the effect as listed as TDP (Thermal Design Power) in above table. The sufficient cooling is also depending on the worst case maximum ambient operating temperature and the actual worst case load of processor.

### 3.6. System Memory Support

The 3.5"-SBC-TGL has two DDR4 SO-DIMM sockets. The sockets support the following memory features:

- ▶ 2x DDR4 SO-DIMM 260-pin
- ▶ Dual-channel with 1x SO-DIMM per channel
- ▶ Up to 64 GB
- ▶ SPD timing supported
- ▶ ECC not supported

The installed DDR4 SO-DIMM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted, or the board may not be able to boot totally.

#### 3.6.1. Memory Operating Frequencies

In all modes, the frequency of system memory is the lowest frequency of all the memory modules placed in the system. Each memory module's frequency can be determined through the SPD registers on the memory modules.

The table below lists the resulting operating memory frequencies based on the combination of SO-DIMMs and processor.

**Table 5: Memory Operating Frequencies**

| SO-DIMM Type | Module Name | Memory Data Transfer (MT/s) | Processor System Bus Frequency (MHz) | Resulting Memory Clock Frequency (MHz) | Peak Transfer Rate (MB/s) |
|--------------|-------------|-----------------------------|--------------------------------------|----------------------------------------|---------------------------|
| DDR4 3200    | PC4-25600   | 3200                        | 1600                                 | 400                                    | 25600                     |

Memory modules have in general a much lower longevity than embedded motherboards, and therefore EOL of modules can be expected several times during lifetime of the motherboard.

As a minimum it is recommend using Kontron memory modules for prototype system(s) in order to prove stability of the system and as for reference.

For volume production you might request to test and qualify other types of RAM. In order to qualify RAM it is recommend configuring 3 systems running RAM Stress Test program in heat chamber at 60° C for a minimum of 24 hours.

### 3.7. On-board Graphics Subsystem

The 3.5"-SBC-TGL supports either Intel® Iris® Xe Graphics integrated in Core™ i7 / i5 Series processors or Intel® UHD Graphics technology in Core™ i3 / Celeron® Series processors for high quality graphics capabilities. All 3.5"-SBC-TGL versions support quadruple displays pipes.

Quadruple displays can be used simultaneously and be used to implement independent or cloned display configuration.

The 3.5"-SBC-TGL itself provides one internal LVDS interface and two external DP connectors. It supports additional two DDI (Digital Display Interface) signals via the extended B2B connector (CN28). One DDI can support eDP or DP port; the other DDI can support DP port.

The model with Intel® Core™ i7 / i5 Series processors can support up to two 8K DP displays and that with Intel® Core™ i3 / Celeron® Series processors can support one 8K DP display.

**Table 6: Quadruple-displays Configurations**

| No. | Display 1                     | Display 2                  | Display 3                                            | Display 4                                            |
|-----|-------------------------------|----------------------------|------------------------------------------------------|------------------------------------------------------|
| 1   | LVDS                          | DP                         | DP                                                   | DDI0                                                 |
| 2   | LVDS                          | DP                         | DP                                                   | DDI1                                                 |
| 3   | LVDS                          | DP                         | DDI0                                                 | DDI1                                                 |
| 4   | DP                            | DP                         | DDI0                                                 | DDI1                                                 |
| No. | Max. Resolution (Px) at 60 Hz |                            |                                                      |                                                      |
|     | Display 1                     | Display 2                  | Display 3                                            | Display 4                                            |
| 1   | 1920 x 1200                   | 7680 x 4320 / 4096 x 2304* | 7680 x 4320 / 4096 x 2304*                           | 4096 x 2304 (eDP)<br>7680 x 4320 / 4096 x 2304* (DP) |
| 2   | 1920 x 1200                   | 7680 x 4320 / 4096 x 2304* | 7680 x 4320 / 4096 x 2304*                           | 7680 x 4320 / 4096 x 2304* (DP)                      |
| 3   | 1920 x 1200                   | 7680 x 4320 / 4096 x 2304* | 4096 x 2304 (eDP)<br>7680 x 4320 / 4096 x 2304* (DP) | 7680 x 4320 / 4096 x 2304* (DP)                      |
| 4   | 7680 x 4320 / 4096 x 2304     | 7680 x 4320 / 4096 x 2304* | 4096 x 2304 (eDP)<br>7680 x 4320 / 4096 x 2304* (DP) | 7680 x 4320 / 4096 x 2304* (DP)                      |



\* The model with Intel® Core™ i7 / i5 Series processors can support up to two 8K DP displays and that with Intel® Core™ i3 / Celeron® Series processors can support one 8K DP display.

### 3.8. Power Supply Voltage

In order to ensure safe operation of the board, the input power supply must monitor the supply voltage and shut down if the supply is out of range – refer to the actual power supply specification. Please note, in order to keep the power consumption to a minimal level, boards do not implement a guaranteed minimum load. The 3.5"-SBC-TGL board must be powered through the 3.0 mm pitch 1x4-pin wafer connector from a DC 12 V power supply.

#### NOTICE

Hot Plugging power supply is not supported. Hot plugging might damage the board.

The requirements to the supply voltages are as follows:

Table 7: Supply Voltages

| Supply | Min.   | Max.   | Note                          |
|--------|--------|--------|-------------------------------|
| +12 V  | 11.4 V | 12.6 V | Should be $\pm 5\%$ tolerance |

### 3.9. Power Consumption

The power consumption is measured under the following software and hardware test condition.

- ▶ 3.5"-SBC-TGL with Intel® Core™ i5-1145GRE processor (Quad Core @ 1.50 GHz)
- ▶ Memory: 2x 8 GByte DDR4
- ▶ Storage: 128 GByte Phison SATA SSD
- ▶ Operating System: Windows 10 Enterprise LTSC 21H2

The power consumption in different modes is as follows:

Table 8: Supply Voltages

| Power Status       | Input Voltage | Power Consumption |
|--------------------|---------------|-------------------|
| Boot (Peak)        | +12 V         | 71.04 W           |
| Idle (S0)          | +12 V         | 14.28 W           |
| Full Run (S0)      | +12 V         | 37.8 W            |
| Sleep (S3)         | +12 V         | 614.16 mW         |
| Shutdown (S4 / S5) | +12 V         | 471.17 mW         |
| Shutdown (PSM)     | +12 V         | 61.92 mW          |

## 4/ Connector Locations

### 4.1. Top Side

Figure 2: Top Side

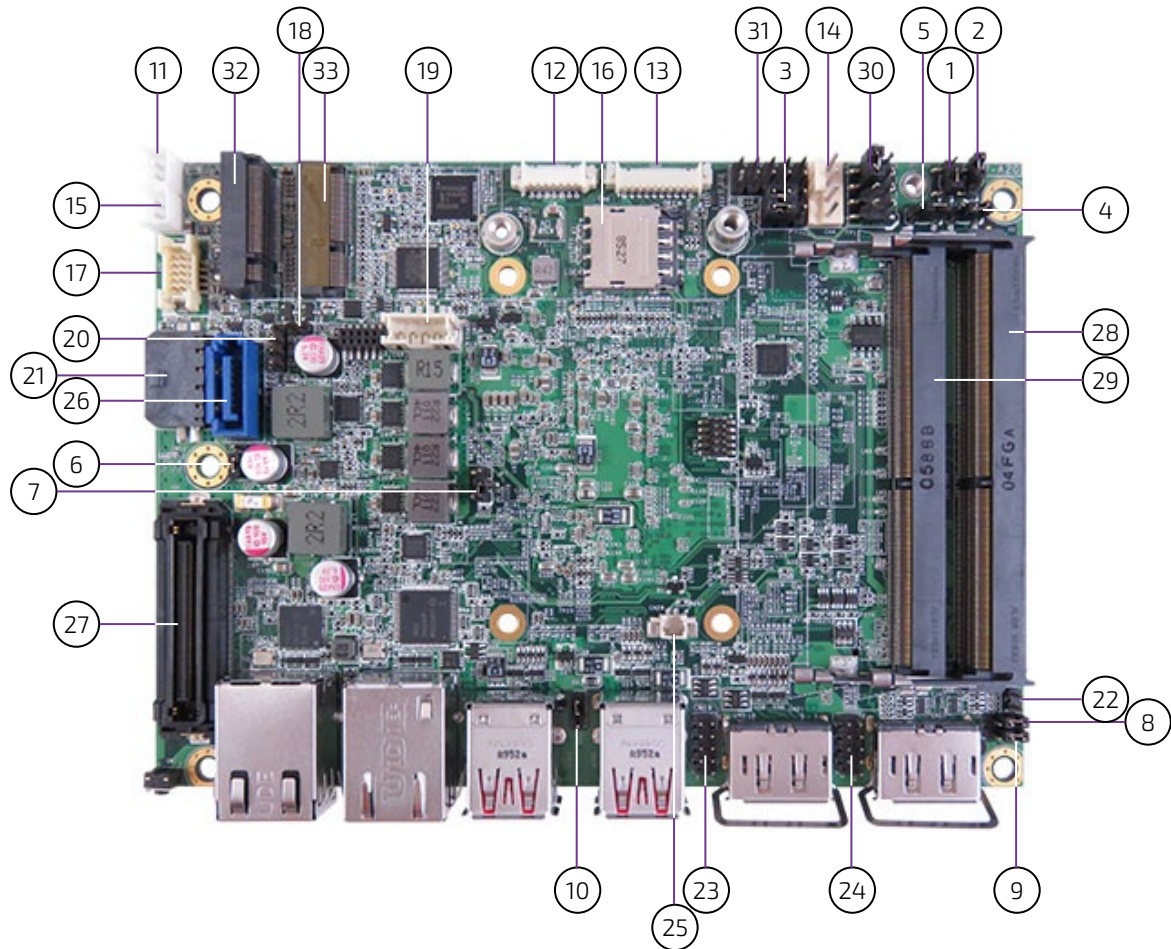


Table 9: Jumper List

| Item | Designation | Description                                  | See Chapter |
|------|-------------|----------------------------------------------|-------------|
| 1    | JP1         | LVDS Backlight Control Selection             | 7.19.1      |
| 2    | JP2         | M.2 Key B Selection                          | 7.19.2      |
| 3    | JP3         | LVDS Panel Power Selection                   | 7.19.3      |
| 4    | JP4         | LVDS Backlight Enable Selection              | 7.19.4      |
| 5    | JP5         | LVDS Backlight Enable Voltage Selection      | 7.19.5      |
| 6    | JP6         | Flash Descriptor Security Override Selection | 7.19.6      |
| 7    | JP7         | AT / ATX Power Mode Selection                | 7.19.7      |
| 8    | JP8         | Clear CMOS Selection                         | 7.19.8      |
| 9    | JP9         | MFG Mode Selection                           | 7.19.9      |
| 10   | JP10        | USB Power Selection                          | 7.19.10     |

Table 10: Top Side Internal Connector Pin Assignment

| Item | Designation | Description                          | See Chapter |
|------|-------------|--------------------------------------|-------------|
| 11   | CN1         | Left Channel Audio AMP Output Wafer  | 7.6         |
| 12   | CN2         | LVDS Backlight Power Wafer           | 7.11        |
| 13   | CN3         | DIO Header                           | 7.12        |
| 14   | CN4         | Fan Wafer                            | 7.2         |
| 15   | CN5         | Right Channel Audio AMP Output Wafer | 7.6         |
| 16   | CN6         | Micro SIM Card Holder for M2B1       | 7.16        |
| 17   | CN7         | Audio Input / Output Header          | 7.7         |
| 18   | CN8         | Activity Indicator Header for M2B1   | 7.17        |
| 19   | CN9         | SATA Power Output Wafer              | 7.4         |
| 20   | CN11        | Activity Indicator Header for M2E1   | 7.17        |
| 21   | CN12        | +12 V DC Power Input Wafer           | 7.1.1       |
| 22   | CN14        | Activity Indicator Header for M2M1   | 7.17        |
| 23   | CN19        | USB 2.0 Port 5, 6 Header             | 7.5         |
| 24   | CN20        | USB 2.0 Port 7, 8 Header             | 7.5         |
| 25   | CN26        | RTC Power Input Wafer                | 7.1.2       |
| 26   | CN27        | SATA Port 0 Connector                | 7.3         |
| 27   | CN28        | Extended B2B Connector               | 7.18        |
| 28   | DIMM1       | DDR4 Channel 0 SO-DIMM Slot          | 3.6         |
| 29   | DIMM2       | DDR4 Channel 1 SO-DIMM Slot          | 3.6         |
| 30   | FP1         | Front Panel Header 1                 | 7.8         |
| 31   | FP2         | Front Panel Header 2                 | 7.8         |
| 32   | M2B1        | M.2 Key B 2242 / 3042 / 2280 Slot    | 7.13        |
| 33   | M2E1        | M.2 Key E 2230 Slot                  | 7.14        |

## 4.2. Rear Side

Figure 3: Rear Side

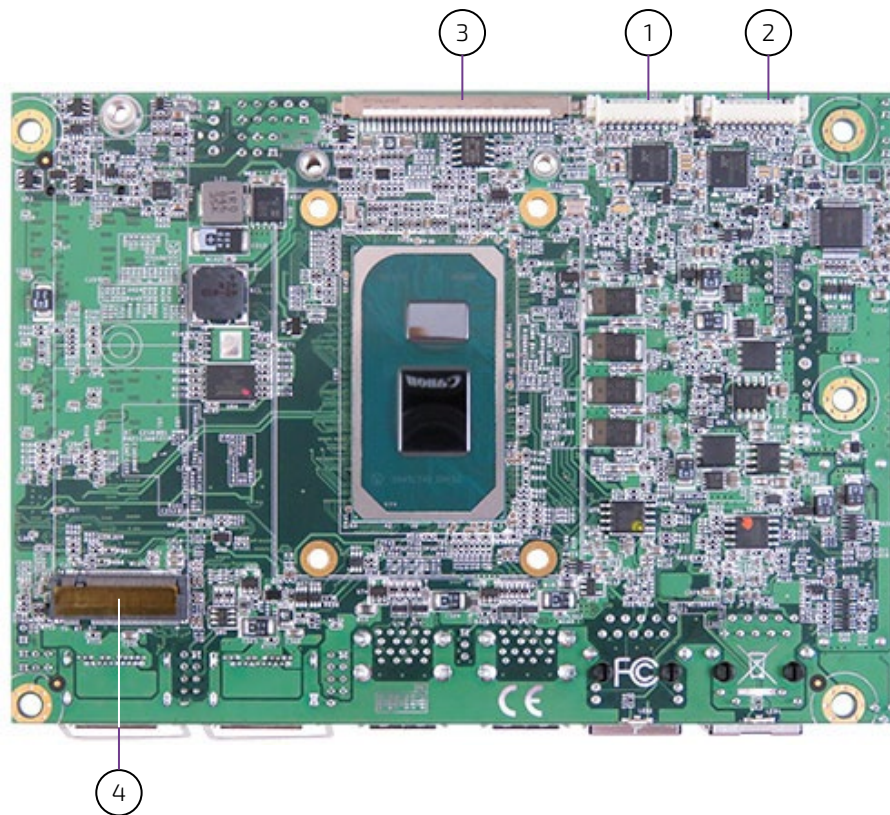


Table 11: Rear Side Internal Connector Pin Assignment

| Item | Designation | Description                  | See Chapter |
|------|-------------|------------------------------|-------------|
| 1    | CN23        | RS232/422/485 COM2 Wafer     | 7.9         |
| 2    | CN24        | RS232/422/485 COM1 Wafer     | 7.9         |
| 3    | CN25        | 24-bit / 2-ch LVDS Connector | 7.10        |
| 4    | M2M1        | M.2 Key M 2280 Slot          | 7.15        |

### 4.3. Connector Panel Side

Figure 4: Connector Panel Side

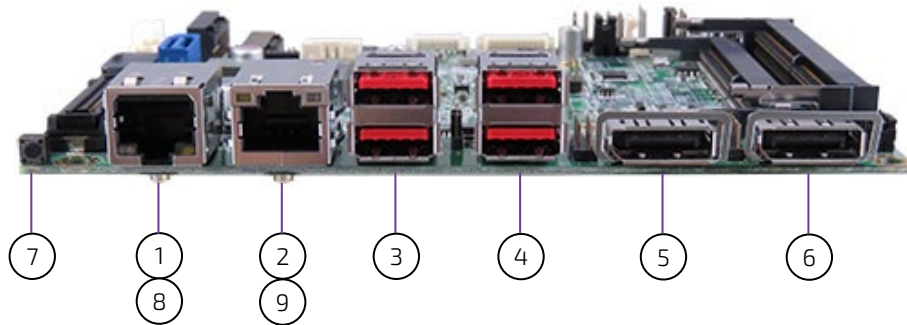


Table 12: Connector Panel Side Connector List

| Item | Designation | Description                              | See Chapter |
|------|-------------|------------------------------------------|-------------|
| 1    | CN15        | 2.5GbE LAN1 RJ45 Connector               | 6.2         |
| 2    | CN16        | GbE LAN2 RJ45 Connector                  | 6.2         |
| 3    | CN17        | USB 3.2 Gen 2 Port 3, 4 Type A Connector | 6.3         |
| 4    | CN18        | USB 3.2 Gen 2 Port 1, 2 Type A Connector | 6.3         |
| 5    | CN21        | DP Port 1 Connector                      | 6.1         |
| 6    | CN22        | DP Port 2 Connector                      | 6.1         |
| 7    | SW1         | Power Button                             | 6.4         |
| 8    | LED1        | Power LED                                | 6.5         |
| 9    | LED2        | Standby LED                              | 6.5         |

## 5/ Connector Definitions

The following defined terms are used within this user guide to give more information concerning the pin assignment and to describe the connector's signals.

| Defined Term | Description                                                                                                           |
|--------------|-----------------------------------------------------------------------------------------------------------------------|
| Pin          | Shows the pin numbers in the connector                                                                                |
| Signal       | The abbreviated name of the signal at the current pin<br>The notation "XX#" states that the signal "XX" is active low |
| Note         | Special remarks concerning the signal                                                                                 |
| Designation  | Type and number of item described                                                                                     |
| See Chapter  | Number of the chapter within this user guide containing a detailed description                                        |

The abbreviation TBD is used for specifications that are not available yet or which are not sufficiently specified by the component vendors.

## 6/ I/O-Area Connectors

### 6.1. DP Connector (CN21 & CN22)

The DP (DisplayPort) connectors are based on standard DP female port.

Figure 5: DP Connector CN21, CN22

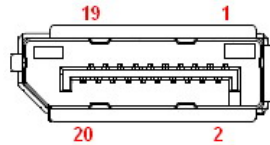


Table 13: Pin Assignment DP Connector CN21, CN22

| Pin | Signal    | Description                                                       | Note |
|-----|-----------|-------------------------------------------------------------------|------|
| 1   | ML_Lane0p | DisplayPort Lane 0 transmitter differential pair (+)              |      |
| 2   | GND       | Ground                                                            |      |
| 3   | ML_Lane0n | DisplayPort Lane 0 transmitter differential pair (-)              |      |
| 4   | ML_Lane1p | DisplayPort Lane 1 transmitter differential pair (+)              |      |
| 5   | GND       | Ground                                                            |      |
| 6   | ML_Lane1n | DisplayPort Lane 1 transmitter differential pair (-)              |      |
| 7   | ML_Lane2p | DisplayPort Lane 2 transmitter differential pair (+)              |      |
| 8   | GND       | Ground                                                            |      |
| 9   | ML_Lane2n | DisplayPort Lane 2 transmitter differential pair (-)              |      |
| 10  | ML_Lane3p | DisplayPort Lane 3 transmitter differential pair (+)              |      |
| 11  | GND       | Ground                                                            |      |
| 12  | ML_Lane3n | DisplayPort Lane 3 transmitter differential pair (-)              |      |
| 13  | Config1   | Connected to ground, either directly or through a pulldown device |      |
| 14  | Config2   | Connected to ground, either directly or through a pulldown device |      |
| 15  | AUX_CHp   | DisplayPort Auxiliary channel differential pair (+)               |      |
| 16  | GND       | Ground                                                            |      |
| 17  | AUX_CHn   | DisplayPort Auxiliary channel differential pair (-)               |      |
| 18  | Hot_Plug  | DisplayPort hot plug detect                                       |      |
| 19  | GND       | Ground                                                            |      |
| 20  | DP_PWR    | Power for connector                                               |      |

## 6.2. Ethernet Connectors (CN15 & CN16)

The 3.5"-SBC-TGL supports one channel of 10/100/1000/2500 Mbit Ethernet and one channel of 10/100/1000 Mbit Ethernet, which are based Intel® I226-LM/IT and Intel® I210-AT/IT controller respectively.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100 MByte and Category 5E, 6 or 6E with 1 Gbit/2.5Gbit LAN networks.

The signals for the Ethernet ports are as follows:

Figure 6: Ethernet Connector CN15

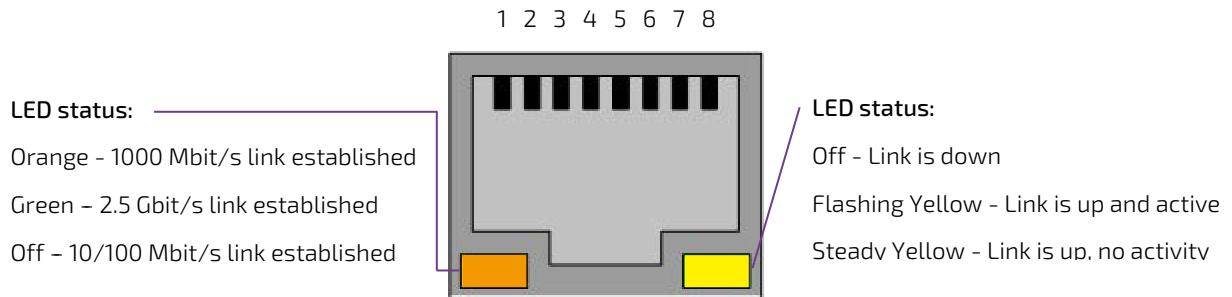


Figure 7: Ethernet Connector CN16

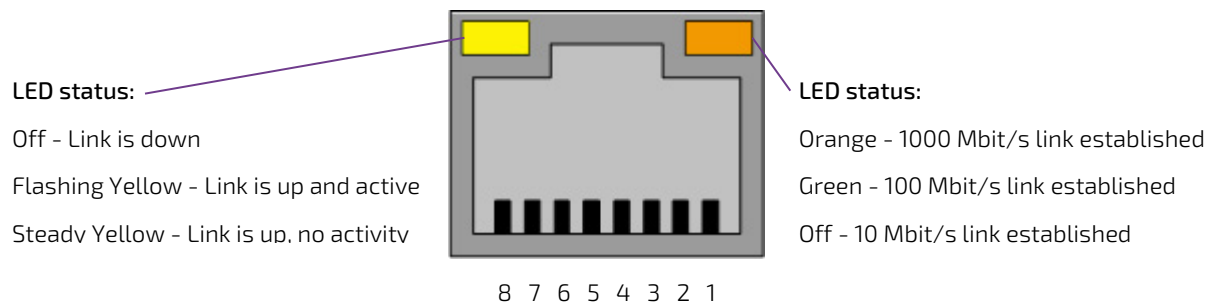


Table 14: Pin Assignment Ethernet Connectors CN15, CN16

| Pin | Signal | Note |
|-----|--------|------|
| 1   | TX1+   |      |
| 2   | TX1-   |      |
| 3   | TX2+   |      |
| 4   | TX3+   |      |
| 5   | TX3-   |      |
| 6   | TX2-   |      |
| 7   | TX4+   |      |
| 8   | TX4-   |      |

### Signal Description

| Signal | Description |
|--------|-------------|
|--------|-------------|

| Signal      | Description                                                                                                                                                                                                                                                     |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TX1+ / TX1- | In MDI mode, this is the first pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.  |
| TX2+ / TX2- | In MDI mode, this is the second pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. |
| TX3+ / TX3- | In MDI mode, this is the third pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.                                                                                                           |
| TX4+ / TX4- | In MDI mode, this is the fourth pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.                                                                                                          |

'MDI' – media dependent Interface

### 6.3. USB Connectors (I/O Area)

The external I/O connector panel supports two dual USB 3.2 Gen 2 connectors.



USB 3.2 Gen 2 ports are backward compatible with USB 2.0.

Figure 8: USB 3.2 Gen 2 Connectors CN17 - Top & Bottom, CN18 - Top & Bottom



Table 15: Pin Assignment USB 3.2 Gen 2 / USB 2.0 Connectors CN17 - Top & Bottom, CN18 - Top & Bottom

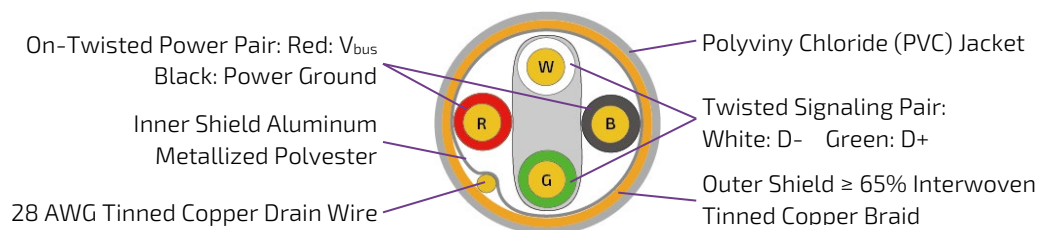
| Pin | Signal    | Description                               | Note |
|-----|-----------|-------------------------------------------|------|
| 1   | +USB_VCC* | +5 V power supply for USB device          |      |
| 2   | USB_D-    | USB 2.0 differential pair (-)             |      |
| 3   | USB_D+    | USB 2.0 differential pair (+)             |      |
| 4   | GND       | Ground                                    |      |
| 5   | USB_RX-   | USB 3.2 receiver differential pair (-)    |      |
| 6   | USB_RX+   | USB 3.2 receiver differential pair (+)    |      |
| 7   | GND       | Ground                                    |      |
| 8   | USB_TX-   | USB 3.2 transmitter differential pair (-) |      |
| 9   | USB_TX+   | USB 3.2 transmitter differential pair (+) |      |



\* The power source of +USB\_VCC can be selected by JP10.

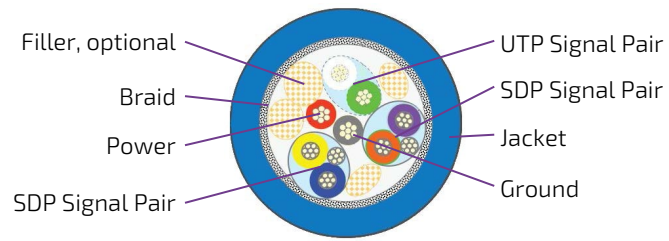
For HiSpeed rates it is required to use a USB cable, which is specified in USB 2.0 standard:

Figure 9: USB 2.0 High Speed Cable



For USB 3.2 Gen 2 cabling it is required to use only HiSpeed USB cable, specified in USB 3.2 standard:

Figure 10: USB 3.2 High Speed Cable



## 6.4. Power Button (SW1)

SW1 carries the same functionality as the PWRBTN signal on the external I/O connector.

## 6.5. LED Indicators (LED1 & LED2)

The external I/O connector panel supports one power LED indicator and one standby LED indicator for power and standby status indication.

**Table 16: LED Indicators LED1, LED2**

| LED Status       |                    | Description                           |
|------------------|--------------------|---------------------------------------|
| Power LED (LED1) | Standby LED (LED2) |                                       |
| Green LED On     | Yellow LED On      | S0 (Full On)                          |
| Green LED Blink  | Yellow LED On      | S3 (Suspend-To-RAM)                   |
| LED Off          | Yellow LED On      | S4 (Suspend-To-Disk) or S5 (Soft Off) |
| LED Off          | LED Off            | EUP Mode or G3 (Mechanical Off)       |

## 7/ Internal Connectors

### 7.1. Power Connector

Power connector must be used to supply the board with +12 VDC ( $\pm 5\%$ ).

#### NOTICE

Hot plugging any of the power connector is not allowed.

Hot plugging might damage the board. In other words, turn off main supply etc. to make sure all the power lines are turned off when connecting to the motherboard.

#### 7.1.1. Power Input Wafer (CN12)

The 1x4-pin 3.0 mm pitch power input wafer provides +12 V DC to the board.

Figure 11: Power Input Wafer CN12

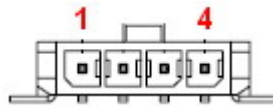


Table 17: Pin Assignment CN12

| Pin                        | Signal        | Description | Note |
|----------------------------|---------------|-------------|------|
| 1                          | +12Vin        | Power +12 V |      |
| 2                          | GND           | Ground      |      |
| 3                          | GND           | Ground      |      |
| 4                          | +12Vin        | Power +12 V |      |
| <b>Connector Type</b>      |               |             |      |
| B2W, 1x4-pin, 3.0 mm pitch |               |             |      |
| <b>Mating Connector</b>    |               |             |      |
| Vendor                     | Pinrex        |             |      |
| Housing Model No.          | 733-75-M104B6 |             |      |
| Terminal Model No.         | 733-70-FT0006 |             |      |

### 7.1.2. RTC Power Input Wafer (CN26)

The 1x2-pin 1.25 mm pitch RTC power input wafer is intended to be connected to the battery. The battery provides power to the system clock to retain the time when power is turn off.

Figure 12: RTC Power Input Wafer CN26



Table 18: Pin Assignment CN26

| Pin                         | Signal        | Description                          | Note |
|-----------------------------|---------------|--------------------------------------|------|
| 1                           | +VRTC         | Real-time clock backup battery input |      |
| 2                           | GND           | Ground                               |      |
| <b>Connector Type</b>       |               |                                      |      |
| B2W, 1x2-pin, 1.25 mm pitch |               |                                      |      |
| <b>Mating Connector</b>     |               |                                      |      |
| Vendor                      | Pinrex        |                                      |      |
| Housing Model No.           | 712-75-02W001 |                                      |      |
| Terminal Model No.          | 712-70-T00001 |                                      |      |

## 7.2. Fan Wafer (CN4)

The 1x4-pin 2.54 mm pitch fan wafer (CN4) is used for the connection of the fan for the processor or system.

Figure 13: Fan Wafer CN4

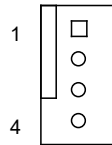


Table 19: Pin Assignment CN4

| Pin                         | Signal | Description                                                                                 | Note     |
|-----------------------------|--------|---------------------------------------------------------------------------------------------|----------|
| 1                           | GND    | Power supply ground signal                                                                  |          |
| 2                           | +12V   | +12 V power supply for fan                                                                  | 1 A max. |
| 3                           | SENSE  | Sense input signal from the fan, for rotation speed supervision RPM (Rotations Per Minute). |          |
| 4                           | PWM    | PWM output signal for FAN speed control                                                     |          |
| <b>Connector Type</b>       |        |                                                                                             |          |
| B2W, 1x4-pin, 2.54 mm pitch |        |                                                                                             |          |

### 7.3. SATA (Serial ATA) Port 0 Connector (CN27)

The SATA connector supplies the data connection for the SATA hard disk and is SATA 3.0 compatible.

Figure 14: SATA Port 0 Connector CN27



Table 20: Pin Assignment CN27

| Pin                         | Signal        | Description                                   | Note |
|-----------------------------|---------------|-----------------------------------------------|------|
| 1                           | GND           | Ground                                        |      |
| 2                           | TX+           | Host transmitter differential signal pair (+) |      |
| 3                           | TX-           | Host transmitter differential signal pair (-) |      |
| 4                           | GND           | Ground                                        |      |
| 5                           | RX-           | Host receiver differential signal pair (-)    |      |
| 6                           | RX+           | Host receiver differential signal pair (+)    |      |
| 7                           | GND           | Ground                                        |      |
| <b>Connector Type</b>       |               |                                               |      |
| B2W, 1x7-pin, 1.27 mm pitch |               |                                               |      |
| <b>Mating Connector</b>     |               |                                               |      |
| Vendor                      | WINWIN        |                                               |      |
| Model No.                   | WATC-07DLPO2U |                                               |      |

## 7.4. SATA Power Output Wafer (CN9)

The 1x4-pin 2.0 mm pitch SATA power output wafer provides power to the SATA hard disk.

Figure 15: SATA Power Output Wafer CN9



Table 21: Pin Assignment CN9

| Pin                        | Signal        | Description                      | Note     |
|----------------------------|---------------|----------------------------------|----------|
| 1                          | +12V          | +12 V power supply for HDD / SSD | 1 A max. |
| 2                          | GND           | Ground                           |          |
| 3                          | GND           | Ground                           |          |
| 4                          | +5V           | +5 V power supply for HDD / SSD  | 1 A max. |
| <b>Connector Type</b>      |               |                                  |          |
| B2W, 1x4-pin, 2.0 mm pitch |               |                                  |          |
| <b>Mating Connector</b>    |               |                                  |          |
| Vendor                     | Pinrex        |                                  |          |
| Housing Model No.          | 721-75-04W009 |                                  |          |
| Terminal Model No.         | 721-70-T00009 |                                  |          |

## 7.5. USB Connectors (Internal) (CN19 & CN20)

The 10-pin 2.0 mm pitch USB port pin header CN19 & CN20 supports two USB 2.0 ports each.

Figure 16: USB 2.0 Port 5, 6 Pin Header CN19, Port 7, 8 Pin Header CN20

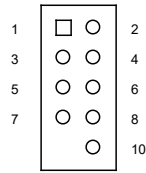


Table 22: Pin Assignment CN19, CN20

| Pin                        | Signal              | Description                                                     | Note     |
|----------------------------|---------------------|-----------------------------------------------------------------|----------|
| 1                          | +USBVCC*            | 5 V supply. SB5V is supplied during power down to allow wakeup. | 1 A max. |
| 2                          | +USBVCC*            | 5 V supply. SB5V is supplied during power down to allow wakeup. | 1 A max. |
| 3                          | USB_DA-             | USB 2.0 differential pair (-) for channel A                     |          |
| 4                          | USB_DB-             | USB 2.0 differential pair (-) for channel B                     |          |
| 5                          | USB_DA+             | USB 2.0 differential pair (+) for channel A                     |          |
| 6                          | USB_DB+             | USB 2.0 differential pair (+) for channel B                     |          |
| 7                          | GND                 | Ground                                                          |          |
| 8                          | GND                 | Ground                                                          |          |
| 9                          | KEY                 |                                                                 |          |
| 10                         | GND                 | Ground                                                          |          |
| <b>Connector Type</b>      |                     |                                                                 |          |
| B2W, 2x5-pin, 2.0 mm pitch |                     |                                                                 |          |
| <b>Mating Connector</b>    |                     |                                                                 |          |
| Vendor                     | Dupont              |                                                                 |          |
| Housing Model No.          | WL2004H-2*5P(DP2.0) |                                                                 |          |
| Terminal Model No.         | KB931-21T1A         |                                                                 |          |



\* The power source of +USBVCC for CN19 and CN20 can be selected by JP10.

## 7.6. Audio AMP Output Wafer (CN1 & CN5)

The Speaker audio-out interface is available through the 2-pin 2.0 mm pitch wafers CN1 for left channel and CN5 for right channel. These outputs are shared with the audio output (Line-out) signals of the audio pin header CN7.

Figure 17: Audio AMP Output Wafer CN1 (Left Channel), CN5 (Right Channel)

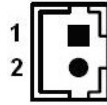


Table 23: Pin Assignment CN1, CN5

| Pin                        | Signal        | Description        | Note |
|----------------------------|---------------|--------------------|------|
| 1                          | Speaker+      | Speaker output (+) |      |
| 2                          | Speaker-      | Speaker output (-) |      |
| <b>Connector Type</b>      |               |                    |      |
| B2W, 1x2-pin, 2.0 mm pitch |               |                    |      |
| <b>Mating Connector</b>    |               |                    |      |
| Vendor                     | Pinrex        |                    |      |
| Housing Model No.          | 721-75-02W009 |                    |      |
| Terminal Model No.         | 721-70-T00009 |                    |      |

## 7.7. Audio Input / Output Header (CN7)

The audio input / output header provides audio output (Line-Out), audio input (Line-In) and microphone (Mic-In) signals through the 10-pin 1.25 mm pitch wafer CN7. The audio output signals are shared with those of the speaker connectors CN1 & CN5.

Figure 18: Audio Input / Output Header CN7

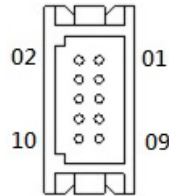


Table 24: Pin Assignment CN7

| Pin                         | Signal          | Description                           | Note |
|-----------------------------|-----------------|---------------------------------------|------|
| 1                           | MIC-In_L        | Microphone input left channel signal  |      |
| 2                           | MIC-In_R        | Microphone input right channel signal |      |
| 3                           | MIC-In_JD#      | Microphone jack detection             |      |
| 4                           | Line-In_JD#     | Audio input jack detection            |      |
| 5                           | Line-In_L       | Audio input left channel signal       |      |
| 6                           | Line-In_R       | Audio input right channel signal      |      |
| 7                           | Line-Out_L      | Audio output left channel signal      |      |
| 8                           | Line-Out_R      | Audio output right channel signal     |      |
| 9                           | Line-Out_JD#    | Audio output jack detection           |      |
| 10                          | GND             | Ground                                |      |
| <b>Connector Type</b>       |                 |                                       |      |
| B2W, 2x5-pin, 1.25 mm pitch |                 |                                       |      |
| <b>Mating Connector</b>     |                 |                                       |      |
| Vendor                      | HRS             |                                       |      |
| Housing Model No.           | DF13-10DS-1.25C |                                       |      |
| Terminal Model No.          | WL1255-T-T-S    |                                       |      |

## 7.8. Front Panel Header (FP1 & FP2)

The 8-pin 2.54 mm pitch front panel header FP1 supplies signals for the reset button, storage LED and system warning speaker.

The 10-pin 2.54 mm pitch front panel header FP2 supplies signals for the power button, power LED, and SM Bus.

Figure 19: Front Panel 1 Header FP1

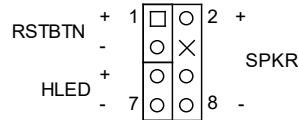


Table 25: Pin Assignment FP1

| Pin                         | Signal             | Description                                                                                       | Note |
|-----------------------------|--------------------|---------------------------------------------------------------------------------------------------|------|
| 1                           | Reset Button +     | System reset button (+)                                                                           |      |
| 2                           | Speaker +          | External system warning speaker (+)                                                               |      |
| 3                           | Reset Button -     | System reset button (-)                                                                           |      |
| 4                           | -                  | No connection                                                                                     |      |
| 5                           | HDD LED +          | HDD activity LED (+). The LED lights up or flashes when data is ready from or written to the HDD. |      |
| 6                           | Internal Speaker - | Internal system warning speaker (-)                                                               |      |
| 7                           | HDD LED -          | HDD activity LED (-).                                                                             |      |
| 8                           | Speaker -          | External system warning speaker (-)                                                               |      |
| <b>Connector Type</b>       |                    |                                                                                                   |      |
| B2W, 2x4-pin, 2.54 mm pitch |                    |                                                                                                   |      |
| <b>Mating Connector</b>     |                    |                                                                                                   |      |
| Vendor                      | Pinrex             |                                                                                                   |      |
| Housing Model No.           | 741-75-204B01      |                                                                                                   |      |
| Terminal Model No.          | 741-70-FT0001      |                                                                                                   |      |



Internal Buzzer is enabled when Pin6-8 is shorted.

Figure 20: Front Panel 2 Header FP2

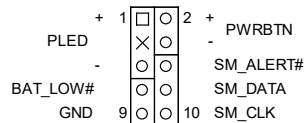


Table 26: Pin Assignment FP2

| Pin | Signal      | Description                                                    | Note |
|-----|-------------|----------------------------------------------------------------|------|
| 1   | Power LED + | System Power LED (+). The LED lights up when users turn on the |      |

| Pin                                                                                                       | Signal         | Description                                                                                                                                                                                                                                                 | Note |
|-----------------------------------------------------------------------------------------------------------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
|                                                                                                           |                | system power, and blinks when the system is in sleep mode.                                                                                                                                                                                                  |      |
| 2                                                                                                         | Power Button + | System power button (+). Pressing the power button turns the system on or puts the system in sleep or soft-off mode depending on the operating system settings. Pressing the power switch for more than four seconds while the system turns from ON to OFF. |      |
| 3                                                                                                         | -              | No connection                                                                                                                                                                                                                                               |      |
| 4                                                                                                         | Power Button - | System power button (-).                                                                                                                                                                                                                                    |      |
| 5                                                                                                         | Power LED -    | System Power LED (-).                                                                                                                                                                                                                                       |      |
| 6                                                                                                         | -              | No connection                                                                                                                                                                                                                                               |      |
| 7                                                                                                         | -              | No connection                                                                                                                                                                                                                                               |      |
| 8                                                                                                         | SMBus Data     | System management bus bidirectional data line                                                                                                                                                                                                               |      |
| 9                                                                                                         | GND            | Ground                                                                                                                                                                                                                                                      |      |
| 10                                                                                                        | SMBus Clock    | System management bus bidirectional clock line                                                                                                                                                                                                              |      |
| <b>Connector Type</b>                                                                                     |                |                                                                                                                                                                                                                                                             |      |
| B2W, 2x5-pin, 2.54 mm pitch                                                                               |                |                                                                                                                                                                                                                                                             |      |
| <b>Mating Connector</b>                                                                                   |                |                                                                                                                                                                                                                                                             |      |
| <b>Vendor</b> Pinrex<br><b>Housing Model No.</b> 741-75-205B01<br><b>Terminal Model No.</b> 741-70-FT0001 |                |                                                                                                                                                                                                                                                             |      |

## 7.9. Serial COM1 & COM2 Ports (CN24 & CN23)

The 10-pin 1.25 mm pitch serial COM wafer CN22 and CN23 provide RS232/422/485 connections.

Figure 21: Serial COM CN23, CN24

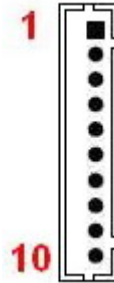


Table 27: Pin Assignment CN23, CN24

| Pin                          | RS232 Signal  | RS422 Signal | Half Duplex RS485 Signal | Full Duplex RS485 Signal | Note        |
|------------------------------|---------------|--------------|--------------------------|--------------------------|-------------|
| 1                            | DCD           | TX-          | DATA-                    | TX-                      |             |
| 2                            | DSR           | -            | -                        | -                        |             |
| 3                            | RXD           | TX+          | DATA+                    | TX+                      |             |
| 4                            | RTS           | -            | -                        | -                        |             |
| 5                            | TXD           | RX+          | -                        | RX+                      |             |
| 6                            | CTS           | -            | -                        | -                        |             |
| 7                            | DTR           | RX-          | -                        | RX-                      |             |
| 8                            | RI            | -            | -                        | -                        |             |
| 9                            | GND           | GND          | GND                      | GND                      |             |
| 10                           | +5V           | +5V          | +5V                      | +5V                      | 500 mA max. |
| <b>Connector Type</b>        |               |              |                          |                          |             |
| B2W, 1x10-pin, 1.25 mm pitch |               |              |                          |                          |             |
| <b>Mating Connector</b>      |               |              |                          |                          |             |
| Vendor                       | Pinrex        |              |                          |                          |             |
| Housing Model No.            | 712-75-10W001 |              |                          |                          |             |
| Terminal Model No.           | 712-70-T00001 |              |                          |                          |             |

Table 28: Signal Description

| Signal | Description                                                                                                                                                                                       |
|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TXD    | Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12 V) on hardware reset when the transmitter is empty or when loop mode operation is initiated. |
| RXD    | Received Data, receives data from the communications link.                                                                                                                                        |
| DTR    | Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to establish communication link.                                                                                 |
| DSR    | Data Set Ready, indicates that the modem etc. is ready to establish a communications link.                                                                                                        |
| RTS    | Request To Send, indicates to the modem etc. that the on-board UART is ready to                                                                                                                   |

| Signal | Description                                                                                     |
|--------|-------------------------------------------------------------------------------------------------|
|        | exchange data.                                                                                  |
| CTS    | Clear To Send, indicates that the modem or data set is ready to exchange data.                  |
| DCD    | Data Carrier Detect, indicates that the modem or data set has detected the data carrier.        |
| RI     | Ring Indicator, indicates that the modem has received a ringing signal from the telephone line. |
| TX+/-  | Transmitted Data differential pair sends data to the communications link.                       |
| RX+/-  | Received Data differential pair receives data from the communications link.                     |
| GND    | Power Supply GND signal                                                                         |

## 7.10. LVDS Connector (CN25)

The 30-pole 1.0 mm pitch JAE connector provides 24-bit, 2-channel LVDS panel connection.

Figure 22: LVDS Connector CN25

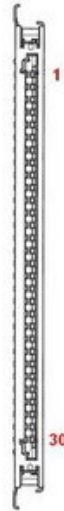


Table 29: Pin Assignment CN25

| Pin | Signal      | Description                                 | Note |
|-----|-------------|---------------------------------------------|------|
| 1   | LVDSA_TX0-  | LVDS Channel A Data 0 differential pair (-) |      |
| 2   | LVDSA_TX0+  | LVDS Channel A Data 0 differential pair (+) |      |
| 3   | LVDSA_TX1-  | LVDS Channel A Data 1 differential pair (-) |      |
| 4   | LVDSA_TX1+  | LVDS Channel A Data 1 differential pair (+) |      |
| 5   | LVDSA_TX2-  | LVDS Channel A Data 2 differential pair (-) |      |
| 6   | LVDSA_TX2+  | LVDS Channel A Data 2 differential pair (+) |      |
| 7   | GND         | Ground                                      |      |
| 8   | LVDSA_BCLK- | LVDS Channel A clock differential pair (-)  |      |
| 9   | LVDSA_BCLK+ | LVDS Channel A clock differential pair (+)  |      |
| 10  | LVDSA_TX3-  | LVDS Channel A Data 3 differential pair (-) |      |
| 11  | LVDSA_TX3+  | LVDS Channel A Data 3 differential pair (+) |      |
| 12  | LVDSB_TX0-  | LVDS Channel B Data 0 differential pair (-) |      |
| 13  | LVDSB_TX0+  | LVDS Channel B Data 0 differential pair (+) |      |
| 14  | GND         | Ground                                      |      |
| 15  | LVDSB_TX1-  | LVDS Channel B Data 1 differential pair (-) |      |
| 16  | LVDSB_TX1+  | LVDS Channel B Data 1 differential pair (+) |      |
| 17  | GND         | Ground                                      |      |
| 18  | LVDSB_TX2-  | LVDS Channel B Data 2 differential pair (-) |      |
| 19  | LVDSB_TX2+  | LVDS Channel B Data 2 differential pair (+) |      |
| 20  | LVDSB_BCLK- | LVDS Channel B clock differential pair (-)  |      |
| 21  | LVDSB_BCLK+ | LVDS Channel B clock differential pair (+)  |      |

| Pin                         | Signal                  | Description                                 | Note        |
|-----------------------------|-------------------------|---------------------------------------------|-------------|
| 22                          | LVDSB_TX3-              | LVDS Channel B Data 3 differential pair (-) |             |
| 23                          | LVDSB_TX3+              | LVDS Channel B Data 3 differential pair (+) |             |
| 24                          | GND                     | Ground                                      |             |
| 25                          | DDC_DATA                | DDC channel Data                            |             |
| 26                          | VDDEN                   | Output Display Enable                       |             |
| 27                          | DDC_CLK                 | DDC Channel Clock                           |             |
| 28                          | +VPNL *                 | +3.3 V / +5 V panel power supply            | 500 mA max. |
| 29                          | +VPNL *                 | +3.3 V / +5 V panel power supply            | 500 mA max. |
| 30                          | +VPNL *                 | +3.3 V / +5 V panel power supply            | 500 mA max. |
| <b>Connector Type</b>       |                         |                                             |             |
| B2W, 1x30-pin, 1.0 mm pitch |                         |                                             |             |
| <b>Mating Connector</b>     |                         |                                             |             |
| Vendor                      | JAE                     |                                             |             |
| Housing Model No.           | WL1058HL-30P (FI-X30HL) |                                             |             |
| Terminal Model No.          | WL1058-G-P              |                                             |             |




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\* Panel Power can be selected by JP3.

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## 7.11. LVDS Backlight Power Wafer (CN2)

The 7-pin 1.25 mm pitch wafer CN2 provides power supply for flat panel and its backlight inverter.

Figure 23: LVDS Backlight Power Wafer CN2

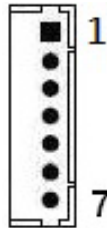


Table 30: Pin Assignment CN2

| Pin                         | Signal             | Description                                              | Note        |
|-----------------------------|--------------------|----------------------------------------------------------|-------------|
| 1                           | BL_EN***           | Backlight Enable signal                                  |             |
| 2                           | GND                | Ground                                                   |             |
| 3                           | +VBKLT**           | +5 V / +12 V backlight power supply                      | 750 mA max. |
| 4                           | +VBKLT**           | +5 V / +12 V backlight power supply                      | 750 mA max. |
| 5                           | GND                | Ground                                                   |             |
| 6                           | BL_ADJ_VOL*        | Backlight Adjustment Voltage signal                      |             |
| 7                           | BL_ADJ_PWM*        | Backlight Adjustment PWM (Pulse Width Modulation) signal |             |
| <b>Connector Type</b>       |                    |                                                          |             |
| B2W, 1x7-pin, 1.25 mm pitch |                    |                                                          |             |
| <b>Mating Connector</b>     |                    |                                                          |             |
| Vendor                      | Pinrex             |                                                          |             |
| Housing Model No.           | WL1025H-7P (51021) |                                                          |             |
| Terminal Model No.          | KB915-10T          |                                                          |             |



\* BL\_ADJ can be selected by JP1.



\*\* Backlight Power can be selected by JP3.



\*\*\* BL\_EN can be selected by JP4.

## 7.12. Digital Input / Output Header (CN3)

The 10-pin 1.25 mm pitch header CN3 supports 8-bit digital input / output signals to provide powering-on function of the connected devices.

Figure 24: Digital Input / Output Header CN3

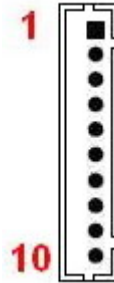


Table 31: Pin Assignment CN3

| Pin                          | Signal        | Description                      | Note        |
|------------------------------|---------------|----------------------------------|-------------|
| 1                            | +5V           | +5 V power supply                | 500 mA max. |
| 2                            | DIO_0         | Digital input / output channel 0 |             |
| 3                            | DIO_1         | Digital input / output channel 1 |             |
| 4                            | DIO_2         | Digital input / output channel 2 |             |
| 5                            | DIO_3         | Digital input / output channel 3 |             |
| 6                            | DIO_4         | Digital input / output channel 4 |             |
| 7                            | DIO_5         | Digital input / output channel 5 |             |
| 8                            | DIO_6         | Digital input / output channel 6 |             |
| 9                            | DIO_7         | Digital input / output channel 7 |             |
| 10                           | GND           | Ground                           |             |
| <b>Connector Type</b>        |               |                                  |             |
| B2W, 1x10-pin, 1.25 mm pitch |               |                                  |             |
| <b>Mating Connector</b>      |               |                                  |             |
| Vendor                       | Pinrex        |                                  |             |
| Housing Model No.            | 712-75-10W001 |                                  |             |
| Terminal Model No.           | 712-70-T00001 |                                  |             |

### 7.13. M.2 Key B 2242 / 3042 / 2280 Slot (M2B1)

The 3.5"-SBC-TGL supports M.2 modules in format 2242 / 3042 / 2280 with Key B. The M.2 specification supports PCIe x1 / SATA 3.0 and USB 2.0 signals as well as UIM signals connected to Micro SIM card holder CN6. The slot can be used to integrate WWAN communication to the mainboard.

#### NOTICE

The module will protrude over the edge of the baseboard in case of installing a M.2 3042 module. Designers shall prescribe the chassis size with regard for maximum assembly dimensions.

Figure 25: M.2 Key B 3042 / 2280 Slot M2B1

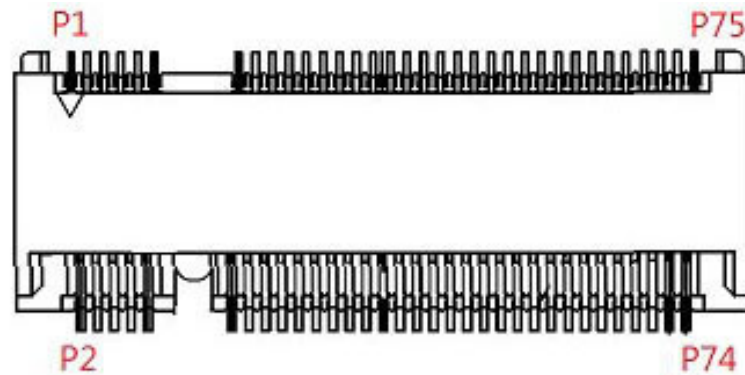


Table 32: Pin Assignment M2B1

| Pin | Signal   | Description                        | Note |
|-----|----------|------------------------------------|------|
| 1   | -        |                                    |      |
| 2   | +3.3V    | 3.3 V power supply                 |      |
| 3   | GND      | Ground                             |      |
| 4   | +3.3V    | 3.3 V power supply                 |      |
| 5   | GND      | Ground                             |      |
| 6   | PWROFF#  | M.2 module power enable            |      |
| 7   | USB_D+   | USB 2.0 data differential pair (+) |      |
| 8   | DISABLE# | Wireless disable                   |      |
| 9   | USB_D-   | USB 2.0 data differential pair (-) |      |
| 10  | LED#     | Device active signal               |      |
| 11  | GND      | Ground                             |      |
| 12  | KEY      |                                    |      |
| 13  | KEY      |                                    |      |
| 14  | KEY      |                                    |      |
| 15  | KEY      |                                    |      |
| 16  | KEY      |                                    |      |
| 17  | KEY      |                                    |      |
| 18  | KEY      |                                    |      |
| 19  | KEY      |                                    |      |
| 20  | -        |                                    |      |

| Pin | Signal          | Description                                               | Note |
|-----|-----------------|-----------------------------------------------------------|------|
| 21  | -               |                                                           |      |
| 22  | -               |                                                           |      |
| 23  | -               |                                                           |      |
| 24  | -               |                                                           |      |
| 25  | -               |                                                           |      |
| 26  | -               |                                                           |      |
| 27  | GND             | Ground                                                    |      |
| 28  | -               |                                                           |      |
| 29  | -               |                                                           |      |
| 30  | UIM_RESET*      | SIM card reset                                            |      |
| 31  | -               |                                                           |      |
| 32  | UIM_CLK*        | SIM card clock                                            |      |
| 33  | GND             | Ground                                                    |      |
| 34  | UIM_DATA*       | SIM card data                                             |      |
| 35  | -               |                                                           |      |
| 36  | UIM_PWR*        | SIM card power                                            |      |
| 37  | -               |                                                           |      |
| 38  | -               |                                                           |      |
| 39  | GND             | Ground                                                    |      |
| 40  | -               |                                                           |      |
| 41  | PERn0 / SATA_B+ | PCIe Lane 0 receiver pair (-) / SATA transmitter pair (+) |      |
| 42  | -               |                                                           |      |
| 43  | PERp0 / SATA_B- | PCIe Lane 0 receiver pair (+) / SATA transmitter pair (-) |      |
| 44  | -               |                                                           |      |
| 45  | GND             | Ground                                                    |      |
| 46  | -               |                                                           |      |
| 47  | PETn0 / SATA_A- | PCIe Lane 0 transmitter pair (-) / SATA receiver pair (-) |      |
| 48  | -               |                                                           |      |
| 49  | PETp0 / SATA_A+ | PCIe Lane 0 transmitter pair (+) / SATA receiver pair (+) |      |
| 50  | PERST#          | PCIe reset                                                |      |
| 51  | GND             | Ground                                                    |      |
| 52  | CLKREQ#         | Reference clock request signal                            |      |
| 53  | REFCLKn         | PCIe reference clock pair (-)                             |      |
| 54  | WAKE#           | PCIe wake                                                 |      |
| 55  | REFCLKp         | PCIe reference clock pair (+)                             |      |
| 56  | -               |                                                           |      |
| 57  | GND             | Ground                                                    |      |
| 58  | -               |                                                           |      |
| 59  | -               |                                                           |      |
| 60  | -               |                                                           |      |
| 61  | -               |                                                           |      |
| 62  | -               |                                                           |      |

| Pin | Signal     | Description                   | Note |
|-----|------------|-------------------------------|------|
| 63  | -          |                               |      |
| 64  | -          |                               |      |
| 65  | -          |                               |      |
| 66  | SIM_DETECT | SIM card detect               |      |
| 67  | -          |                               |      |
| 68  | SUSCLK     | 32.768 kHz clock supply input |      |
| 69  | -          |                               |      |
| 70  | +3.3V      | 3.3 V power supply            |      |
| 71  | GND        | Ground                        |      |
| 72  | +3.3V      | 3.3 V power supply            |      |
| 73  | GND        | Ground                        |      |
| 74  | +3.3V      | 3.3 V power supply            |      |
| 75  | -          |                               |      |




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\* These pins are connected to CN6 Micro SIM card holder directly.

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## 7.14. M.2 Key E 2230 Slot (M2E1)

The 3.5"-SBC-TGL supports M.2 modules in format 2230 with Key E. The M.2 specification supports PCIe x1, USB 2.0, UART, PCM and / or CNVi signals. The slot can be used to integrate WLAN (Wi-Fi or CNVi Wi-Fi) and / or Bluetooth communication to the mainboard.

Figure 26: M.2 Key E 2230 Slot M2E1

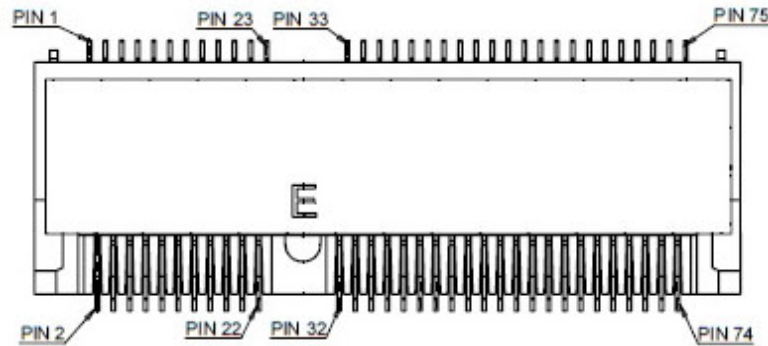


Table 33: Pin Assignment M2E1

| Pin | Key E*     |                             | CNVi*    |                          | Note |
|-----|------------|-----------------------------|----------|--------------------------|------|
|     | Signal     | Description                 | Signal   | Description              |      |
| 1   | GND        | Ground                      | GND      | Ground                   |      |
| 2   | +3.3V      | 3.3 V power supply          | +3.3V    | 3.3 V power supply       |      |
| 3   | USB_D+     | USB 2.0 data diff. pair (+) | -        |                          |      |
| 4   | +3.3V      | 3.3 V power supply          | +3.3V    | 3.3 V power supply       |      |
| 5   | USB_D-     | USB 2.0 data diff. pair (-) | -        |                          |      |
| 6   | LED1#      | Device active signal 1      | LED1#    | Device active signal 1   |      |
| 7   | GND        | Ground                      | GND      | Ground                   |      |
| 8   | PCM_CLK    | PCM synchronous data clock  | -        |                          |      |
| 9   | -          |                             | WGR_D1N  | CNVio bus Rx Lane 1 (-)  |      |
| 10  | PCM_SYNC   | PCM synchronous data sync   | LCP_RSTN | RF companion (CRF) reset |      |
| 11  | -          |                             | WGR_D1P  | CNVio bus Rx Lane 1 (+)  |      |
| 12  | PCM_IN     | PCM synchronous data input  | -        |                          |      |
| 13  | GND        | Ground                      | GND      | Ground                   |      |
| 14  | PCM_OUT    | PCM synchronous data output | CLKREQ0  | Clock request            |      |
| 15  | -          |                             | WGR_D0N  | CNVio bus Rx Lane 0 (-)  |      |
| 16  | LED2#      | Device active signal 2      | LED2#    | Device active signal 2   |      |
| 17  | -          |                             | WGR_D0P  | CNVio bus Rx Lane 0 (+)  |      |
| 18  | GND        | Ground                      | GND      | Ground                   |      |
| 19  | GND        | Ground                      | GND      | Ground                   |      |
| 20  | UART_WAKE# | UART wake-up                | -        |                          |      |
| 21  | -          |                             | WGR_CLKN | CNVio bus Rx clock (-)   |      |
| 22  | UART_RX    | UART data input             | BRI_RSP  | BRI bus Rx               |      |
| 23  | -          |                             | WGR_CLKP | CNVio bus Rx clock (+)   |      |

| Pin | Key E*      |                                | CNVi*       |                               | Note |
|-----|-------------|--------------------------------|-------------|-------------------------------|------|
|     | Signal      | Description                    | Signal      | Description                   |      |
| 24  | Key         |                                | Key         |                               |      |
| 25  | Key         |                                | Key         |                               |      |
| 26  | Key         |                                | Key         |                               |      |
| 27  | Key         |                                | Key         |                               |      |
| 28  | Key         |                                | Key         |                               |      |
| 29  | Key         |                                | Key         |                               |      |
| 30  | Key         |                                | Key         |                               |      |
| 31  | Key         |                                | Key         |                               |      |
| 32  | UART_TX     | UART data output               | RGI_DT      | RGI bus Tx                    |      |
| 33  | GND         | Ground                         | GND         | Ground                        |      |
| 34  | UART_CTS    | UART clear to send             | RGI_RSP     | RGI bus Rx                    |      |
| 35  | PET0+       | PCIe Lane 0 Tx pair (+)        | -           |                               |      |
| 36  | UART_RTS    | UART request to send           | BRI_DT      | BRI bus Tx                    |      |
| 37  | PET0-       | PCIe Lane 0 Tx pair (-)        | -           |                               |      |
| 38  | Clink_RST   | Wi-Fi CLINK host bus reset     | -           |                               |      |
| 39  | GND         | Ground                         | GND         | Ground                        |      |
| 40  | Clink_DATA  | Wi-Fi CLINK host bus data      | -           |                               |      |
| 41  | PER0+       | PCIe Lane 0 Rx pair (+)        | -           |                               |      |
| 42  | Clink_CLK   | Wi-Fi CLINK host bus clock     | -           |                               |      |
| 43  | PER0-       | PCIe Lane 0 Rx pair (-)        | -           |                               |      |
| 44  | -           |                                | -           |                               |      |
| 45  | GND         | Ground                         | GND         | Ground                        |      |
| 46  | -           |                                | -           |                               |      |
| 47  | REFCLK0+    | PCIe reference clock pair (+)  | -           |                               |      |
| 48  | -           |                                | -           |                               |      |
| 49  | REFCLK0-    | PCIe reference clock pair (-)  | -           |                               |      |
| 50  | SUSCLK      | 32.768 kHz clock supply input  | SUSCLK      | 32.768 kHz clock supply input |      |
| 51  | GND         | Ground                         | GND         | Ground                        |      |
| 52  | PERST0#     | PCIe reset                     | -           |                               |      |
| 53  | CLKREQ0#    | Reference clock request signal | -           |                               |      |
| 54  | W_DISABLE2# | Wireless disable 2             | W_DISABLE2# | Wireless disable 2            |      |
| 55  | PEWAKE0#    | PCIe wake                      | -           |                               |      |
| 56  | W_DISABLE1# | Wireless disable 1             | W_DISABLE1# | Wireless disable 1            |      |
| 57  | GND         | Ground                         | GND         | Ground                        |      |
| 58  | -           |                                | -           |                               |      |
| 59  | -           |                                | WT_D1N      | CNVio bus Tx Lane 1 (-)       |      |
| 60  | -           |                                | -           |                               |      |
| 61  | -           |                                | WT_D1P      | CNVio bus Tx Lane 1 (+)       |      |
| 62  | -           |                                | -           |                               |      |
| 63  | GND         | Ground                         | GND         | Ground                        |      |
| 64  | -           |                                | REFCLK0     | Reference clock               |      |

| Pin | Key E* |                    | CNVi*   |                         | Note |
|-----|--------|--------------------|---------|-------------------------|------|
|     | Signal | Description        | Signal  | Description             |      |
| 65  | -      |                    | WT_D0N  | CNVio bus Tx Lane 0 (-) |      |
| 66  | -      |                    | -       |                         |      |
| 67  | -      |                    | WT_D0P  | CNVio bus Tx Lane 0 (+) |      |
| 68  | -      |                    | -       |                         |      |
| 69  | GND    | Ground             | GND     | Ground                  |      |
| 70  | -      |                    | -       |                         |      |
| 71  | -      |                    | WT_CLKN | CNVio bus Tx clock (-)  |      |
| 72  | +3.3V  | 3.3 V power supply | +3.3V   | 3.3 V power supply      |      |
| 73  | -      |                    | WT_CLKP | CNVio bus Tx clock (+)  |      |
| 74  | +3.3V  | 3.3 V power supply | +3.3V   | 3.3 V power supply      |      |
| 75  | GND    | Ground             | GND     | Ground                  |      |




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\* The board will auto-detect the module type and re-configure itself to an appropriate mode.

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## 7.15. M.2 Key M 2280 Slot (M2M1)

The 3.5"-SBC-TGL supports M.2 modules in format 2280 with Key M. The M.2 specification supports PCIe x4 signal. The slot can be used to integrate an M.2 PCIe x4 SSD (NVMe) to the mainboard.



NVMe controllers are using up to 10 W (type dependent). A thermal design to compensate the heat dissipation needs to be considered.

Figure 27: M.2 Key M 2280 Slot M2M1

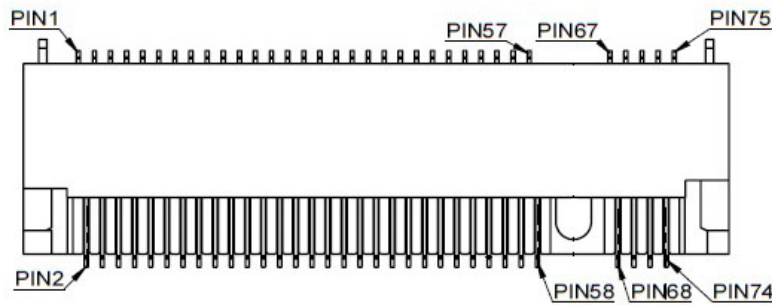


Table 34: Pin Assignment M2M1

| Pin | Signal             | Description                                            | Note |
|-----|--------------------|--------------------------------------------------------|------|
| 1   | GND                | Ground                                                 |      |
| 2   | +3.3V              | 3.3 V power supply                                     |      |
| 3   | GND                | Ground                                                 |      |
| 4   | +3.3V              | 3.3 V power supply                                     |      |
| 5   | PERn3              | PCIe Lane 3 receiver pair (-)                          |      |
| 6   | -                  |                                                        |      |
| 7   | PERp3              | PCIe Lane 3 receiver pair (+)                          |      |
| 8   | -                  | -                                                      |      |
| 9   | GND                | Ground                                                 |      |
| 10  | DAS / DSS# / LED1# | Device active signal / disable staggered spin-up / LED |      |
| 11  | PETn3              | PCIe Lane 3 transmitter pair (-)                       |      |
| 12  | +3.3V              | 3.3 V power supply                                     |      |
| 13  | PETp3              | PCIe Lane 3 transmitter pair (+)                       |      |
| 14  | +3.3V              | 3.3 V power supply                                     |      |
| 15  | GND                | Ground                                                 |      |
| 16  | +3.3V              | 3.3 V power supply                                     |      |
| 17  | PERn2              | PCIe Lane 2 receiver pair (-)                          |      |
| 18  | +3.3V              | 3.3 V power supply                                     |      |
| 19  | PERp2              | PCIe Lane 2 receiver pair (-)                          |      |
| 20  | -                  |                                                        |      |
| 21  | GND                | Ground                                                 |      |
| 22  | -                  |                                                        |      |

| Pin | Signal  | Description                      | Note |
|-----|---------|----------------------------------|------|
| 23  | PETn2   | PCIe Lane 2 transmitter pair (-) |      |
| 24  | -       |                                  |      |
| 25  | PETp2   | PCIe Lane 2 transmitter pair (+) |      |
| 26  | -       |                                  |      |
| 27  | GND     | Ground                           |      |
| 28  | -       |                                  |      |
| 29  | PERn1   | PCIe Lane 1 receiver pair (-)    |      |
| 30  | -       |                                  |      |
| 31  | PERp1   | PCIe Lane 1 receiver pair (+)    |      |
| 32  | -       |                                  |      |
| 33  | GND     | Ground                           |      |
| 34  | -       |                                  |      |
| 35  | PETn1   | PCIe Lane 1 transmitter pair (-) |      |
| 36  | -       |                                  |      |
| 37  | PETp1   | PCIe Lane 1 transmitter pair (+) |      |
| 38  | DEVSLP  | Device sleep                     |      |
| 39  | GND     | Ground                           |      |
| 40  | -       |                                  |      |
| 41  | PERn0   | PCIe Lane 0 receiver pair (-)    |      |
| 42  | -       |                                  |      |
| 43  | PERp0   | PCIe Lane 0 receiver pair (+)    |      |
| 44  | -       |                                  |      |
| 45  | GND     | Ground                           |      |
| 46  | -       |                                  |      |
| 47  | PETn0   | PCIe Lane 0 transmitter pair (-) |      |
| 48  | -       |                                  |      |
| 49  | PETp0   | PCIe Lane 0 transmitter pair (+) |      |
| 50  | PERST#  | PCIe reset                       |      |
| 51  | GND     | Ground                           |      |
| 52  | CLKREQ# | Reference clock request signal   |      |
| 53  | REFCLKn | PCIe reference clock pair (-)    |      |
| 54  | PEWAKE# | PCIe wake                        |      |
| 55  | REFCLKp | PCIe reference clock pair (+)    |      |
| 56  | -       |                                  |      |
| 57  | GND     | Ground                           |      |
| 58  | -       |                                  |      |
| 59  | Key     |                                  |      |
| 60  | Key     |                                  |      |
| 61  | Key     |                                  |      |
| 62  | Key     |                                  |      |
| 63  | Key     |                                  |      |
| 64  | Key     |                                  |      |

| Pin | Signal | Description                   | Note |
|-----|--------|-------------------------------|------|
| 65  | Key    |                               |      |
| 66  | Key    |                               |      |
| 67  | -      |                               |      |
| 68  | SUSCLK | 32.768 kHz clock supply input |      |
| 69  | PEDET  | PCIe detect                   |      |
| 70  | +3.3V  | 3.3 V power supply            |      |
| 71  | GND    | Ground                        |      |
| 72  | +3.3V  | 3.3 V power supply            |      |
| 73  | GND    | Ground                        |      |
| 74  | +3.3V  | 3.3 V power supply            |      |
| 75  | GND    | Ground                        |      |

## 7.16. Micro SIM Card Holder for M.2 Key B (CN6)

The Micro SIM card holder CN6 is intended to accommodate a Micro SIM card and connected to UIM signals on the M.2 Key B slot M2B1.

Figure 28: Micro SIM Card Holder CN6

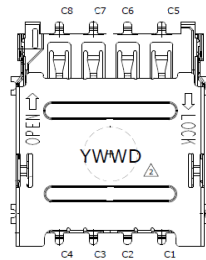


Table 35: Pin Assignment CN6

| Pin | Signal | Description                     | Note |
|-----|--------|---------------------------------|------|
| C1  | VCC    | Power +3.3 V                    |      |
| C2  | RST    | Reset signal                    |      |
| C3  | CLK    | Clock signal                    |      |
| C4  | NC     | Not connected                   |      |
| C5  | GND    | Ground                          |      |
| C6  | VPP    | Programming voltage input       |      |
| C7  | IO     | Input or Output for serial data |      |
| C8  | NC     | Not connected                   |      |

## 7.17. M.2 Key B / M.2 Key E / M.2 Key M Activity Indicator Header (CN8, CN11 & CN14)

The header CN8 is intended to connect M.2 Key B activity LED cable.

The header CN11 is intended to connect M.2 Key E activity LED cable.

The header CN14 is intended to connect M.2 Key M activity LED cable.

Figure 29: M.2 Key B / M.2 Key M Activity Indicator Header CN8, CN14

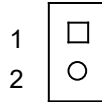


Table 36: Pin Assignment CN8, CN14

| Pin                        | Signal | Description                            | Note |
|----------------------------|--------|----------------------------------------|------|
| 1                          | LED+   | M.2 Key B / M.2 Key M activity LED (+) |      |
| 2                          | LED-   | M.2 Key B / M.2 Key M activity LED (-) |      |
| <b>Connector Type</b>      |        |                                        |      |
| B2W, 1x2-pin, 2.0 mm pitch |        |                                        |      |

Figure 30: M.2 Key E Activity Indicator Header CN11

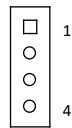


Table 37: Pin Assignment CN11

| Pin                        | Signal     | Description    | Note |
|----------------------------|------------|----------------|------|
| 1                          | WLAN_LED1+ | WLAN LED (+)   |      |
| 2                          | WLAN_LED1- | WLAN LED (-)   |      |
| 3                          | BR_LED2+   | Breath LED (+) |      |
| 4                          | BR_LED2-   | Breath LED (-) |      |
| <b>Connector Type</b>      |            |                |      |
| B2W, 1x4-pin, 2.0 mm pitch |            |                |      |

## 7.18. Extended B2B Connector (CN28)

The extended board-to-board connector provides connection to a daughter board for additional I/O port and / or feature expansion. The specification of the B2B connector supports DDI (eDP / DP), PCIe x2, PCIe x1, SM bus, I2C, UART and GSPI signals.

Figure 31: Extended B2B Connector CN28

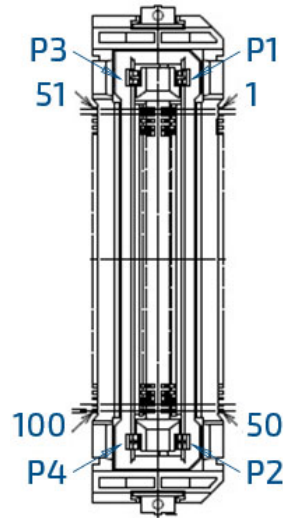


Table 38: Pin Assignment CN28

| Pin | Signal       | Description                            | Note        |
|-----|--------------|----------------------------------------|-------------|
| 1   | +3.3VSB_OUT  | 3.3 V standby power output             | 400 mA max. |
| 2   | +3.3VSB_OUT  | 3.3 V standby power output             | 400 mA max. |
| 3   | +3.3VSB_OUT  | 3.3 V standby power output             | 400 mA max. |
| 4   | +3.3VSB_OUT  | 3.3 V standby power output             | 400 mA max. |
| 5   | +3.3VSB_OUT  | 3.3 V standby power output             | 400 mA max. |
| 6   | GND          | Ground                                 |             |
| 7   | eDP_DP0_TX0+ | eDP / DP 0 Lane 0 transmitter pair (+) |             |
| 8   | eDP_DP0_TX0- | eDP / DP 0 Lane 0 transmitter pair (-) |             |
| 9   | GND          | Ground                                 |             |
| 10  | eDP_DP0_TX1+ | eDP / DP 0 Lane 1 transmitter pair (+) |             |
| 11  | eDP_DP0_TX1- | eDP / DP 0 Lane 1 transmitter pair (-) |             |
| 12  | GND          | Ground                                 |             |
| 13  | eDP_DP0_TX2+ | eDP / DP 0 Lane 2 transmitter pair (+) |             |
| 14  | eDP_DP0_TX2- | eDP / DP 0 Lane 2 transmitter pair (-) |             |
| 15  | GND          | Ground                                 |             |
| 16  | eDP_DP0_TX3+ | eDP / DP 0 Lane 3 transmitter pair (+) |             |
| 17  | eDP_DP0_TX3- | eDP / DP 0 Lane 3 transmitter pair (-) |             |
| 18  | GND          | Ground                                 |             |
| 19  | eDP_DP0_AUX+ | eDP / DP 0 Auxiliary channel pair (+)  |             |
| 20  | eDP_DP0_AUX- | eDP / DP 0 Auxiliary channel pair (-)  |             |

| Pin | Signal         | Description                                       | Note |
|-----|----------------|---------------------------------------------------|------|
| 21  | GND            | Ground                                            |      |
| 22  | PCIE0_CLK_REF+ | PCIe Lane 0 clock reference pair (+)              |      |
| 23  | PCIE0_CLK_REF- | PCIe Lane 0 clock reference pair (-)              |      |
| 24  | GND            | Ground                                            |      |
| 25  | PCIE0_TX+      | PCIe Lane 0 transmitter pair (+)                  |      |
| 26  | PCIE0_TX-      | PCIe Lane 0 transmitter pair (-)                  |      |
| 27  | GND            | Ground                                            |      |
| 28  | PCIE0_RX+      | PCIe Lane 0 receiver pair (+)                     |      |
| 29  | PCIE0_RX-      | PCIe Lane 0 receiver pair (-)                     |      |
| 30  | GND            | Ground                                            |      |
| 31  | PCIE2_TX+      | PCIe Lane 2 receiver pair (+)                     |      |
| 32  | PCIE2_TX-      | PCIe Lane 2 receiver pair (-)                     |      |
| 33  | GND            | Ground                                            |      |
| 34  | PCIE2_RX+      | PCIe Lane 2 receiver pair (+)                     |      |
| 35  | PCIE2_RX-      | PCIe Lane 2 receiver pair (-)                     |      |
| 36  | GND            | Ground                                            |      |
| 37  | NC             | Not connected                                     |      |
| 38  | NC             | Not connected                                     |      |
| 39  | GND            | Ground                                            |      |
| 40  | UART_TXD       | UART transmitted data                             |      |
| 41  | UART_RXD       | UART received data                                |      |
| 42  | UART_CTS#      | UART clear to send                                |      |
| 43  | UART_RTS#      | UART request to send                              |      |
| 44  | GND            | Ground                                            |      |
| 45  | eDP_PWM        | eDP backlight PWM (Pulse Width Modulation) signal |      |
| 46  | eDP_VDDEN      | eDP panel power enable signal                     |      |
| 47  | eDP_BKLTEN     | eDP backlight enable signal                       |      |
| 48  | eDP_D00_HPD    | eDP / DP 0 hot plug detect                        |      |
| 49  | eDP_DP0_EN#    | eDP / DP 0 enable                                 |      |
| 50  | NC             | Not connected                                     |      |
| 51  | GSPI_CLK       | General SPI clock                                 |      |
| 52  | GSPI_MOSI      | General SPI master output / slave input           |      |
| 53  | GSPI_MISO      | General SPI master input / slave output           |      |
| 54  | GSPI_CS0#      | General SPI chip select bit 0                     |      |
| 55  | GSPI_CS1#      | General SPI chip select bit 1                     |      |
| 56  | GND            | Ground                                            |      |
| 57  | DP1_TX0+       | DP 1 Lane 0 transmitter pair (+)                  |      |
| 58  | DP1_TX0-       | DP 1 Lane 0 transmitter pair (-)                  |      |
| 59  | GND            | Ground                                            |      |
| 60  | DP1_TX1+       | DP 1 Lane 1 transmitter pair (+)                  |      |
| 61  | DP1_TX1-       | DP 1 Lane 1 transmitter pair (-)                  |      |
| 62  | GND            | Ground                                            |      |

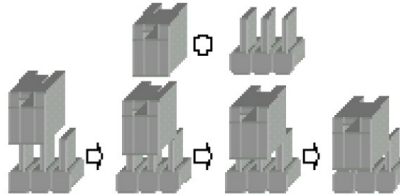
| Pin | Signal             | Description                          | Note     |
|-----|--------------------|--------------------------------------|----------|
| 63  | DP1_TX2+           | DP 1 Lane 2 transmitter pair (+)     |          |
| 64  | DP1_TX2-           | DP 1 Lane 2 transmitter pair (-)     |          |
| 65  | GND                | Ground                               |          |
| 66  | DP1_TX3+           | DP 1 Lane 3 transmitter pair (+)     |          |
| 67  | DP1_TX3-           | DP 1 Lane 3 transmitter pair (-)     |          |
| 68  | GND                | Ground                               |          |
| 69  | DP1_AUX+           | DP 1 Auxiliary channel pair (+)      |          |
| 70  | DP1_AUX-           | DP 1 Auxiliary channel pair (-)      |          |
| 71  | GND                | Ground                               |          |
| 72  | PCIE1_CLK_REF+     | PCle Lane 1 clock reference pair (+) |          |
| 73  | PCIE1_CLK_REF-     | PCle Lane 1 clock reference pair (-) |          |
| 74  | GND                | Ground                               |          |
| 75  | PCIE1_TX+          | PCle Lane 1 transmitter pair (+)     |          |
| 76  | PCIE1_TX-          | PCle Lane 1 transmitter pair (-)     |          |
| 77  | GND                | Ground                               |          |
| 78  | PCIE1_RX+          | PCle Lane 1 receiver pair (+)        |          |
| 79  | PCIE1_RX-          | PCle Lane 1 receiver pair (-)        |          |
| 80  | GND                | Ground                               |          |
| 81  | NC                 | Not connected                        |          |
| 82  | NC                 | Not connected                        |          |
| 83  | GND                | Ground                               |          |
| 84  | NC                 | Not connected                        |          |
| 85  | NC                 | Not connected                        |          |
| 86  | GND                | Ground                               |          |
| 87  | NC                 | Not connected                        |          |
| 88  | NC                 | Not connected                        |          |
| 89  | GND                | Ground                               |          |
| 90  | I2C_CLK            | I2C clock                            |          |
| 91  | I2C_DATA           | I2C data                             |          |
| 92  | SMB_CLK            | SM bus clock                         |          |
| 93  | SMB_DATA           | SM bus data                          |          |
| 94  | GND                | Ground                               |          |
| 95  | SMB_ALERT#         | SM bus alert                         |          |
| 96  | PCIE_WAKE#         | PCle wake                            |          |
| 97  | PCIE_PLTRST#       | PCle platform reset                  |          |
| 98  | DP1_HPD            | DP 1 hot plug detect                 |          |
| 99  | DP1_EN#            | DP 1 enable                          |          |
| 100 | PS_ON#             | Power supply enable / disable        |          |
| P1  | +5VSB_OUT          | 5 V standby power output             | 2 A max. |
| P2  | +12V_IN / +12V_OUT | 12 V power input / 12 V power output | 3 A max. |
| P3  | +12V_IN / +12V_OUT | 12 V power input / 12 V power output | 3 A max. |
| P4  | +12V_IN / +12V_OUT | 12 V power input / 12 V power output | 3 A max. |

| Pin                         | Signal            | Description | Note |
|-----------------------------|-------------------|-------------|------|
| <b>Connector Type</b>       |                   |             |      |
| B2B, 2x50-pin, 0.5 mm pitch |                   |             |      |
| <b>Mating Connector</b>     |                   |             |      |
| Vendor                      | HRS               |             |      |
| Model No.                   | FX23-100P-0.5SV20 |             |      |

## 7.19. Switches and Jumpers

The product has several jumpers which must be properly configured to ensure correct operation.

Figure 32: Jumper Connector



For a three-pin jumper (see Figure 32), the jumper setting is designated "1-2" when the jumper connects pins 1 and 2. The jumper setting is designated "2-3" when pins 2 and 3 are connected and so on. You will see that one of the lines surrounding a jumper pin is thick, which indicates pin No.1.

To move a jumper from one position to another, use needle-nose pliers or tweezers to pull the pin cap off the pins and move it to the desired position.

### 7.19.1. LVDS Backlight Control Selection (JP1)

The 2.0 mm pitch "LVDS Backlight Control Selection" jumper (JP1) can be used to select by which mode the brightness level in the LCD panel is controlled.

Figure 33: LVDS Backlight Control Selection JP1



Table 39: Pin Assignment JP1

| Jumper 1 Position |         | Description          |
|-------------------|---------|----------------------|
| Pin 1-2           | Pin 2-3 |                      |
| X                 | -       | PWM Control Mode     |
| -                 | X       | Voltage Control Mode |

"X" = Jumper set (short) and "-" = jumper not set (open)

### 7.19.2. M.2 Key B Selection (JP2)

The 2.0 mm pitch "M.2 Key B Selection" jumper (JP2) can be used to select which interface of M.2 SSD the M.2 Key B slot supports.

Figure 34: M.2 Key B Selection JP2

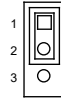


Table 40: Pin Assignment JP2

| Jumper 1 Position |         | Description    |
|-------------------|---------|----------------|
| Pin 1-2           | Pin 2-3 |                |
| X                 | -       | PCIe x1        |
| -                 | X       | SATA (Default) |

"X" = Jumper set (short) and "-" = jumper not set (open)

### 7.19.3. LVDS Panel Power Selection (JP3)

The 2.54 mm pitch "LVDS Panel Power Selection" jumper (JP3) can be used to select LVDS panel and backlight power voltage.

Figure 35: LVDS Panel Power Selection JP3

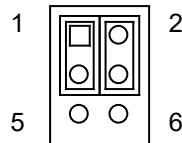


Table 41: Pin Assignment JP3

| Jumper 1 Position |         | Description             |
|-------------------|---------|-------------------------|
| Pin 1-3           | Pin 3-5 |                         |
| X                 | -       | Backlight Power = +12 V |
| -                 | X       | Backlight Power = +5 V  |
| Jumper 2 Position |         | Description             |
| Pin 2-4           | Pin 4-6 |                         |
| X                 | -       | Panel Power = +3.3 V    |
| -                 | X       | Panel Power = +5 V      |

"X" = Jumper set (short) and "-" = jumper not set (open)

#### 7.19.4. LVDS Backlight Enable Selection (JP4)

The 2.0 mm patch "LVDS Backlight Enable Selection" jumper (JP4) can be used to select the polarity of backlight enable signal.

Figure 36: LVDS Backlight Enable Selection JP4



Table 42: Pin Assignment JP4

| Jumper 1 Position |         | Description |
|-------------------|---------|-------------|
| Pin 1-2           | Pin 2-3 |             |
| X                 | -       | High Active |
| -                 | X       | Low Active  |

"X" = Jumper set (short) and "-" = jumper not set (open)

#### 7.19.5. LVDS Backlight Enable Voltage Selection (JP5)

The 2.0 mm patch "LVDS Backlight Enable Voltage Selection" jumper (JP5) can be used to select voltage level of backlight enable signal.

Figure 37: LVDS Backlight Enable Voltage Selection JP5



Table 43: Pin Assignment JP5

| Jumper 1 Position |         | Description |
|-------------------|---------|-------------|
| Pin 1-2           | Pin 2-3 |             |
| X                 | -       | +3.3 V      |
| -                 | X       | +5 V        |

"X" = Jumper set (short) and "-" = jumper not set (open)

### 7.19.6. Flash Descriptor Security Override Selection (JP6)

The 2.0 mm pitch "Flash Descriptor Security Override Selection" jumper (JP6) can be used to specify whether to override the flash descriptor.

Figure 38: Flash Descriptor Security Override Selection JP6



Table 44: Pin Assignment JP6

| Jumper 1 Position |         | Description             |
|-------------------|---------|-------------------------|
| Pin 1-2           | Pin 2-3 |                         |
| X                 | -       | Normal Operation        |
| -                 | X       | Flash Security Override |

"X" = Jumper set (short) and "-" = jumper not set (open)

### 7.19.7. AT / ATX Power Mode Selection (JP7)

The 2.0 mm pitch jumper JP7 can be used to select AT power mode or ATX power mode.

Figure 39: AT / ATX Power Mode Selection JP7



Table 45: Pin Assignment JP7

| Jumper 1 Position |         | Description    |
|-------------------|---------|----------------|
| Pin 1-2           | Pin 2-3 |                |
| X                 | -       | ATX Power Mode |
| -                 | X       | AT Power Mode  |

"X" = Jumper set (short) and "-" = jumper not set (open)

### 7.19.8. Clear CMOS Selection (JP8)

The 2.0 mm pitch "Clear COMS Selection" jumper (JP8) can be used to reset the Real Time Clock (RTC) and drain RTC well.

The jumper has one position: Pin 1-2 mounted (default position) and Pin 2-3 mounted. More information on setting the "Clear CMOS Selection" jumper can be found in the following table.

Figure 40: Clear CMOS Selection JP8



Table 46: Pin Assignment JP8

| Jumper 1 Position |         | Description                                                       |
|-------------------|---------|-------------------------------------------------------------------|
| Pin 1-2           | Pin 2-3 |                                                                   |
| X                 | -       | Normal Operation (default position)                               |
| -                 | X       | Clear CMOS (board does not boot with the jumper in this position) |

"X" = Jumper set (short) and "-" = jumper not set (open)



Do not leave the jumper in position 2-3, otherwise if the power is disconnected, the battery will fully deplete within a few weeks.

### 7.19.9. MFG Mode Selection (JP9)

The 2.0 mm pitch "MFG Mode Selection" jumper (JP9) can be used to rewrite Intel ME firmware onto another version.

Figure 41: MFG Mode Selection JP9



Table 47: Pin Assignment JP9

| Jumper 1 Position |         | Description      |
|-------------------|---------|------------------|
| Pin 1-2           | Pin 2-3 |                  |
| X                 | -       | Normal Operation |
| -                 | X       | Enable MFG Mode  |

"X" = Jumper set (short) and "-" = jumper not set (open)

### 7.19.10. USB Power Selection (JP10)

The 2.0 mm pitch "USB Power Selection" jumper (JP10) can be used to determine whether the USB ports are powered in the S4 / S5 state.

Figure 42: USB Power Selection JP10



Table 48: Pin Assignment JP10

| Jumper 1 Position |         | Description |
|-------------------|---------|-------------|
| Pin 1-2           | Pin 2-3 |             |
| X                 | -       | +5 V        |
| -                 | X       | +5 VSB      |

"X" = Jumper set (short) and "-" = jumper not set (open)

## 8/ BIOS

### 8.1. Starting the uEFI BIOS

The 3.5"-SBC-TGL is provided with a Kontron-customized, pre-installed and configured version of AMI Aptio® V uEFI BIOS. AMI BIOS firmware is based on the Unified Extensible Firmware Interface (UEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the 3.5"-SBC-TGL.

The uEFI BIOS comes with a setup program that provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The setup program allows the accessing of various menus that provide functions or access to sub-menus with more specific functions of their own.

To start the uEFI BIOS setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <DEL> key.
4. If the uEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see Security menu), press <RETURN>, and proceed with step 5.
5. A setup menu will appear.

The 3.5"-SBC-TGL uEFI BIOS setup program uses a hot key-based navigation system. A hot key legend bar is located on the bottom of the setup screens.

The following table provides information concerning the usage of these hot keys.

**Table 49: Hotkeys Table**

| Signal     | Description                                                                                                                                        |
|------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| <F1>       | The <F1> key invokes the General Help window.                                                                                                      |
| <->        | The <Minus> key selects the next lower value within a field.                                                                                       |
| <+>        | The <Plus> key selects the next higher value within a field.                                                                                       |
| <F2>       | The <F2> key loads the previous values.                                                                                                            |
| <F3>       | The <F3> key loads the standard default values.                                                                                                    |
| <F4>       | The <F4> key saves the current settings and exit the uEFI BIOS setup.                                                                              |
| <→> or <←> | The <Left/Right> arrows selects major setup menus on the menu bar. For example: Main, Advanced, Security, etc.                                     |
| <↑> or <↓> | The <Up/Down> arrows selects fields in the current menu. For example: A setup function or a sub-screen.                                            |
| <ESC>      | The <ESC> key exits a major setup menu and enter the Exit setup menu.<br>Pressing the <ESC> key in a sub-menu displays the next higher menu level. |
| <RETURN>   | The <RETURN> key executes a command or select a submenu.                                                                                           |

## 8.2. Starting the uEFI BIOS

The Setup utility features shows six menus in the selection bar at the top of the screen:

- ▶ Main
- ▶ Advanced
- ▶ Power
- ▶ Boot
- ▶ Security
- ▶ Save & Exit

The Setup menus are selected via the left and right arrow keys. The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white. Each Setup menu provides two main frames. The left frame displays all available functions. Functions that can be configured are displayed in blue. Functions displayed in gray provide information about the status or the operational configuration. The right frame displays an Item Specific Help window providing an explanation of the respective function.

### 8.2.1. Main Setup Menu

Upon entering the uEFI BIOS Setup program, the Main Setup menu is displayed. This screen lists the Main Setup menu sub-screens and provides basic system information. Additionally functions for setting the system time and date are offered.

**Table 50: Main Setup Menu Sub-Screens and Functions**

| Function                       | Description                                                                                                      |
|--------------------------------|------------------------------------------------------------------------------------------------------------------|
| Product, BIOS & ME Information | Read only field.<br>Displays information about the product, system BIOS and Intel Management Engine (ME) version |
| CPU Information                | Read only field<br>Display information about the processor                                                       |
| Memory Information             | Read only field.<br>Displays information about total memory                                                      |
| Board Information              | Read only field.<br>Displays information about UUID, serial number and LAN address                               |
| System Date                    | Set System Date                                                                                                  |
| System Time                    | Set System Time                                                                                                  |

Figure 43: BIOS Main Menu Screen System Data and Time

| BIOS SETUP UTILITY                          |                                      |       |      |                        |             |
|---------------------------------------------|--------------------------------------|-------|------|------------------------|-------------|
| Main                                        | Advanced                             | Power | Boot | Security               | Save & Exit |
| Product Information                         |                                      |       |      |                        |             |
| Product Name                                | 3.5-SBC-TGL                          |       |      |                        |             |
| BIOS Version                                | TGLUVEX.T00F (x64)                   |       |      |                        |             |
| BIOS Build Date                             | 12/15/2021                           |       |      |                        |             |
| ME Firmware Version                         | 15.0.30.1776 (Corporate)             |       |      |                        |             |
| CPU Information                             |                                      |       |      |                        |             |
| 11th Gen Intel® Core™ i5-1145GRE @ 2.60 GHz |                                      |       |      |                        |             |
| Microcode Revision                          | 9A                                   |       |      |                        |             |
| Processor Cores                             | 4 Core(s) / 8 Thread(s)              |       |      |                        |             |
| Memory Information                          |                                      |       |      |                        |             |
| Total Size                                  | 15872 MB (DDR4)                      |       |      |                        |             |
| Frequency                                   | 2667 MT/s                            |       |      |                        |             |
| Board Information                           |                                      |       |      |                        |             |
| UUID                                        | 737AC850-2C5A-11B2-8001-00500808D21B |       |      | → ←: Select Screen     |             |
| Serial #                                    | 00000000                             |       |      | ↑ ↓: Select Item       |             |
| LAN1 MAC Address                            | 00:50:08:08:D2:1B                    |       |      | Enter: Select          |             |
| LAN2 MAC Address                            | 00:50:08:08:D2:1C                    |       |      | +/-: Change Opt.       |             |
| System Date                                 | [Tue 12/28/2021]                     |       |      | F1: General Help       |             |
| System Time                                 | [13:43:40]                           |       |      | F2: Previous Values    |             |
| Access Level                                | Administrator                        |       |      | F3: Optimized Defaults |             |
|                                             |                                      |       |      | F4: Save & Exit        |             |
|                                             |                                      |       |      | ESC: Exit              |             |
| Version 2.22.1282 Copyright (C) 2021 AMI    |                                      |       |      |                        |             |

| Feature     | Option       | Description                                            |
|-------------|--------------|--------------------------------------------------------|
| System Date | [dd/mm/yyyy] | Set the Date. Use Tab to switch between Data elements. |
| System Time | [hh:mm:ss]   | Set the Time. Use Tab to switch between Time elements. |

## 8.2.2. Advanced Setup Menu

The Advanced setup menu provides sub-screens and functions for advanced configurations. The following sub-screen functions are included in the menu:

- ▶ Audio & LAN Configuration
- ▶ Display Configuration
- ▶ CPU Chipset Configuration
- ▶ NVMe Configuration
- ▶ SATA Configuration
- ▶ USB Configuration
- ▶ AMT Configuration
- ▶ Trusted Computing
- ▶ DIO Configuration
- ▶ Network Stack
- ▶ Super IO Configuration
- ▶ H/W Monitor

---

**NOTICE**

Setting items on this screen to incorrect values may cause the system to malfunction.

---

Figure 44: BIOS Advanced Menu

| BIOS SETUP UTILITY                       |          |            |      |                                                                                                                                                                                  |             |
|------------------------------------------|----------|------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Main                                     | Advanced | Power      | Boot | Security                                                                                                                                                                         | Save & Exit |
| HD Audio                                 |          | [Enabled]  |      |                                                                                                                                                                                  |             |
| Onboard LAN1 Controller                  |          | [Enabled]  |      |                                                                                                                                                                                  |             |
| Onboard LAN2 Controller                  |          | [Enabled]  |      |                                                                                                                                                                                  |             |
| Load Intel I226-IT UNDI*                 |          | [Disabled] |      |                                                                                                                                                                                  |             |
| Load Intel I210 UNDI**                   |          | [Disabled] |      |                                                                                                                                                                                  |             |
| > Display Configuration                  |          |            |      | → ←: Select Screen<br>↑ ↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit |             |
| > CPU Chipset Configuration              |          |            |      |                                                                                                                                                                                  |             |
| > NVMe Configuration                     |          |            |      |                                                                                                                                                                                  |             |
| > SATA Configuration                     |          |            |      |                                                                                                                                                                                  |             |
| > USB Configuration                      |          |            |      |                                                                                                                                                                                  |             |
| > AMT Configuration                      |          |            |      |                                                                                                                                                                                  |             |
| > Trusted Computing                      |          |            |      |                                                                                                                                                                                  |             |
| > DIO Configuration                      |          |            |      |                                                                                                                                                                                  |             |
| > Network Stack                          |          |            |      |                                                                                                                                                                                  |             |
| > Super IO Configuration                 |          |            |      |                                                                                                                                                                                  |             |
| > H/W Monitor                            |          |            |      |                                                                                                                                                                                  |             |
| Version 2.22.1282 Copyright (C) 2021 AMI |          |            |      |                                                                                                                                                                                  |             |

\* This item appears only when enabling Onboard LAN1 Controller.

\*\* This item appears only when enabling Onboard LAN2 Controller.

| Feature                 | Option                   | Description                                                                                                                                       |
|-------------------------|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| HD Audio                | [Disabled],<br>[Enabled] | Control Detection of the HD-Audio device.<br>[Disabled]: HDA will be unconditionally disabled.<br>[Enabled]: HDA will be unconditionally enabled. |
| Onboard LAN1 Controller | [Disabled],<br>[Enabled] | Select whether to enable or disable Onboard LAN1 Controller. Intel-i226-IT.                                                                       |
| Onboard LAN2 Controller | [Disabled],<br>[Enabled] | Select whether to enable or disable Onboard LAN2 Controller. Intel-i210.                                                                          |
| Load Intel I226-IT UNDI | [Disabled],<br>[Enabled] | Load onboard UNDI (Universal Network Driver Interface) for Intel I226-IT.                                                                         |
| Load I210 UNDI Driver   | [Disabled],<br>[Enabled] | Load onboard UNDI (Universal Network Driver Interface) for Intel I210.                                                                            |

Figure 45: BIOS Advanced Menu - Display Configuration

| BIOS SETUP UTILITY                               |          |                |      |                                                                                                                                                                                  |             |
|--------------------------------------------------|----------|----------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Main                                             | Advanced | Power          | Boot | Security                                                                                                                                                                         | Save & Exit |
| Display Configuration                            |          |                |      | → ←: Select Screen<br>↑ ↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit |             |
| Aperture Size                                    |          | [256MB]        |      |                                                                                                                                                                                  |             |
| DVMT Pre-Allocated                               |          | [64M]          |      |                                                                                                                                                                                  |             |
| DVMT Total Gfx Mem                               |          | [256MB]        |      |                                                                                                                                                                                  |             |
| Active LVDS                                      |          | [Disabled]     |      |                                                                                                                                                                                  |             |
| LVDS Panel Type*                                 |          | [1366x768 1CH] |      |                                                                                                                                                                                  |             |
| LVDS Panel Color Depth*                          |          | [18Bit]        |      |                                                                                                                                                                                  |             |
| PWM Backlight Control*                           |          | [By External]  |      |                                                                                                                                                                                  |             |
| LVDS Backlight Control Mode*                     |          | [PWM]          |      |                                                                                                                                                                                  |             |
| LVDS Backlight Control - PWM <sup>*(1)(2)</sup>  |          | 127            |      |                                                                                                                                                                                  |             |
| LVDS Backlight Control - Voltage <sup>*(3)</sup> |          | [2.5 V]        |      |                                                                                                                                                                                  |             |
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\* These items appear only when enabling Active LVDS.

<sup>(1)</sup> These items appear only when selecting By External for PWM Backlight Control.

<sup>(2)</sup> This item appears only when selecting PWM for the LVDS Backlight Control Mode.

<sup>(3)</sup> This item appears only when selecting Voltage for the LVDS Backlight Control Mode.

| Feature            | Option                                                                                                          | Description                                                                                                                                                                 |
|--------------------|-----------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Aperture Size      | [128MB],<br>[256MB],<br>[512MB],<br>[1024MB]                                                                    | Select the Aperture Size.<br>Note: Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM Support. |
| DVMT Pre-Allocated | [32M],<br>[64M],<br>[96M],<br>[128M],<br>[160M]                                                                 | Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.                                                                            |
| DVMT Total Gfx Mem | [128M],<br>[256M],<br>[MAX]                                                                                     | Select DVMT 5.0 Total Graphic Memory size used by the Internal Graphics Device.                                                                                             |
| Active LVDS        | [Disabled],<br>[Enabled]                                                                                        | Select the Active LVDS Configuration.<br>[Disabled]: don't enable LVDS.<br>[Enabled]: enable LVDS.                                                                          |
| LVDS Panel Type    | [800x600 1CH],<br>[1024x768 1CH],<br>[1280x1024 2CH],<br>[1366x768 1CH],<br>[1366x768 2CH],<br>[1600x1200 2CH], | LVDS panel by selecting the appropriate setup item.                                                                                                                         |

| Feature                          | Option                                                                                                                          | Description                                                                                              |
|----------------------------------|---------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|
|                                  | [1920x1080 2CH]                                                                                                                 |                                                                                                          |
| LVDS Panel Color Depth           | [18Bit],<br>[24Bit]                                                                                                             | LVDS panel color depth by appropriate setup item.                                                        |
| PWM Backlight Control            | [By External],<br>[By Internal]                                                                                                 | [By External]: Control by external HW circuit.<br>[By Internal]: Control by LBKL_CTL on the PCH Chipset. |
| LVDS Backlight Control Mode      | [Voltage],<br>[PWM]                                                                                                             | CNx LVDS Backlight Power Wafer output control<br>[Voltage]: Pin 1 output<br>[PWM]: Pin 2 output          |
| LVDS Backlight Control - PWM     | Value input                                                                                                                     | 0 – 255 PWM Duty                                                                                         |
| LVDS Backlight Control - Voltage | [0.0 V],<br>[0.5 V],<br>[1.0 V],<br>[1.5 V],<br>[2.0 V],<br>[2.5 V],<br>[3.0 V],<br>[3.5 V],<br>[4.0 V],<br>[4.5 V],<br>[5.0 V] | Min: 0.0 V<br>Max: 5.0 V                                                                                 |

Figure 46: BIOS Advanced Menu - CPU Chipset Configuration

| BIOS SETUP UTILITY                       |          |            |      |                        |             |
|------------------------------------------|----------|------------|------|------------------------|-------------|
| Main                                     | Advanced | Power      | Boot | Security               | Save & Exit |
| CPU Chipset Configuration                |          |            |      |                        |             |
| Intel® SpeedStep™                        |          | [Enabled]  |      |                        |             |
| Turbo Mode                               |          | [Enabled]  |      |                        |             |
| Hyper-Threading                          |          | [Enabled]  |      |                        |             |
| VT-d                                     |          | [Disabled] |      | → ←: Select Screen     |             |
| Active Processor Cores                   |          | [All]      |      | ↑ ↓: Select Item       |             |
| Configurable TDP Mode                    |          | [28W]      |      | Enter: Select          |             |
| Intel (VMX) Virtualization Technology    |          | [Enabled]  |      | +/-: Change Opt.       |             |
| Intel Trusted Execution Technology       |          | [Disabled] |      | F1: General Help       |             |
| CPU CrashLog (Device 10)                 |          | [Disabled] |      | F2: Previous Values    |             |
| GNA Device (B0:D8:F0)                    |          | [Disabled] |      | F3: Optimized Defaults |             |
| IPU Device (B0:D5:F0)                    |          | [Disabled] |      | F4: Save & Exit        |             |
| IPU IMR Configuration**                  |          | [IPU Gen]  |      | ESC: Exit              |             |
| Version 2.22.1282 Copyright (C) 2021 AMI |          |            |      |                        |             |

\* This item appears only when enabling Intel® SpeedStep™.

\*\* This item appears only when enabling IPU Device.

| Feature                               | Option                        | Description                                                                                             |
|---------------------------------------|-------------------------------|---------------------------------------------------------------------------------------------------------|
| Intel® SpeedStep™                     | [Disabled],<br>[Enabled]      | Allows more than two frequency ranges to be supported.                                                  |
| Turbo Mode                            | [Disabled],<br>[Enabled]      | Enable / Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.                 |
| Hyper-Threading                       | [Disabled],<br>[Enabled]      | Enable or Disable Hyper-Threading Technology.                                                           |
| VT-d                                  | [Disabled],<br>[Enabled]      | Select whether to enable or disable VT-d capability.                                                    |
| Active Processor Cores                | [All],<br>[1],<br>[2],<br>[3] | Number of cores to enable in each processor package.                                                    |
| Configurable TDP Mode                 | [28W],<br>[15W],<br>[12W]     | Configurable TDP Mode as 28W / 15W / 12W TDP selection. Celeron cannot support it.                      |
| Intel (VMX) Virtualization Technology | [Disabled],<br>[Enabled]      | When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. |
| Intel Trusted Execution Technology    | [Disabled]                    | Read only item.                                                                                         |
| CPU CrashLog (Device 10)              | [Enabled],<br>[Disabled]      | Enable / Disable CPU CrashLog Device.                                                                   |
| GNA Device                            | [Enabled],                    | Enable / Disable SA GNA Device.                                                                         |

| Feature               | Option                     | Description                       |
|-----------------------|----------------------------|-----------------------------------|
| (B0:D8:F0)            | [Disabled]                 |                                   |
| IPU Device (B0:D5:F0) | [Enabled],<br>[Disabled]   | Enable / Disable SA IPU Device.   |
| IPU IMR Configuration | [IPU Camera],<br>[IPU Gen] | Select the IPU IMR configuration. |

Figure 47: BIOS Advanced Menu - NVMe Configuration

| BIOS SETUP UTILITY                       |          |       |      |                                                                                                                                                                                  |             |
|------------------------------------------|----------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Main                                     | Advanced | Power | Boot | Security                                                                                                                                                                         | Save & Exit |
| NVMe Configuration                       |          |       |      |                                                                                                                                                                                  |             |
| No NVMe Device Found                     |          |       |      | → ←: Select Screen<br>↑ ↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit |             |
| Version 2.22.1282 Copyright (C) 2021 AMI |          |       |      |                                                                                                                                                                                  |             |

Figure 48: BIOS Advanced Menu - SATA Configuration

| BIOS SETUP UTILITY                        |          |                    |      |                                                                                                   |             |
|-------------------------------------------|----------|--------------------|------|---------------------------------------------------------------------------------------------------|-------------|
| Main                                      | Advanced | Power              | Boot | Security                                                                                          | Save & Exit |
| SATA Configuration                        |          |                    |      |                                                                                                   |             |
| SATA Controller(s)                        |          | [Enabled]          |      | → ←: Select Screen<br>↑ ↓: Select Item                                                            |             |
| Serial ATA Port 0 (CN27)*<br>Port 0*      |          | Empty<br>[Enabled] |      | Enter: Select<br>+/-: Change Opt.                                                                 |             |
| Serial ATA Port 1 (M.2 Key-B)*<br>Port 1* |          | Empty<br>[Enabled] |      | F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit |             |
| Version 2.22.1282 Copyright (C) 2021 AMI  |          |                    |      |                                                                                                   |             |

\* These items appear only when enabling SATA Controller(s).

| Feature            | Option                   | Description                                                    |
|--------------------|--------------------------|----------------------------------------------------------------|
| SATA Controller(s) | [Enabled],<br>[Disabled] | Enable / Disable SATA Device.                                  |
| Port 0, 1          | [Disabled],<br>[Enabled] | Select whether to enable or disable SATA Controller Port 0, 1. |

Figure 49: BIOS Advanced Menu - USB Configuration

| BIOS SETUP UTILITY                       |          |           |      |                        |             |
|------------------------------------------|----------|-----------|------|------------------------|-------------|
| Main                                     | Advanced | Power     | Boot | Security               | Save & Exit |
| USB Configuration                        |          |           |      |                        |             |
| USB Devices:                             |          |           |      | → ←: Select Screen     |             |
| 1 Keyboard                               |          |           |      | ↑ ↓: Select Item       |             |
| XHCI Hand-off                            |          | [Enabled] |      | Enter: Select          |             |
| USB Mass Storage Driver Support          |          | [Enabled] |      | +/-: Change Opt.       |             |
|                                          |          |           |      | F1: General Help       |             |
|                                          |          |           |      | F2: Previous Values    |             |
|                                          |          |           |      | F3: Optimized Defaults |             |
|                                          |          |           |      | F4: Save & Exit        |             |
|                                          |          |           |      | ESC: Exit              |             |
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| Feature                         | Option                   | Description                                                                                                              |
|---------------------------------|--------------------------|--------------------------------------------------------------------------------------------------------------------------|
| XHCI Hand-off                   | [Enabled],<br>[Disabled] | This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver. |
| USB Mass Storage Driver Support | [Disabled],<br>[Enabled] | Enable / Disable USB Mass Storage Driver Support.                                                                        |

Figure 50: BIOS Advanced Menu - AMT Configuration

| BIOS SETUP UTILITY                       |          |            |      |                        |             |
|------------------------------------------|----------|------------|------|------------------------|-------------|
| Main                                     | Advanced | Power      | Boot | Security               | Save & Exit |
| AMT Configuration                        |          |            |      |                        |             |
| AMT BIOS Features                        |          | [Enabled]  |      | → ←: Select Screen     |             |
| Unconfigure ME*                          |          | [Disabled] |      | ↑ ↓: Select Item       |             |
|                                          |          |            |      | Enter: Select          |             |
|                                          |          |            |      | +/-: Change Opt.       |             |
|                                          |          |            |      | F1: General Help       |             |
|                                          |          |            |      | F2: Previous Values    |             |
|                                          |          |            |      | F3: Optimized Defaults |             |
|                                          |          |            |      | F4: Save & Exit        |             |
|                                          |          |            |      | ESC: Exit              |             |
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\* This item is selectable only when enabling AMT BIOS Features.

| Feature           | Option                   | Description                                                                                                                                                                  |
|-------------------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AMT BIOS Features | [Disabled],<br>[Enabled] | When disabled AMT BIOS Features are no longer supported and user is no longer able to access MEBx Setup.<br>Note: This option does not disable Manageability Features in FW. |
| Unconfigure ME    | [Disabled],<br>[Enabled] | OEMFlag Bit 15: Unconfigure ME with resetting MEBx password to default.                                                                                                      |

Figure 51: BIOS Advanced Menu - Trusted Computing

| BIOS SETUP UTILITY                       |          |            |      |                                                                                                                                                                                  |             |
|------------------------------------------|----------|------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Main                                     | Advanced | Power      | Boot | Security                                                                                                                                                                         | Save & Exit |
| Configuration                            |          |            |      |                                                                                                                                                                                  |             |
| Security Device Support                  |          | [Disabled] |      |                                                                                                                                                                                  |             |
| No Security Device Found                 |          |            |      | → ←: Select Screen<br>↑ ↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit |             |
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| Feature                 | Option                   | Description                                                                                                                                            |
|-------------------------|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| Security Device Support | [Disabled],<br>[Enabled] | Enable or Disable BIOS support for security device.<br>O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. |

Figure 52: BIOS Advanced Menu - DIO Configuration

| BIOS SETUP UTILITY                       |          |               |      |                        |             |
|------------------------------------------|----------|---------------|------|------------------------|-------------|
| Main                                     | Advanced | Power         | Boot | Security               | Save & Exit |
| DIO Configuration                        |          |               |      |                        |             |
| User Configuration                       |          | [Disabled]    |      |                        |             |
| Force unlock on all GPIO pads            |          | [Enabled]     |      |                        |             |
| DIO_0*                                   |          | [Output High] |      |                        |             |
| DIO_1*                                   |          | [Output High] |      |                        |             |
| DIO_2*                                   |          | [Output High] |      |                        |             |
| DIO_3*                                   |          | [Output High] |      |                        |             |
| DIO_4*                                   |          | [Output High] |      |                        |             |
| DIO_5*                                   |          | [Output High] |      |                        |             |
| DIO_6*                                   |          | [Output High] |      |                        |             |
| DIO_7*                                   |          | [Output High] |      |                        |             |
| DIO_0 Value                              |          |               |      | → ←: Select Screen     |             |
| DIO_1 Value                              |          |               |      | ↑ ↓: Select Item       |             |
| DIO_2 Value                              |          |               |      | Enter: Select          |             |
| DIO_3 Value                              |          |               |      | +/-: Change Opt.       |             |
| DIO_4 Value                              |          |               |      | F1: General Help       |             |
| DIO_5 Value                              |          |               |      | F2: Previous Values    |             |
| DIO_6 Value                              |          |               |      | F3: Optimized Defaults |             |
| DIO_7 Value                              |          |               |      | F4: Save & Exit        |             |
|                                          |          |               |      | ESC: Exit              |             |
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\* These items appear only when enabling User Configuration.

| Feature                       | Option                                     | Description                                                       |
|-------------------------------|--------------------------------------------|-------------------------------------------------------------------|
| User Configuration            | [Enabled],<br>[Disabled]                   | User can set the DO pin output value.                             |
| Force unlock on all GPIO pads | [Disabled],<br>[Enabled]                   | If Enabled BIOS will force all GPIO pads to be in unlocked state. |
| DIO_0..7                      | [Output Low],<br>[Output High],<br>[Input] | Setting the DO pin output value.                                  |

Figure 53: BIOS Advanced Menu - Network Stack

| BIOS SETUP UTILITY                       |          |            |      |                                                                                                                                                                                  |             |
|------------------------------------------|----------|------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Main                                     | Advanced | Power      | Boot | Security                                                                                                                                                                         | Save & Exit |
| IPv4 PXE Support                         |          | [Enabled]  |      |                                                                                                                                                                                  |             |
| IPv6 PXE Support                         |          | [Disabled] |      |                                                                                                                                                                                  |             |
|                                          |          |            |      | → ←: Select Screen<br>↑ ↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit |             |
| Version 2.22.1282 Copyright (C) 2021 AMI |          |            |      |                                                                                                                                                                                  |             |

| Feature          | Option                   | Description                                                                                          |
|------------------|--------------------------|------------------------------------------------------------------------------------------------------|
| IPv4 PXE Support | [Disabled],<br>[Enabled] | Enable / Disable IPv4 PXE boot support.<br>If disabled, IPv4 PXE boot support will not be available. |
| IPv6 PXE Support | [Disabled],<br>[Enabled] | Enable / Disable IPv6 PXE boot support.<br>If disabled, IPv6 PXE boot support will not be available. |

Figure 54: BIOS Advanced Menu - Super IO Configuration

| BIOS SETUP UTILITY                                                                           |          |       |      |                                                                                                                                                                                  |             |
|----------------------------------------------------------------------------------------------|----------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Main                                                                                         | Advanced | Power | Boot | Security                                                                                                                                                                         | Save & Exit |
| Super IO Configuration<br><br>> Serial Port 1 Configuration<br>> Serial Port 2 Configuration |          |       |      |                                                                                                                                                                                  |             |
|                                                                                              |          |       |      | → ←: Select Screen<br>↑ ↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit |             |
| Version 2.22.1282 Copyright (C) 2021 AMI                                                     |          |       |      |                                                                                                                                                                                  |             |

Figure 55: BIOS Advanced Menu - Super IO Configuration - Serial Port 1 Configuration

| BIOS SETUP UTILITY                       |          |                 |      |                        |             |
|------------------------------------------|----------|-----------------|------|------------------------|-------------|
| Main                                     | Advanced | Power           | Boot | Security               | Save & Exit |
| Super Port 1 Configuration               |          |                 |      |                        |             |
| Serial Port                              |          | [Enabled]       |      | → ←: Select Screen     |             |
| Device Settings*                         |          | IO=3F8h; IRQ=4; |      | ↑ ↓: Select Item       |             |
| Change Setting*                          |          | [Auto]          |      | Enter: Select          |             |
| Serial Port 1 Type*                      |          | [RS232]         |      | +/-: Change Opt.       |             |
| RS485 Deplx Mode*(1)                     |          | [Half Duplex]   |      | F1: General Help       |             |
| RS485 Auto Flow Control*(1)(3)           |          | [Disabled]      |      | F2: Previous Values    |             |
| RS485/422 Receiver Termination*(2)       |          | [Enabled]       |      | F3: Optimized Defaults |             |
|                                          |          |                 |      | F4: Save & Exit        |             |
|                                          |          |                 |      | ESC: Exit              |             |
| Version 2.22.1282 Copyright (C) 2021 AMI |          |                 |      |                        |             |

\* These items appear only when enabling Serial Port.

(1) These items appear only when selecting RS485 for the Serial Port 1 Type.

(2) This item appears only when selecting RS485 or RS422 for the Serial Port 1 Type.

(3) This item appear only when selecting Half Duplex for RS485 Auto Flow Control.

| Feature         | Option                                                                         | Description                                     |
|-----------------|--------------------------------------------------------------------------------|-------------------------------------------------|
| Serial Port     | [Disabled],<br>[Enabled]                                                       | Enable or Disable Serial Port (COM).            |
| Change Settings | [Auto],<br>[IO=3F8h; IRQ=4;],<br>[IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], | Select an optional setting for Super IO device. |

| Feature                        | Option                                                                                        | Description                                                         |
|--------------------------------|-----------------------------------------------------------------------------------------------|---------------------------------------------------------------------|
|                                | [IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;] |                                                                     |
| Serial Port 1 Type             | [RS232],<br>[RS422],<br>[RS485]                                                               | Select an appropriate type for Serial Port 1.                       |
| RS485 Duplex Mode              | [Half Duplex],<br>[Full Duplex]                                                               | Select an appropriate RS485 Duplex Mode.                            |
| RS485 Auto Flow Control        | [Disabled],<br>[Enabled]                                                                      | Select whether to enable or disable RS485 Auto Flow Control.        |
| RS485/422 Receiver Termination | [Disabled],<br>[Enabled]                                                                      | Select whether to enable or disable RS485/422 Receiver Termination. |

Figure 56: BIOS Advanced Menu - Super IO Configuration - Serial Port 2 Configuration

| BIOS SETUP UTILITY                       |          |                 |      |                        |             |
|------------------------------------------|----------|-----------------|------|------------------------|-------------|
| Main                                     | Advanced | Power           | Boot | Security               | Save & Exit |
| Super Port 2 Configuration               |          |                 |      |                        |             |
| Serial Port                              |          | [Enabled]       |      | → ←: Select Screen     |             |
| Device Settings*                         |          | IO=2F8h; IRQ=3; |      | ↑ ↓: Select Item       |             |
| Change Setting*                          |          | [Auto]          |      | Enter: Select          |             |
| Serial Port 2 Type*                      |          | [RS232]         |      | +/-: Change Opt.       |             |
| RS485 Duplex Mode*(1)                    |          | [Half Duplex]   |      | F1: General Help       |             |
| RS485 Auto Flow Control*(1)(3)           |          | [Disabled]      |      | F2: Previous Values    |             |
| RS485/422 Receiver Termination*(2)       |          | [Enabled]       |      | F3: Optimized Defaults |             |
|                                          |          |                 |      | F4: Save & Exit        |             |
|                                          |          |                 |      | ESC: Exit              |             |
| Version 2.22.1282 Copyright (C) 2021 AMI |          |                 |      |                        |             |

\* These items appear only when enabling Serial Port.

(1) These items appear only when selecting RS485 for the Serial Port 2 Type.

(2) This item appears only when selecting RS485 or RS422 for the Serial Port 2 Type.

(3) This item appears only when selecting Half Duplex for RS485 Auto Flow Control.

| Feature            | Option                                                                                                                                                                          | Description                                     |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------|
| Serial Port        | [Disabled],<br>[Enabled]                                                                                                                                                        | Enable or Disable Serial Port (COM).            |
| Change Settings    | [Auto],<br>[IO=2F8h; IRQ=3;],<br>[IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;],<br>[IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;] | Select an optional setting for Super IO device. |
| Serial Port 2 Type | [RS232],<br>[RS422],<br>[RS485]                                                                                                                                                 | Select an appropriate type for Serial Port 2.   |

| Feature                        | Option                          | Description                                                         |
|--------------------------------|---------------------------------|---------------------------------------------------------------------|
| RS485 Duplex Mode              | [Half Duplex],<br>[Full Duplex] | Select an appropriate RS485 Duplex Mode.                            |
| RS485 Auto Flow Control        | [Disabled],<br>[Enabled]        | Select whether to enable or disable RS485 Auto Flow Control.        |
| RS485/422 Receiver Termination | [Disabled],<br>[Enabled]        | Select whether to enable or disable RS485/422 Receiver Termination. |

Figure 57: BIOS Advanced Menu - H/W Monitor

| BIOS SETUP UTILITY                            |          |             |                        |           |             |
|-----------------------------------------------|----------|-------------|------------------------|-----------|-------------|
| Main                                          | Advanced | Power       | Boot                   | Security  | Save & Exit |
| PC Health Status<br>> Smart FAN Configuration |          |             |                        |           |             |
| CPU Temperature                               |          | : +36 C     | → ←: Select Screen     |           |             |
| System Temperature                            |          | : +32 C     | ↑ ↓: Select Item       |           |             |
| CPU Fan Speed                                 |          | : 7258 RPM  | Enter: Select          |           |             |
| +12VIN                                        |          | : +12.063 V | +/-: Change Opt.       |           |             |
| +3.3V                                         |          | : +3.312 V  | F1: General Help       |           |             |
| +5V                                           |          | : +5.039 V  | F2: Previous Values    |           |             |
| +3.3VA                                        |          | : +3.296 V  | F3: Optimized Defaults |           |             |
| +VRTC                                         |          | : +3.104 V  | F4: Save & Exit        |           |             |
|                                               |          |             |                        | ESC: Exit |             |
| Version 2.22.1282 Copyright (C) 2021 AMI      |          |             |                        |           |             |

Figure 58: BIOS Advanced Menu - H/W Monitor - Smart FAN Configuration

| BIOS SETUP UTILITY                       |          |          |      |                        |             |
|------------------------------------------|----------|----------|------|------------------------|-------------|
| Main                                     | Advanced | Power    | Boot | Security               | Save & Exit |
| Smart FAN Configuration                  |          |          |      |                        |             |
| CPU FAN Setting                          |          | [Manual] |      |                        |             |
| Manual Duty*                             |          | 255      |      | → ←: Select Screen     |             |
| 1st Boundary Temperature**               |          | 30       |      | ↑ ↓ : Select Item      |             |
| 1st FAN Speed**                          |          | 50       |      | Enter: Select          |             |
| 2nd Boundary Temperature**               |          | 40       |      | +/-: Change Opt.       |             |
| 2nd FAN Speed**                          |          | 100      |      | F1: General Help       |             |
| 3rd Boundary Temperature**               |          | 50       |      | F2: Previous Values    |             |
| 3rd FAN Speed**                          |          | 150      |      | F3: Optimized Defaults |             |
| 4th Boundary Temperature**               |          | 60       |      | F4: Save & Exit        |             |
| 4th FAN Speed**                          |          | 200      |      | ESC: Exit              |             |
| Version 2.22.1282 Copyright (C) 2021 AMI |          |          |      |                        |             |

\* This item appears only when selecting Manual for CPU FAN Setting.

\*\* These items appear only when selecting Smart for CPU FAN Setting.

| Feature                        | Option               | Description                      |
|--------------------------------|----------------------|----------------------------------|
| CPU FAN Setting                | [Manual],<br>[Smart] | Switch the CPU FAN control mode. |
| Manual Duty                    | Value Input          | 0 – 255 PWM Duty                 |
| 1st / 2nd / 3rd / 4th Boundary | Value Input          | 1 – 100 C                        |

| Feature                            | Option      | Description      |
|------------------------------------|-------------|------------------|
| Temperature                        |             |                  |
| 1st / 2nd / 3rd / 4th<br>FAN Speed | Value Input | 0 – 255 PWM Duty |

### 8.2.3. Power Setup Menu

The Power setup menu provides functions and a sub-screen for power configurations. The following sub-screen function is included in the menu:

- ▶ WatchDog Timer Configuration

Figure 59: BIOS Power Setup Menu

| BIOS SETUP UTILITY                       |          |                       |      |                        |             |
|------------------------------------------|----------|-----------------------|------|------------------------|-------------|
| Main                                     | Advanced | Power                 | Boot | Security               | Save & Exit |
| Power Configuration                      |          |                       |      |                        |             |
| ACPI Sleep State                         |          | [S3 (Suspend to RAM)] |      |                        |             |
| Restore AC Power Loss                    |          | [Power Off]           |      |                        |             |
| Power Saving Mode                        |          | [Disabled]            |      |                        |             |
| Resume Event Control                     |          |                       |      |                        |             |
| ResumeLan I226-IT                        |          | [Disabled]            |      |                        |             |
| ResumeLan I210                           |          | [Disabled]            |      |                        |             |
| Resume By PCI-E Device                   |          | [Disabled]            |      | → ←: Select Screen     |             |
| Resume By Ring Device                    |          | [Disabled]            |      | ↑ ↓ : Select Item      |             |
| Resume By RTC Alarm                      |          | [Disabled]            |      | Enter: Select          |             |
| RTC Alarm Mode <sup>(1)</sup>            |          | [Fixed Time]          |      | +/-: Change Opt.       |             |
| Time(Days)Alarm <sup>(2)</sup>           |          | 0                     |      | F1: General Help       |             |
| Time(hh)Alarm <sup>(1)</sup>             |          | 0                     |      | F2: Previous Values    |             |
| Time(mm)Alarm <sup>(1)</sup>             |          | 1                     |      | F3: Optimized Defaults |             |
| Time(ss)Alarm <sup>(1)</sup>             |          | 0                     |      | F4: Save & Exit        |             |
| > WatchDog Timer Configuration           |          |                       |      | ESC: Exit              |             |
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<sup>(1)</sup> These items appear only when enabling Resume By RTC Alarm.

<sup>(2)</sup> This item appears only when enabling Resume By RTC Alarm and selecting Fixed Time for RTC Alarm Mode.

| Feature               | Option                                          | Description                                                                                                                                                                                    |
|-----------------------|-------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ACPI Sleep State      | [Suspend Disabled],<br>[S3 (Suspend to RAM)]    | Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.                                                                                                  |
| Restore AC Power Loss | [Power Off],<br>[Power On],<br>[Last State]     | Select AC power state when power is re-applied after a power failure.                                                                                                                          |
| Power Saving Mode     | [Disabled],<br>[EUP Enabled]                    | Configure the Power Saving Mode configuration.<br>EUP AUX Power: Save Power for USB and PCIE-Slot components.<br>EUP SOC Power: Save Power for USB, PCIE-Slot, Lan and Chipset-SOC components. |
| ResumeLan I226-IT     | [Disabled],<br>[OS-Driver],<br>[FW-MagicPacket] | Select whether to enable Wake from LAN Device Intel I226-IT.                                                                                                                                   |

| Feature                | Option                                          | Description                                                                                      |
|------------------------|-------------------------------------------------|--------------------------------------------------------------------------------------------------|
| ResumeLan I210         | [Disabled],<br>[OS-Driver],<br>[FW-MagicPacket] | Select whether to enable Wake from LAN Device Intel I210.                                        |
| Resume By PCI-E Device | [Disabled],<br>[Enabled]                        | Select whether to enable Wake from PCI-E Device.                                                 |
| Resume By Ring Device  | [Disabled],<br>[Enabled]                        | Select whether to enable Wake from Ring Device.                                                  |
| Resume By RTC Alarm    | [Disabled],<br>[Enabled]                        | Select whether to enable Wake Up on Alarm, to turn on your system on a special day of the month. |
| RTC Alarm Mode         | [Fixed Time],<br>[After S4/S5]                  | Select an appropriate RTC Alarm Mode.                                                            |
| Date(Days)Alarm        | Value Input                                     | 0 - 31, 0 stands for every day.                                                                  |
| Time(hh)Alarm          | Value Input                                     | 0 - 23                                                                                           |
| Time(mm)Alarm          | Value Input                                     | 0 - 59                                                                                           |
| Time(ss)Alarm          | Value Input                                     | 0 - 59                                                                                           |

Figure 60: BIOS Power Setup Menu - WatchDog Timer Configuration

| BIOS SETUP UTILITY                       |          |            |      |                        |             |
|------------------------------------------|----------|------------|------|------------------------|-------------|
| Main                                     | Advanced | Power      | Boot | Security               | Save & Exit |
| WatchDog Timer Configuration             |          |            |      |                        |             |
| WDT Function                             |          | [Disabled] |      | → ←: Select Screen     |             |
| WDT Count Mode*                          |          | [Minute]   |      | ↑ ↓: Select Item       |             |
| WDT Timer*                               |          | 3          |      | Enter: Select          |             |
|                                          |          |            |      | +/-: Change Opt.       |             |
|                                          |          |            |      | F1: General Help       |             |
|                                          |          |            |      | F2: Previous Values    |             |
|                                          |          |            |      | F3: Optimized Defaults |             |
|                                          |          |            |      | F4: Save & Exit        |             |
|                                          |          |            |      | ESC: Exit              |             |
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\* These items appear only when enabling WDT Function.

| Feature        | Option                   | Description                                                  |
|----------------|--------------------------|--------------------------------------------------------------|
| WDT Function   | [Disabled],<br>[Enabled] | Select whether to enable or disable WatchDog Timer function. |
| WDT Count Mode | [Second],<br>[Minute]    | Select WatchDog Count Mode: Second or Minute.                |
| WDT Timer      | Value Input              | Count 0 - 255                                                |

## 8.2.4. Boot Setup Menu

The boot setup menu lists the for boot device priority order, that is generated dynamically.

Figure 61: BIOS Boot Setup Menu

| BIOS SETUP UTILITY                       |          |                            |      |                                                                                                                                                                                                                                                                 |             |
|------------------------------------------|----------|----------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Main                                     | Advanced | Power                      | Boot | Security                                                                                                                                                                                                                                                        | Save & Exit |
| Boot Configuration                       |          |                            |      | <div>→ ←: Select Screen</div> <div>↑ ↓: Select Item</div> <div>Enter: Select</div> <div>+/-: Change Opt.</div> <div>F1: General Help</div> <div>F2: Previous Values</div> <div>F3: Optimized Defaults</div> <div>F4: Save &amp; Exit</div> <div>ESC: Exit</div> |             |
| Full Screen LOGO Display                 |          | [Disabled]                 |      |                                                                                                                                                                                                                                                                 |             |
| Setup Prompt Timeout                     |          | 1                          |      |                                                                                                                                                                                                                                                                 |             |
| Bootup NumLock State                     |          | [On]                       |      |                                                                                                                                                                                                                                                                 |             |
| CSM Support                              |          | [Disabled]                 |      |                                                                                                                                                                                                                                                                 |             |
| Boot Option Filter                       |          | [UEFI Only]                |      |                                                                                                                                                                                                                                                                 |             |
| Boot Option Priorities                   |          |                            |      |                                                                                                                                                                                                                                                                 |             |
| Boot Option #1                           |          | [UEFI: Built-in EFI Shell] |      |                                                                                                                                                                                                                                                                 |             |
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| Feature                  | Option                                    | Description                                                                                                                                                                                              |
|--------------------------|-------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Full Screen LOGO Display | [Disabled],<br>[Enabled]                  | Select whether to enable or disable to display logo screen.                                                                                                                                              |
| Setup Prompt Timeout     | Value Input                               | Number of seconds to wait for setup activation key.<br>65535(0xFFFF) means indefinite waiting.                                                                                                           |
| Bootup NumLock State     | [On],<br>[Off]                            | This field indicates the state of the NumLock feature of the keyboard after Startup.<br>[On]: The keys on the keypad will act as numeric keys.<br>[Off]: The keys on the keypad will act as cursor keys. |
| CSM Support              | [Disabled]                                | Read only item                                                                                                                                                                                           |
| Boot Option Filter       | [UEFI only]                               | Read only item                                                                                                                                                                                           |
| Boot Option #1           | [UEFI: Built-in EFI Shell],<br>[Disabled] | Select an option for first boot device.                                                                                                                                                                  |

## 8.2.5. Security Setup Menu

The Security setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive. The 3.5"-SBC-TGL provides no factory-set passwords.

### NOTICE

If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing <RETURN>. To set a password, enter it twice and acknowledge by pressing <RETURN>.

Figure 62: BIOS Security Setup Menu

| BIOS SETUP UTILITY                                                                                                                                                |          |       |      |                        |             |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-------|------|------------------------|-------------|
| Main                                                                                                                                                              | Advanced | Power | Boot | Security               | Save & Exit |
| Password Description                                                                                                                                              |          |       |      |                        |             |
| If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup                                      |          |       |      |                        |             |
| If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights |          |       |      |                        |             |
| The password length must be in the following range:                                                                                                               |          |       |      |                        |             |
| Minimum Length                                                                                                                                                    |          | 3     |      |                        |             |
| Maximum length                                                                                                                                                    |          | 20    |      | → ←: Select Screen     |             |
| Administrator Password                                                                                                                                            |          |       |      | ↑ ↓ : Select Item      |             |
| User Password                                                                                                                                                     |          |       |      | Enter: Select          |             |
| > Secure Boot                                                                                                                                                     |          |       |      | +/-: Change Opt.       |             |
|                                                                                                                                                                   |          |       |      | F1: General Help       |             |
|                                                                                                                                                                   |          |       |      | F2: Previous Values    |             |
|                                                                                                                                                                   |          |       |      | F3: Optimized Defaults |             |
|                                                                                                                                                                   |          |       |      | F4: Save & Exit        |             |
|                                                                                                                                                                   |          |       |      | ESC: Exit              |             |
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| Feature                | Description                |
|------------------------|----------------------------|
| Administrator Password | Set administrator password |
| User Password          | Set user password          |



If only the administrator's password is set, then only access to setup is limited. The password is only entered when entering setup.

If only the user's password is set, then the password is a power on password and must be entered to boot or enter setup. Within the setup menu the user has administrator rights.

Password length requirements are maximum 20 characters and minimum 3 characters.

Figure 63: BIOS Security Setup Menu – Secure Boot

| BIOS SETUP UTILITY                       |          |                          |      |                                                                                                                                                                                  |             |
|------------------------------------------|----------|--------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Main                                     | Advanced | Power                    | Boot | Security                                                                                                                                                                         | Save & Exit |
| System Mode                              |          | Setup                    |      |                                                                                                                                                                                  |             |
| Secure Boot                              |          | [Disabled]<br>Not Active |      | → ←: Select Screen<br>↑ ↓: Select Item<br>Enter: Select<br>+/-: Change Opt.<br>F1: General Help<br>F2: Previous Values<br>F3: Optimized Defaults<br>F4: Save & Exit<br>ESC: Exit |             |
| Secure Boot Mode                         |          | [Standard]               |      |                                                                                                                                                                                  |             |
| > Restore Factory Keys*                  |          |                          |      |                                                                                                                                                                                  |             |
| > Reset To Setup Mode*                   |          |                          |      |                                                                                                                                                                                  |             |
| > Key Management*                        |          |                          |      |                                                                                                                                                                                  |             |
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\*These items are selectable only when selecting Custom for Secure Boot Mode.

| Feature              | Option                   | Description                                                                                                                                                            |
|----------------------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Secure Boot          | [Disabled],<br>[Enabled] | Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset.        |
| Secure Boot Mode     | [Standard],<br>[Custom]  | Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication. |
| Restore Factory Keys | [Yes],<br>[No]           | Force System to User Mode.<br>Install factory default Secure Boot key databases.                                                                                       |
| Reset to Setup Mode  | [Yes],<br>[No]           | Delete all Secure Boot key databases from NVRAM.                                                                                                                       |

Figure 64: BIOS Security Setup Menu – Secure Boot – Key Management

| BIOS SETUP UTILITY                       |          |            |      |                    |                        |
|------------------------------------------|----------|------------|------|--------------------|------------------------|
| Main                                     | Advanced | Power      | Boot | Security           | Save & Exit            |
| Vendor Keys                              |          | Valid      |      |                    |                        |
| Factory Key Provision                    |          | [Disabled] |      |                    |                        |
| > Restore Factory Keys                   |          |            |      |                    |                        |
| > Reset To Setup Mode                    |          |            |      |                    |                        |
| > Export Secure Boot variables           |          |            |      |                    |                        |
| > Enroll Efi Image                       |          |            |      |                    |                        |
| Device Guard Ready                       |          |            |      |                    |                        |
| > Remove 'UEFI CA' from DB               |          |            |      |                    |                        |
| > Restore DB defaults                    |          |            |      | → ←: Select Screen |                        |
|                                          |          |            |      | ↑ ↓: Select Item   |                        |
| Secure Boot variable                     |          | Size       | Keys | Key Source         | Enter: Select          |
| > Platform Key (PK)                      |          | 862        | 1    | Test (AMI)         | +/-: Change Opt.       |
| > Key Exchange Keys                      |          | 1560       | 1    | Factory            | F1: General Help       |
| > Authorized Signatures                  |          | 3143       | 2    | Factory            | F2: Previous Values    |
| > Forbidden Signatures                   |          | 3724       | 77   | Factory            | F3: Optimized Defaults |
| > Authorized TimeStamps                  |          | 0          | 0    | No Keys            | F4: Save & Exit        |
| > OsRecovery Signatures                  |          | 0          | 0    | No Keys            | ESC: Exit              |
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| Feature                      | Option                                           | Description                                                                                                                                  |
|------------------------------|--------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| Factory Key Provision        | [Disabled],<br>[Enabled]                         | Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode.                                     |
| Reset Factory Keys           | [Yes],<br>[No]                                   | Force System to User Mode.<br>Install factory default Secure Boot key databases.                                                             |
| Reset to Setup Mode          | [Yes],<br>[No]                                   | Delete all Secure Boot key databases from NVRAM.                                                                                             |
| Export Secure Boot variables | Select a File system                             | Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device.                                               |
| Enroll Efi Image             | Select a File system                             | Allow the image to run in Secure Boot mode.<br>Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db).         |
| Remove 'UEFI CA' from DB     | [Yes],<br>[No]                                   | Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db).                               |
| Restore DB defaults          | [Yes],<br>[No]                                   | Restore DB variable to factory defaults.                                                                                                     |
| Platform Key (PK)            | [Details],<br>[Export],<br>[Update],<br>[Delete] | Enroll Factory Defaults or load certificates from a file:<br>1. Public Key Certificate:<br>(a) EFI_SIGNATURE_LIST<br>(b) EFI_CERT_X509 (DER) |

| Feature               | Option                                                        | Description                                                                                                                                                    |
|-----------------------|---------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Key Exchange Keys     | [Details],<br>[Export],<br>[Update],<br>[Append],<br>[Delete] | (c) EFI_CERT_RSA2048 (bin)<br>(d) EFI_CERT_SHAXXX<br>2. Authenticated UEFI Variable<br>3. EFI PE / COFF Image (SHA256)<br>Key Source: Factory, External, Mixed |
| Authorized Signatures | [Details],<br>[Export],<br>[Update],<br>[Append],<br>[Delete] |                                                                                                                                                                |
| Forbidden Signatures  | [Details],<br>[Export],<br>[Update],<br>[Append],<br>[Delete] |                                                                                                                                                                |
| Authorized TimeStamps | [Update],<br>[Append]                                         |                                                                                                                                                                |
| OsRecovery Signatures | [Update],<br>[Append]                                         |                                                                                                                                                                |

### 8.2.5.1. Remember the password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords results in being locked out of the system.

If the system cannot be booted because the User Password or the Supervisor Password are not know, contact Kontron Support for further assistance.



---

**HDD security passwords cannot be cleared using the above method.**

---

## 8.2.6. Save & Exit Setup Menu

The exit setup menu provides functions for handling changes made to the UEFI BIOS settings and the exiting of the setup program.

Figure 65: BIOS Save & Exit Setup Menu

| BIOS SETUP UTILITY                                                                                                                 |          |       |      |                        |             |
|------------------------------------------------------------------------------------------------------------------------------------|----------|-------|------|------------------------|-------------|
| Main                                                                                                                               | Advanced | Power | Boot | Security               | Save & Exit |
| Save Changes and Reset<br>Discard Changes and Reset<br><br>Save Options<br>Save Changes<br>Discard Changes<br><br>Restore Defaults |          |       |      |                        |             |
|                                                                                                                                    |          |       |      | → ←: Select Screen     |             |
|                                                                                                                                    |          |       |      | ↑ ↓: Select Item       |             |
|                                                                                                                                    |          |       |      | Enter: Select          |             |
|                                                                                                                                    |          |       |      | +/-: Change Opt.       |             |
|                                                                                                                                    |          |       |      | F1: General Help       |             |
|                                                                                                                                    |          |       |      | F2: Previous Values    |             |
|                                                                                                                                    |          |       |      | F3: Optimized Defaults |             |
|                                                                                                                                    |          |       |      | F4: Save & Exit        |             |
|                                                                                                                                    |          |       |      | ESC: Exit              |             |
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| Feature                   | Description                                              |
|---------------------------|----------------------------------------------------------|
| Save Changes and Reset    | Reset the system after saving the changes.               |
| Discard Changes and Reset | Reset system setup without saving any changes.           |
| Save Changes              | Save Changes done so far to any of the setup options.    |
| Discard Changes           | Discard Changes done so far to any of the setup options. |
| Restore Defaults          | Restore / Load Default values for all the setup options. |

## Appendix A: List of Acronyms



The following table does not contain the complete acronyms used in signal names, signal type definitions or similar. A description of the signals is included in the I/O Connector and Internal connector chapters within this user guide.

Table 51: List of Acronyms

|               |                                                |
|---------------|------------------------------------------------|
| <b>2D</b>     | Two-Dimensional                                |
| <b>3D</b>     | Three-Dimensional                              |
| <b>AT</b>     | Advanced Technology                            |
| <b>ATX</b>    | Advanced Technology eXtended                   |
| <b>BGA</b>    | Ball Grid Array                                |
| <b>BIOS</b>   | Basic Input / Output System                    |
| <b>BSP</b>    | Board Support Package                          |
| <b>CMOS</b>   | Complementary Metal Oxide Semiconductor        |
| <b>CPU</b>    | Central Processing Unit                        |
| <b>DC</b>     | Direct Current                                 |
| <b>DDC</b>    | Display Data Channel                           |
| <b>DIO</b>    | Digital Input / Output                         |
| <b>DP</b>     | DisplayPort                                    |
| <b>ECC</b>    | Error-Correcting Code                          |
| <b>EEE</b>    | Electrical and Electronic Equipment            |
| <b>EOS</b>    | Electrical OverStress                          |
| <b>ESD</b>    | ElectroStatic Discharge                        |
| <b>GbE</b>    | Gigabit Ethernet                               |
| <b>HDD</b>    | Hard Disk Drive                                |
| <b>HDMI</b>   | High Definition Multimedia Interface           |
| <b>LAN</b>    | Local Area Network                             |
| <b>LED</b>    | Light Emitting Device                          |
| <b>LVDS</b>   | Low-Voltage Differential Signaling             |
| <b>ME F/W</b> | Management Engine Firmware                     |
| <b>mPCIe</b>  | mini Peripheral Component Interconnect express |
| <b>NGFF</b>   | Next Generation Form Factor                    |
| <b>PC-AT</b>  | Personal Computer - Advanced Technology        |
| <b>PCB</b>    | Printed Circuit Board                          |
| <b>PSU</b>    | Power Supply Unit                              |
| <b>PVC</b>    | PolyViny Chloride                              |
| <b>PWM</b>    | Pulse Width Modulation                         |
| <b>RAM</b>    | Random Access Memory                           |
| <b>ROM</b>    | Read-Only Memory                               |

|                |                                           |
|----------------|-------------------------------------------|
| <b>RTC</b>     | Real-Time Clock                           |
| <b>SATA</b>    | Serial Advanced Technology Attachment     |
| <b>SD</b>      | Secure Digital memory card                |
| <b>SDP</b>     | Serial Download Protocol                  |
| <b>SELV</b>    | Safety Extra-Low Voltage                  |
| <b>SIM</b>     | Subscriber Identity Module                |
| <b>SMBus</b>   | System Management Bus                     |
| <b>SoC</b>     | System on Chip                            |
| <b>SO-DIMM</b> | Small Outline Dual In-line Memory Module  |
| <b>SPD</b>     | Serial Presence Detect                    |
| <b>SPI</b>     | Serial Peripheral Interface               |
| <b>TDP</b>     | Thermal Design Power                      |
| <b>TPM</b>     | Trusted Platform Module                   |
| <b>UEFI</b>    | Unified Extensible Firmware Interface     |
| <b>USB</b>     | Universal Serial Bus                      |
| <b>UTP</b>     | Update Transfer Protocol                  |
| <b>VGA</b>     | Video Graphics Array                      |
| <b>WDT</b>     | WatchDog Timer                            |
| <b>WEEE</b>    | Waste Electrical and Electronic Equipment |
|                |                                           |
|                |                                           |
|                |                                           |
|                |                                           |
|                |                                           |



## About Kontron

Kontron is a global leader in IoT / Embedded Computing Technology (ECT) and offers individual solutions in the areas of Internet of Things (IoT) and Industry 4.0 through a combined portfolio of hardware, software and services. With its standard and customized products based on highly reliable state-of-the-art technologies, Kontron provides secure and innovative applications for a wide variety of industries. As a result, customers benefit from accelerated time-to-market, lower total cost of ownership, extended product lifecycles and the best fully integrated applications.

For more information, please visit: [www.kontron.com](http://www.kontron.com)

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