Modular Computers ®

CP600/CP610

Double-Height System CPU Board for CompactPCI Systems

Manual ID 18940, Rev. Index 0300
May 00

The product described in this manual is in compliance with all applied CE standards.

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Revision History				
Manual/Product Title:	**CP600/CP610**			
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Explanation of Symbols

CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please see also the section “Applied Standards” in this manual.

Caution!

This symbol and title warn you of hazards due to electrical shocks (> 60 V) when touching products or parts of them. Failure to observe the necessary precautions as described and/or prescribed by the law may result in damage to your product and/or endanger your life/health.

Please see also the section “High Voltage Safety Instructions”.

ESD-Sensitive Device!

This symbol and title highlight the fact that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following pageof this manual.

Attention!

This symbol and title emphasize aspects which, if not understood and taken into consideration by the reader, may result in hazards to health and/or material damage.

Note:

This symbol and title relate to information the user should read through carefully for his or her own advantage.

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This symbol and title accompany information highlighting positive aspects of a *PEP* product and/or procedure.

Troubleshooting

This symbol and title accompany information about troubleshooting and problem solving.

For your safety

Your new *PEP* product has been developed and carefully tested in order to provide all the features necessary to ensure full compliance with all electrical safety requirements. It has also been designed for a long fault-free life. However, the life expectancy of your product will be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interests of your own safety and of the correct operation of your new *PEP* product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

Warning!

All operations on this device must be carried out by sufficiently skilled personnel.

Caution!

The power supply must always be disconnected before installation, repair and maintenance operations are carried out on this product. Failure to comply with this basic precaution will subject the operator to serious electrical shock hazards. Always unplug the power cable before such operations.
Before installing your new *PEP* product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Special Handling and Unpacking Instructions

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Care must therefore be exercised at all times during handling and inspection of the board, in order to ensure product integrity.

- Do not handle this product while it is outside its protective enclosure while it is not used for operational purposes, unless it is otherwise protected.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where safe work stations are not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or tracks on the board.

General Instructions on Usage

- In order to maintain *PEP's* product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by *PEP Modular Computers* and described in this manual or received from *PEP* Technical Support as a special handling instruction, will void your warranty.
- This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.
- In performing all necessary installation and application operations, please, follow only the instructions supplied by the present manual.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.
- Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instructions on the previous page of this manual.

Two Year Warranty

PEP Modular Computers grants the original purchaser of a *PEP* product a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of *PEP* are valid unless the customer has the express written consent of *PEP Modular Computers*.

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If the customer's eligibility for warranty has not been voided he should, in the event of any claim, return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application in which the product has been used and a description of the defect. Please pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

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1. Introduction

1.1 Introduction to CompactPCI

The *PEP Modular Computers* CompactPCI product described in this chapter operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the homepage of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system-relevant CompactPCI features that are specific to *PEP Modular Computers* CompactPCI systems may be found described in the *PEP* CompactPCI System Manual. Due to its size, this manual cannot be downloaded via the internet. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All necessary information to combine *PEP Modular Computers* racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of *PEP Modular Computers* CompactPCI boards, such as functionality, hotswap capability. In addition, an overview is given for all existing *PEP Modular Computers* CompactPCI boards with links to the relating datasheets.
- Generic information on the *PEP Modular Computers* CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the *PEP Modular Computers* CompactPCI standard backplane family.
- Generic information on the *PEP Modular Computers* CompactPCI power supply units, such as the input/output characteristics, redundant operation and distinctive features, as well as an overview of the *PEP Modular Computers* CompactPCI standard power supply unit family.

1.2 *PEP* Double-height CPU Boards

The *PEP* range of double-height 6U CompactPCI CPU boards based on Socket-7 processors has been designed to meet the needs of users in a wide range of applications, while maintaining an identical software environment.

The CP610 is a system controller which controls three PCI buses comprising one local and two external CompactPCI buses (P1/P2 and P4/P5). The on-board PCI bus supports a Fast Ethernet port and one PMC slot. The VGA interface is integrated in the Chipset. To achieve a high CPU and memory performance the board includes 512kB L2 Cache. DRAM comes as 32MB or 64 MB soldered with additional SODIMM providing up to 320MB of main memory. All standard PC interfaces are implemented and assigned to the front panel and to the rear connector P3.

The CP600 is a system controller which is identical to the CP610 in every respect except that it does not have the second CompactPCI interface on P4/P5 and P3 is available as an option.

The CP611 is a non-system controller which is the same as the CP600 but has a different PCI/PCI (non-transparent) bridge at P1/P2. This makes possible additional CP611's together with a system controller CPU on one CompactPCI bus, i.e. multiprocessing.

The CP612 is a special controller. On the CompactPCI interface on P1/P2 there is a non transparent bridge implemented, as on the CP611. However, on the second CompactPCI interface on P4/P5 the CP612 controls an additional independent CompactPCI bus as a system controller.

Table 1-1: Comparison between the CP600, CP610, CP611 and CP612

Feature	CP600	CP610	CP611	CP612
System Controller CPU 32-bit	P1/P2	P1/P2 P4/P5	--	P4/P5
Max. 3U CompactPCI peripheral slots	7	14	--	7
Non-transparent PCI/PCI bridge	No	No	P1/P2	P1/P2
Rear I/O via P3	Optional	Yes	Optional	Optional

1.3 Board Introduction

The CP600/CP610 is a CompactPCI Pentium-based single-board computer specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the CP600/CP610's outstanding features are:

- compliance with CompactPCI Interface 2.1
- optional one/two independent CompactPCI interfaces
- suitable for all common socket-7 processors for standard PC applications
- max. 512 kB CPU L2 cache
- up to 320 MB main memory
- 256 kB FLASH for BIOS
- on-board SVGA
- Flash Disk up to 144 MB
- two IDE interfaces
- Fast Ethernet: 10BaseT & 100BaseTX

The CP600/CP610 includes the following commonly used peripheral devices:

- floppy disk interface
- keyboard/USB controller
- serial I/O (ESD protected)
- counter/timers
- watchdog timer
- real-time clock
- double-width version with three serial ports and an additional parallel port on additional transition module
- rear I/O at P3
- PMC Interface and break-out on front panel
- hotswap compliant

1.4 Product Overview

The CP600/610 is a highly integrated single-board computer that is designed around the Pentium family of Intel and K6 of AMD microprocessors. The CP600 is equipped with one CompactPCI interface while the CP610 is distinguished by offering two CompactPCI interfaces enabling the user to select the model most suited to operational requirements.The CP612 is a system controller on the CompactPCI interface P4/P5 and a peripheral controller on the P1/P2.

Finding an optimum equilibrium between performance and power dissipation, the CP600/CP610 is a reliable Pentium-controlled board supporting a clock speed of 400 MHz.

Designed for stability and produced in a rugged format, the board has been developed to operate in all applications situated in industrial environments. The low power feature of the board is further assured through the use of 3.3 V technology for support of the latest 64 Mbit DRAM components.

The CPU is compatible with the operating system Microsoft Windows NT®. However, the performance of CompactPCI can be tuned to suit real-time applications and operating systems like VxWorks or QNX which are instrumental to the success of CompactPCI in these market sectors.

For industrial applications, a solid mechanical configuration requires easy access to the main module interfaces. Therefore, all critical user I/O's (keyboard, USB, VGA, Ethernet and COM1) are routed to the front panel. The remaining two IDE hard-disk interfaces and one floppy-disk interface are provided as on-board pin-row connectors.

1.5 Special Features of the CP600/CP610

Watchdog Timer

The CP600/CP610 is equipped with a watchdog timer with a programmable timeout ranging from 125 msec. to 250 sec.

Interrupts

Two enhanced 8259 style interrupt controllers provide a total of fifteen interrupt inputs with features which include: level and edge triggered inputs, fixed and rotating priorities and individual input masking. Interrupt sources include: Counter/timers, serial I/O, RTC, keyboard/mouse, printer, floppy-disk, IDE interfaces and four interrupt sources on the CompactPCI backplane.

Reset

The CP600/CP610 is automatically reset in the event of power supply problems. Other reset sources include the watchdog timer and local push-button switch.

Note:

For more detailed information about these features please see section 2.7.2 and under section 2.9.4 in chapter 2, Functional Description and Configuration.

1.6 Optional Modules for Expanded Capability

1.6.1 Transition Module

A double-width version of the CP600/CP610 including a special transition module is available. This version of the CP600/CP610 CPU board differs from the single-width version in that the double-width front panel is provided with three additional serial interfaces and a parallel port. Front panel LED's and interfaces characterize the CP600/CP610 board as a whole and are described in detail in the next chapter. The jumper settings and pinouts of the transition module are also described under separate headings in chapter 2, "Functional Description and Configuration".

Note:

The transition module is used only with the double-width version of the CP600/CP610.

1.6.2 Hard-Disk/Flash Disk Module

A double-width version of the CP600/CP610 including an adapter module allowing connection of a 2.5" hard-disk is available and may be mounted in addition to the transition module. The hard-disk itself has to be mounted directly onto the adapter module.

Optionally, instead of the hard-disk, a 1.8" flash disk may be mounted on the module.

Note:

The hard-disk/flash disk module can only be used with the double-width version of the CP600/CP610.

1.6.3 Rear I/O Module

All 6U CPU boards provided with a P3 rear I/O connector can be upgraded with the rear I/O module CP-RIO6-10 which must be inserted from the back of the system. It is plugged into the backplane CompactPCI connector P3 which is in line with the CPU board.

If a rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interfaces. Thus, the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

Note:

For the specifications of the rear I/O module, please see chapter 4, "Rear I/O Module".

1.7 Main Specifications

Table 1-2: CP600/CP610 Main Specifications

CP600/CP610	Specifications
CPU	All common socket-7 processors up to 400 MHz Built-in numeric co-processor support.
Memory	• 32 kB or 64 kB internal CPU cache (processor) • 512 kB burst-SRAM pipelined L2 expansion cache • 64 MB on-board DRAM expandable to 320 MB SODIMM socket for 256 MB EDO and SDRAM
Pentium System Controller	SiS 5598 single-chip PCI set with: • Level 2 write-back cache controller, Burst DRAM controller, PCI & ISA interface, consuming only 1PCI load • Real-time clock with general purpose, battery-backed CMOS RAM, s/w compatible with DS1287/MC146818 • Two enhanced 8237-style DMA controllers • 8042 compatible PC/AT keyboard controller
AT Peripheral Controller	Two SMC FDC37C669's provide the following functions: • Four 16C550 compatible UART's with 16 bytes FIFO. • Multi-mode, bi-directional parallel port, IBM CENTRONICS compatible. Enhanced parallel Port (EPP), high speed mode: ECP compatible
Mass Storage Interfaces	Floppy-disk interface for up to 2 devices: • 720 kB, 1.2/1.44 or 2.88 MB • 2 IDE/ATA interfaces each supporting ultra DMA protocol for 2 hard-disks or CD-ROM on 40-pin 2.54mm connectors • 144 MB FLASH Disk-on-Chip
Real-Time Features	Software configured watchdog timer that can be BIOS configured to issue an IRQ, NMI or system reset
SVGA Video Support	High performance, embedded 64-bit GUI accelerator with shared display memory (4 MB) for screen resolutions up to 1024 768 pixels for both interlaced and non-interlaced operational modes
Software Support	• Award BIOS contained within 256 kB of Flash memory. • Real-time operating systems: Windows NT, QNX, VxWorks etc. • PC operating systems technically possible: MS-DOS, Windows 95, OS-2, UNIX.
CompactPCI Bus Interface	Conforms with CompactPCI Specification V 2.0, Rev. 2.1 32-bit master interface CP600: one CPCI interface at P1/P2 CP610: two CPCI interfaces at P1/P2 and P4/P5 3.3V/5.0V compatible

Table 1-2: CP600/CP610 Main Specifications

CP600/CP610	Specifications
General	Power consumption (AMD K6, 300 MHz): • 3.3 V: 4W • 5.0 V: 12W • 12.0 V: 1W approx. (fan version only) Dimensions: 233.35mm*160mm (6U card size) Temperatures • Operating: 0°C to +60°C • Extended: -25°C to +75°C • Storage: -55°C to +85°C Operating humidity: 0% to 95% non-condensing Weight: • 4HP: 400g • 8HP: 600g
Front Panel Interfaces	PS2 keyboard/mouse connector COM1 mouse/serial port with 9-pin D-Sub COM2-COM4 serial port with 9-pin D-Sub (8HP version) Twin USB Interfaces Fast Ethernet on RJ45 connector 15-pin D-Sub SVGA connector LPT physical interface on 25-pin D-Sub (8HP version) Board RESET button PMC slot
LED's (4 HP and 8HP version)	Board LED's: • Yellow ("W"): Watchdog timer status, • Red ("T"): Temperature alarm. Ethernet LED's (green): • Left: Active, • Middle: Link, • Right: Speed.
Fast Ethernet Interface	Controller: Intel 82558 Fast Ethernet controller Data Rate: 10 & 100 Mbit/s Ethernet Int.: Full 802.2 & 802.3 IEEE compliance supporting both 10Base-T & 100Base-TX Cabling: Category 5 two-pair cabling
Rear I/O Interface	Compatible with Dual System Slot Specification Draft 0.4 with two Independent IDE interfaces
Hotswap Compatible	The CP600/CP610 supports other boards which may be removed or added with power on. Individual clocks for each slot and Enum signal handling are in compliance with the PCIMG 2.1 Hotswap specification.

Table 1-2: CP600/CP610 Main Specifications

CP600/CP610	Specifications
PMC Interface	Complies with single CMC specification IEEEP1386 32-bit master interface 5.0V compatible
Common Features	DC power monitors (3.3V and 5V) Battery socket and 3.0V lithium battery for RTC: • VARTA Type CR2025 • PANASONIC BR2020 LM75 temperature sensor

1.8 Applied Standards

1.8.1 CE Compliance

The *PEP Modular Computers'* CompactPCI systems comply with the requirements of the following CE-relevant standards:

- Emission EN50081-1
- Immission EN50082-2
- Electrical Safety EN60950

1.8.2 Mechanical Compliance

- Mechanical Dimensions IEEE 1101.10

1.8.3 Environmental Tests

- Vibration/Broadband Random Vibration IEC68-2-6 IEC68-2-64 (3U boards)
- Permanent Shock IEC68-2-29
- Single Shock IEC68-2-27

1.9 Related Publications

1.9.1 CompactPCI Systems/Boards

- CompactPCI Specification, V. 2.0, Rev. 3.0

Chapter 2

Functional Description and Configuration

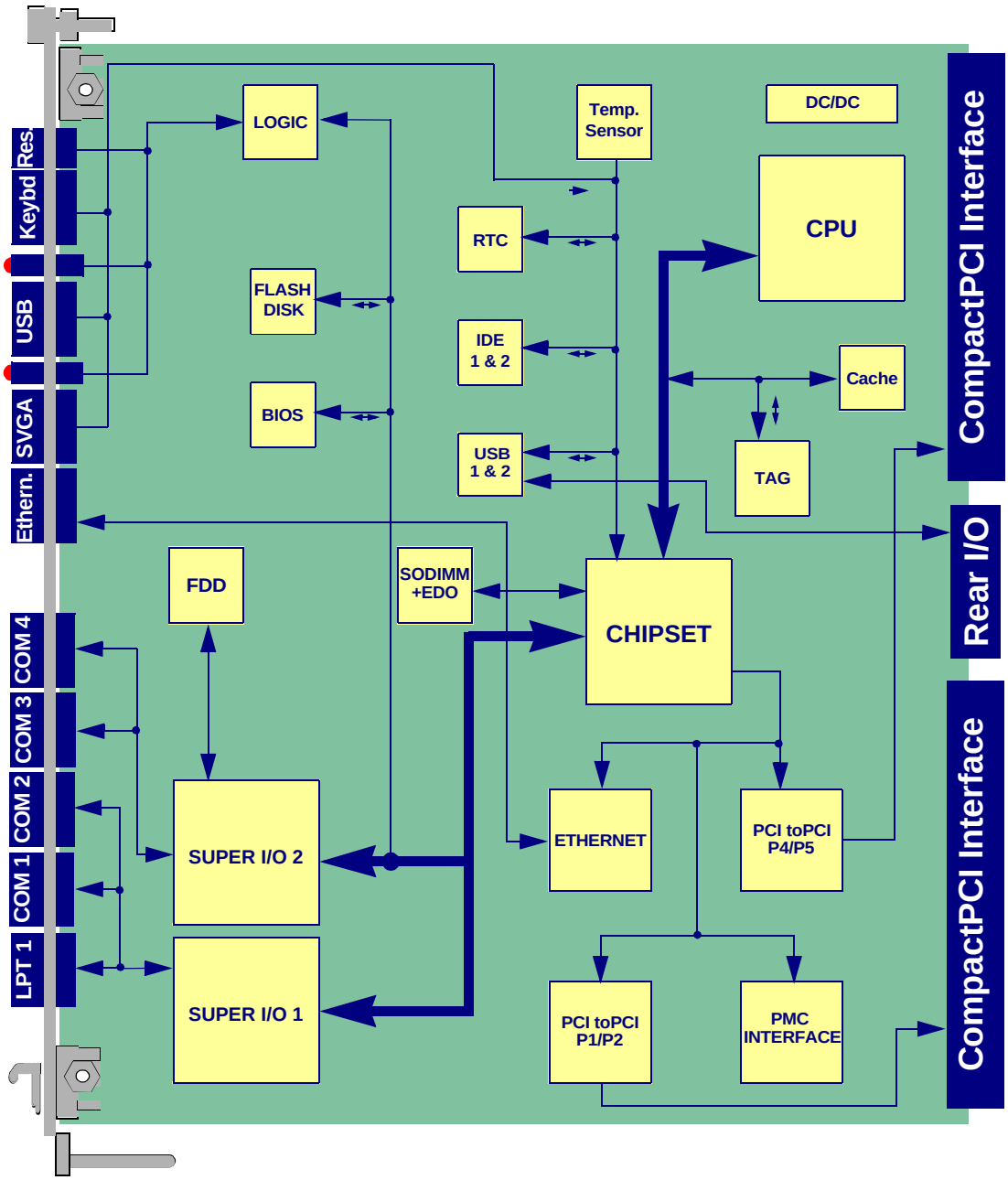
Functional Description and Configuration

Functional Description and Configuration

2. Functional Description and Configuration

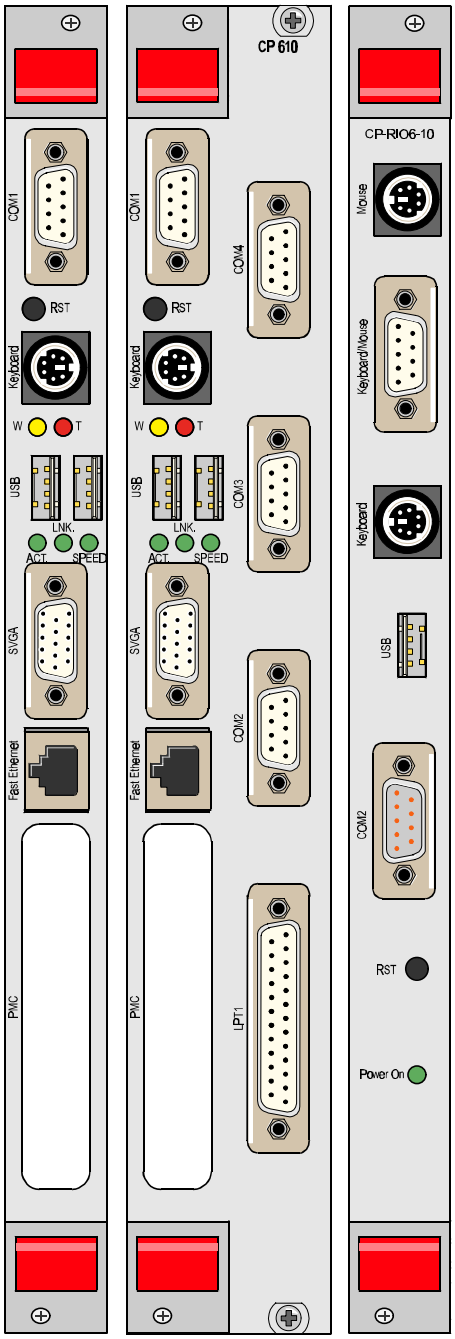
2.1 CP600/CP610 Functional Block Diagram

Figure 2-1: CP600/610 Functional Block Diagram



2.2 Front Panels

Figure 2-2: Front Panel View of a CP600/CP610: Single-Width Version (Left), Double-Width Version (Center) and Rear I/O Module (Right)



The front panels of both the single-width and double-width versions include two LED's placed under the keyboard/mouse interface connector ("Board LED's") and three LED's placed under the USB connector ("Ethernet LED's"). The functions of the LED's are as follows:-

Board LED's:

- "W" (yellow) = Watchdog timer status; if ON, the watchdog is active.
- "T" (red) = Temperature alarm; if ON, an overtemperature has occurred. To rectify, reduce the CPU clock speed.

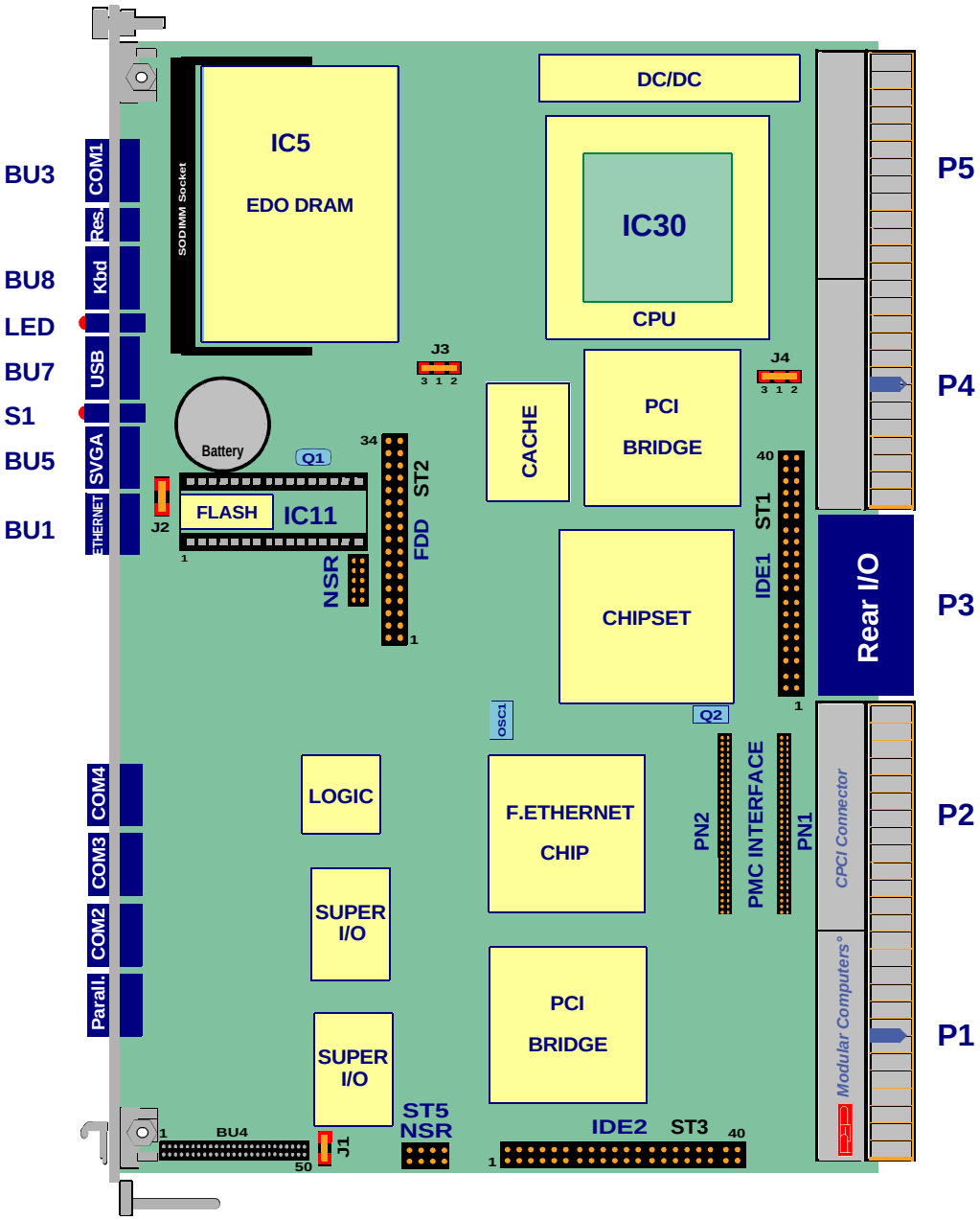
Ethernet LED's (green):

- Left = Active; if ON, the Ethernet link is active.
- Middle = Link; if ON, transmission is in progress via the Ethernet link.
- Right = Speed; if ON transmission speed is 100 MBit/s.

2.3 Board Layouts

2.3.1 CP600/CP610 Baseboard

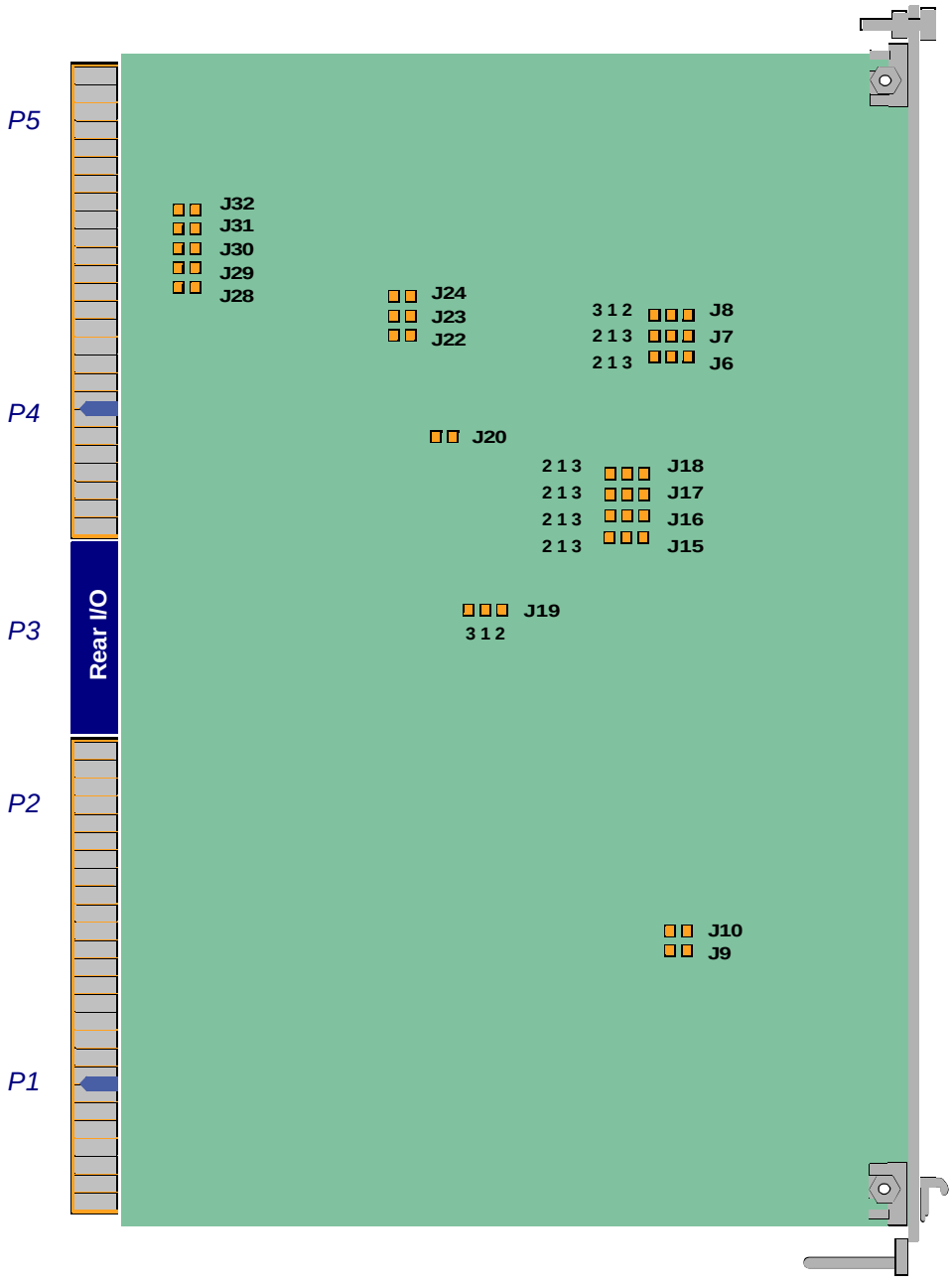
Figure 2-3: CP600/CP610 Board Layout (Front Side of Single-Width Version)



Legend:

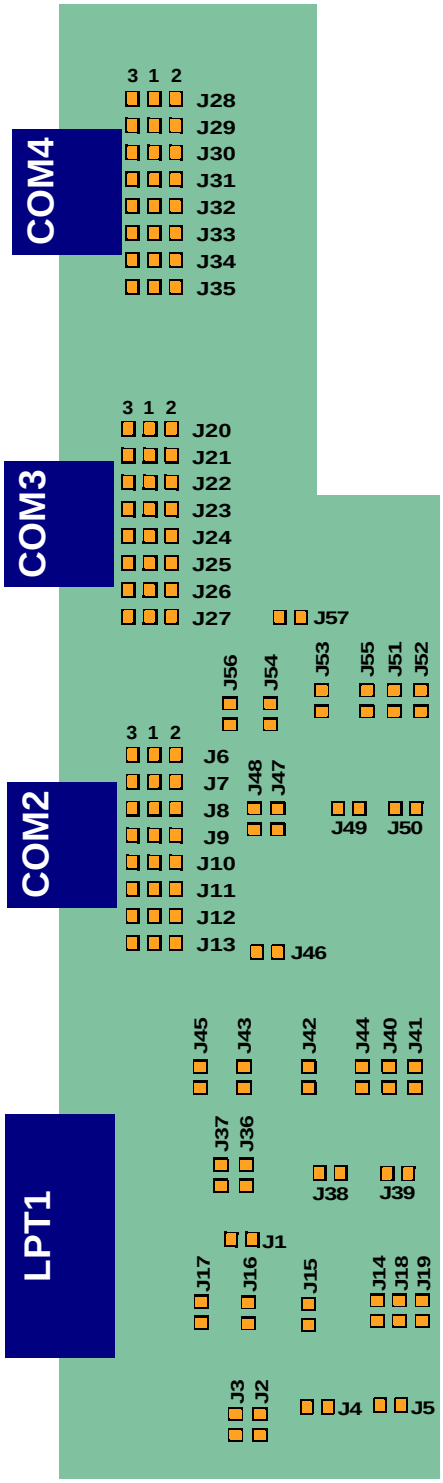
NSR = Not System Relevant

Figure 2-4: CP600/CP610 Board Layout (Reverse Side)



2.3.2 Transition Module TR1

Figure 2-5: Transition Module TR1 Layout



2.4 Baseboard Main Features

The following sections describe the main features of the principal functional blocks of the CP600/CP610 and include, where relevant, jumper settings and pinouts.

2.4.1 CPU

The CP600/CP610 supports the Pentium processor family:

- P54C, P55C, up to 233 MHz;
- Intel VRT with 133 MHz;
- AMD K6 up to 400 MHz

Principally, the CP600/CP610 controller board is designed for all socket-7 processors. The CPU frequency may be determined by setting the frequency ratio and system frequency which are in the following relationship with one another:

CPU frequency = frequency ratio x system frequency

2.4.1.1 System Frequency

The table below shows the solder jumper settings for the different CPU and PCI-synchronous speed configurations.

Table 2-1: Jumper Settings for Different CPU and PCI Frequency Configurations

J18	J17	J16	J15	CPU Clock	PCI Clock	Notes
Open, 1-3	Closed, 1-2	Closed, 1-2	Closed, 1-2	33.3MHz	16.7MHz	PCI synchronous
Open, 1-3	Open, 1-3	Closed, 1-2	Closed, 1-2	50.0MHz	25.0MHz	PCI synchronous
Open, 1-3	Closed, 1-2	Open, 1-3	Closed, 1-2	55.0MHz	27.0MHz	PCI synchronous
Open, 1-3	Open, 1-3	Open, 1-3	Closed, 1-2	60.0MHz	30.0MHz	PCI synchronous
Open, 1-3	*Open, 1-3*	*Closed, 1-2*	*Open, 1-3*	*66.6MHz*	*33.3MHz*	*PCI synchronous*

The default setting is indicated by italics.

2.4.1.2 CPU-to-Bus Frequency Ratio

These three solder jumpers are used in combination to decide the ratio of the internal frequency of the CPU to the bus clock.

Table 2-2: Jumper Settings for CPU-to-Bus Frequency Ratio

J24 (BF2)	J23 (BF1)	J22 (BF0)	Intel Pentium P54C	Intel Pentium MMX P55C	AMD K6
Closed	Closed	Closed	N/A	N/A	4.5x
Closed	Closed	Open	N/A	N/A	5.0x
Closed	Open	Closed	N/A	N/A	4.0x
Closed	Open	Open	N/A	N/A	5.5x
Open	Closed	Closed	2.5x	2.5x	2.5x
Open	Closed	Open	3.0x	3.0x	3.0x
Open	Open	Closed	2.0x	2.0x	2.0x
Open	Open	Open	1.5x	3.5x	3.5x

2.4.1.3 CPU Voltage Selection

The core voltage must be configured for every CPU type. The voltage is digitally programmable from 1.3V to 3.3V.

J32	J31	J30	J29	J28	Core Voltage	CPU
Open	Closed	Open	Closed	Closed	3.3V	--
Open	Closed	Open	Closed	Open	3.2V	--
Open	Closed	Closed	Open	Closed	3.1V	--
Open	Closed	Closed	Open	Open	3.0V	--
Open	Closed	Open	Open	Closed	2.9V	Intel Pentium VRT 133 MHz
Open	*Closed*	*Open*	*Open*	*Open*	*2.8V*	*Intel Pentium P55C 133 MHz-233 MHz*
Open	Open	Closed	Closed	Closed	2.7V	--
Open	Open	Closed	Closed	Open	2.6V	--
Open	Open	Open	Closed	Closed	2.5V	--
Open	Open	Open	Closed	Open	2.4V	--
Open	Open	Closed	Open	Closed	2.3V	--
Open	Open	Closed	Open	Open	2.2V	AMD K6 266 MHz-400 MHz
Open	Open	Open	Open	Closed	2.1V	--
Closed	Closed	Closed	Closed	Open	2.0V	AMD K6 266 MHz Mobile
Open	Open	Open	Open	Open	OFF	Intel Pentium P54C 100 MHz-200 MHz Core Voltage = I/O Voltage
Closed	Closed	Closed	Closed	Open	2.0V	--
Closed	Closed	Open	Closed	Closed	1.9V	--
Closed	Closed	Closed	Open	Open	1.8V	--
Closed	Closed	Open	Open	Open	1.7V	--
Closed	Open	Closed	Closed	Open	1.6V	--
Closed	Open	Open	Closed	Open	1.5V	--
Closed	Open	Closed	Open	Open	1.4V	--
Closed	Open	Open	Open	Open	1.3V	--

The default setting is indicated by italics.

2.4.2 Memory

The CP600/CP610 can accommodate 32 MB or 64 MB of 64-bit DRAM which are soldered in place for optimum mechanical stability. In addition, up to 256 MB DRAM EDO or SDRAM are installed on a SODIMM socket. Up to 144 MB memory is available in the on-board FLASH on a DIL socket.

2.4.2.1 Memory Configuration

The integrated VGA controller can only share the DRAM bank “0”. To achieve a high system performance it is recommended to use SDRAM memory for the VGA controller. The following solder jumpers select the DRAM type for the integrated VGA

Table 2-3: Jumpers J8/J7/J6 — DRAM Type Selection

J8	J7	J6	On-board EDO	SODIMM EDO	SODIMM SDRAM	Note
1-2	*1-2*	*1-2*	*32/64 MB bank “0”*	--	--	--
1-2	*1-2*	*1-2*	*32 MB or 64 MB bank0*	*£ 128 MB*	--	--
1-3	1-3	1-3	32 MB or 64 MB	--	≤ 256 MB Bank “0”	Recommended for integrated VGA

The default setting is indicated by italics.

2.4.3 Standard Peripherals

The following standard peripherals are available on the CP600/CP610 board:

- *Real-Time Clock*

  The real-time clock performs time keeping functions and includes 256 bytes of general purpose battery-backed CMOS RAM. Features include an alarm function, programmable periodic interrupt and a 100-year calendar.

- *Counter/Timer*

  Three 8254-style counter/timers are included on the CP600/CP610 as defined for the PC/AT.

2.5 Baseboard Interfaces with Jumper Settings and Pinouts

2.5.1 Overview of Connector Names and Functions

The following table shows the function of each main board connector/socket.

Table 2-4: Connector Names and Functions

Connector Name	Function
IC30	CPU socket
IC5	SODIMM socket 144 pins 3.3V EDO or SDRAM
BU3	Serial port COM1
BU5	VGA interface
BU8	Keyboard/mouse PS/2
BU7	USB
BU1	Ethernet
J1, S1	External reset
BU4	Transition module
ST2	Floppy-disk drive
ST1 = IDE1 ST3=IDE2	IDE interface
CP600: P1-P2 CP610: P1-P5 P3 is optional for all variants	CompactPCI
PN1, PN2	PMC
IC11	Flash socket 600mil DIL

The default setting is indicated by italics.

2.5.2 CompactPCI Bus Interface(s)

The CP600 has one and the CP610 two CompactPCI interfaces.

The CP600/CP610 can operate as a system controller for 32-bit CompactPCI systems which are electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

2.5.2.1 CompactPCI Bus Connectors' Pinouts

The CP600 is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, P1 and P2. The CP610 is provided with two additional CompactPCI bus connectors, P4 and P5. The pinouts of P1 and P4 are identical, as are the pinouts of P2 and P5 and they are thus combined in the same tables as follows:-

Table 2-5: CompactPCI Bus Connectors P1 and P4 Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
25	5V	REQ64#	ENUM#	3.3V	5V	GND
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	3.3V	IPMB SCL	IPMB SDA	GND	PERR#	GND
16	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	3.3V	FRAME#	IRDY#	BD SEL#	TRDY#	GND
12-14	Key Area					
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ#	GND	3.3V	CLK	AD[31]	GND
5	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	IPMB PWR	HEALTHY#	V(I/O)	INTP	INTS	GND
3	INTA#	INTB#	INTC#	5V	INTD#	GND
2	TCK	5V	TMS	TDO	TDI	GND
1	5V	-12V	TRST#	+12V	5V	GND

Note: a "#" symbol after a symbol name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven to a low level.

Table 2-6: CompactPCI Bus Connectors P2 and P5

Pin	Row A	Row B	Row C	Row D	Row E	Row F
22	N/C	N/C	N/C	N/C	N/C	GND
21	N/C	GND	N/C	N/C	N/C	GND
20	N/C	GND	N/C	GND	N/C	GND
19	GND	GND	N/C	N/C	N/C	GND
18	N/C	N/C	N/C	GND	N/C	GND
17	N/C	GND	PRST#	REQ6#	GNT6#	GND
16	N/C	N/C	DEG#	GND	GND	GND
15	N/C	GND	FAL#	REQ5#	GNT5#	GND
14	N/C	N/C	N/C	GND	N/C	GND
13	N/C	GND	V(I/O)	N/C	N/C	GND
12	N/C	N/C	N/C	GND	N/C	GND
11	N/C	GND	V(I/O)	N/C	N/C	GND
10	N/C	N/C	N/C	GND	N/C	GND
9	N/C	GND	V(I/O)	N/C	N/C	GND
8	N/C	N/C	N/C	GND	N/C	GND
7	N/C	GND	V(I/O)	N/C	N/C	GND
6	N/C	N/C	N/C	GND	N/C	GND
5	N/C	GND	V(I/O)	N/C	N/C	GND
4	V(I/O)	N/C	N/C	GND	N/C	GND
3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	CLK2	CLK3	N/C	GNT2#	REQ3#	GND
1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Note: a "#" symbol after a symbol name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven to a low level.

2.5.3 PMC Interface

For flexible and easy configuration one on-board PMC socket is available. The PN1 and PN2 connectors provide the signals for the 32-bit PCI Bus. The 64-bit interface for the PMC interface is not implemented. User defined I/O signals are not supported.

The interface has been designed to comply with the IEEEP1386.1 specification which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor. It supports only 5V Rear I/O.

2.5.3.1 PMC Connectors PN1 and PN2 Pinout

Table 2-7: PMC Connector Pin Assignments

PN1/JN1				PN2/JN2			
Pin #	**Signal Name**	**Signal Name**	**Pin #**	**Pin #**	**Signal Name**	**Signal Name**	**Pin #**
1	Signal	-12V	2	1	+12V	Signal	2
3	Ground	Signal	4	3	Signal	Signal	4
5	Signal	Signal	6	5	Signal	Ground	6
7	BUSMODE1#	+5V	8	7	Ground	Signal	8
9	Signal	Signal	10	9	Signal	Signal	10
11	Ground	Signal	12	11	BUSMODE2#	+3.3V	12
13	Signal	Ground	14	13	Signal	BUSMODE3#	14
15	Ground	Signal	16	15	+3.3V	BUSMODE4#	16
17	Signal	+5V	18	17	Signal	Ground	18
19	V (I/O)	Signal	20	19	Signal	Signal	20
21	Signal	Signal	22	21	Ground	Signal	22
23	Signal	Ground	24	23	Signal	+3.3V	24
25	Ground	Signal	26	25	Signal	Signal	26
27	Signal	Signal	28	27	+3.3V	Signal	28
29	Signal	+5V	30	29	Signal	Ground	30
31	V (I/O)	Signal	32	31	Signal	Signal	32
33	Signal	Ground	34	33	Ground	Signal	34
35	Ground	Signal	36	35	Signal	+3.3V	36
37	Signal	+5V	38	37	Ground	Signal	38
39	Ground	Signal	40	39	Signal	Ground	40
41	Signal	Signal	42	41	+3.3V	Signal	42
43	Signal	Ground	44	43	Signal	Ground	44
45	V (I/O)	Signal	46	45	Signal	Signal	46
47	Signal	Signal	48	47	Ground	Signal	48
49	Signal	+5V	50	49	Signal	+3.3V	50
51	Ground	Signal	52	51	Signal	Signal	52
53	Signal	Signal	54	53	+3.3V	Signal	54
55	Signal	Ground	56	55	Signal	Ground	56
57	V (I/O)	Signal	58	57	Signal	Signal	58
59	Signal	Signal	60	59	Ground	Signal	60
61	Signal	+5V	62	61	Signal	+3.3V	62
63	Ground	Signal	64	63	Ground	Signal	64

Note: "#" = active low

2.5.4 VGA Interface

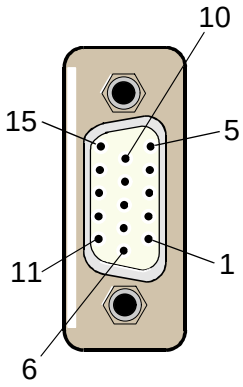


Figure 2-6: DSUB VGA Connector

The VGA interface includes an embedded 64-bit SVGA chip and a PC-compatible 15-pin female DSUB connector, BU5, which is used to connect a VGA monitor to the CP600/CP610 board. The system memory shares up to 4 MB with the video buffer and supports high resolution graphic mode 1024*768, 64k colors

2.5.4.1 VGA Connector BU5 Pinout

Table 2-8: VGA Connector BU5 Pinout

DSUB 15	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	HSYNC	Horizontal sync.	TTL Out
14	VSYNC	Vertical sync.	TTL Out
12	SDATA	I2C data	In/Out
15	SCLK	I2C clock	Out
9	VCC	Power +5V 200 mA, no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Reserved	--	--

2.5.4.2 Integrated VGA Controller

The tables below show the jumper settings for the integrated VGA controller.

Table 2-9: Jumper J19 — VGA Interrupt Selection

J19	VGA Interrupt Selection
1-2	*Disable VGA interrupt*
1-3	Enable VGA interrupt

The default setting is indicated by italics.

Table 2-10: Jumper J3 — Integrated VGA Control

J3	Integrated VGA Control
1-2	*Enable integrated VGA*
1-3	Disable integrated VGA

The default setting is indicated by italics.

Note:

If the BIOS detects an external VGA, it disables the internal VGA controller.

2.5.5 Hard-Drive Interfaces

The CP600/CP610 supports two IDE interfaces, a primary one (IDE1) and a secondary one (IDE2). The IDE interfaces are 40-pin male connector AT standard interfaces for IDE hard-disks. These two main board IDE interfaces allow up to 4 hard-disk drives (two master/slave pairs) to be connected

Each IDE interface provides support for up to two hard-disk and/or CD-ROM drives (two master-slave pairs). All hard-disks can be used in CHS mode, but the BIOS also supports the LBA mode.

Important

Each of the two interfaces, IDE1 and IDE2, support a maximum of two hard-disks connected in the master-slave mode. To configure the first as a master disk and the second as a slave disk, please refer to the hard-disk manufacturer's documentation.

2.5.5.1 IDE Interface Pinouts

If a rear I/O module is used, signals from the main board IDE connectors IDE1 and IDE2 are routed to the module connectors IDE0 and IDE1 respectively.

Table 2-11: Pinout of AT Standard Connectors IDE1/IDE2 and IDE0/IDE1

Pin	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In

Table continued on following page

Table 2-11: Pinout of AT Standard Connectors IDE1/IDE2 and IDE0/IDE1

Pin	Signal	Function	In/Out
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	N/C	--	--
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--

2.5.6 Floppy-Drive Interface

The CP600/CP610 is provided with a 2-row 34-pin male standard connector, ST2, realized as a 2.54-mm pitch pin-row connector which provides the signals for up to two floppy-drives.

Note:

If a rear I/O module is used, the signals from the main board connector ST2 are routed to the module interface CON2.

Important!

If the floppy-disk drive connection cable is inverted (pin 1 in place of pin 34), at "power on", the floppy-disk drive will work uninterruptedly, with consequent risk of damage to the floppy-disk inserted.

2.5.6.1 Floppy Drive Connector Pinout

Table 2-12: Floppy Drive Connector ST2 Pinout

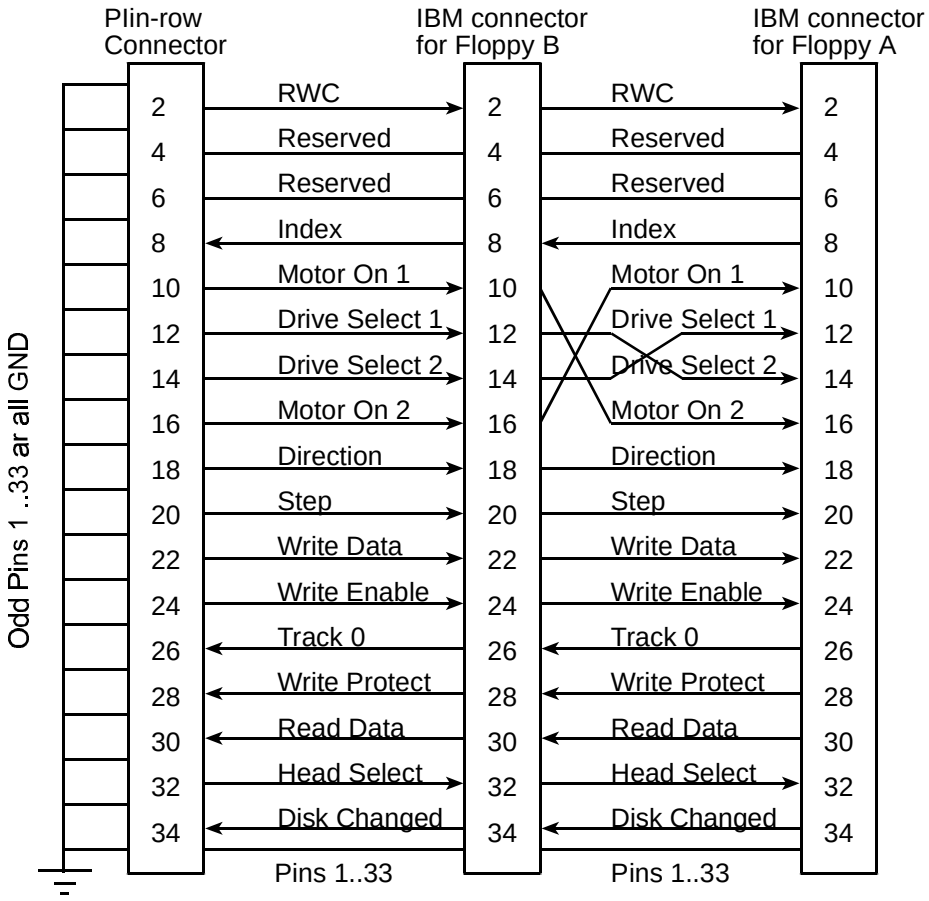
Pin	Signal	Function	In/Out
2	RWC	Write precompensation	Out
4	N/C	--	--
6	N/C	--	--
8	INDEX	Index pulse	In
10	MOTEN1	Motor 1 enable	Out
12	DRVSEL2	Driver select 2	Out
14	DRVSEL1	Driver select 1	Out
16	MOTEN2	Motor 2 enable	Out
18	DIRECTION	Step direction	Out
20	STEP	Step pulse	Out
22	WRDATA	Write data	Out
24	WREN	Write enable	Out
26	TRACK0	Track 0 signal	In
28	WRPROT	Write protect	In
30	RDDATA	Read data	In
32	HEADSEL	Head select	Out
34	DSKCHG	Disk change	In
ODD NR.	GND	Ground signal	--

2.5.6.2 Floppy-Drive “A+B” Configuration

Important!

The floppy-drive connection cable is suitable for access by two PC-compatible floppy-disk drives. Make sure you plug the cable into the connector assigned to floppy-drive “A:”. If it is plugged into the drive “B:” connector, no boot from the floppy drive is possible.

Figure 2-7: Two-Drive Floppy-Disk Configuration



2.5.7 Keyboard/Mouse Interface

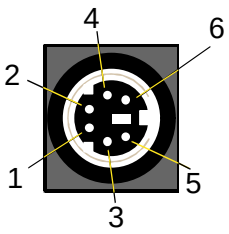


Figure 2-8: Keyboard/Mouse Connector

The CP600/CP610 is provided with a PC/AT standard keyboard/mouse connector implemented on a PS/2-type 6-pin shielded mini-DIN connector. A special adapter to connect a mouse device and/or keyboard to the PS/2 connector BU8 is available from *PEP.* The keyboard power supply unit is protected by a 500 mA fuse. All signal lines are EMI-filtered.

Note:

When a rear I/O module is used, two additional keyboard/mouse connectors become available (for details please see sections 4.1.2 and 4.1.3 in chapter 4, “Rear I/O Connector”).

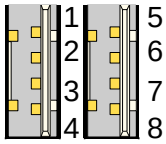
2.5.7.1 Keyboard/Mouse Connector BU8 Pinout

Table 2-13: Keyboard/Mouse Connector BU8 Pinout

Pin	Signal	Description	Direction
1	KDATA	Keyboard data	In
2	MDATA	Mouse data	In
3	GND	Ground signal	N/C
4	VCC	VCC signal	N/C
5	KCLK	Keyboard clock	Out
6	MDATA	Mouse Clock	Out

2.5.8 USB Interfaces

Figure 2-9: USB Connectors



The CP600/CP610 baseboard is provided with two independant USB interfaces implemented on the dual-stacked 4-pin connector BU7. These USB interfaces have a maximum transfer rate of 12 Mbit each. The USB power supply feeding the two connectors is protected by a 1.5A fuse. All signal lines are EMI-filtered.

Note:

When a rear I/O module is used, the signals from this baseboard interface are routed to pins 1 through 4 of the module interface CON8 (please see section 4.1.4 in chapter 4, “Rear I/O Module” for details of the module interface).

2.5.8.1 USB Connector BU7 Pinouts

Table 2-14: USB Connector BU7 Pinouts

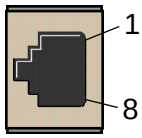
Pin	Name	Function	In/Out	Pin	Name	Function	In/Out
1	VCC	VCC signal	--	5	VCC	VCC signal	--
2	UV0-	Diff. USB-	--	6	UV1-	Diff. USB-	--
3	UV0+	Diff. USB+	--	7	UV1+	Diff. USB+	--
4	GND	GND signal	--	8	GND	GND signal	--

2.5.9 Fast Ethernet Interface

An extremely efficient 10/100 MBaud Fast Ethernet controller for CompactPCI applications is provided which supports star topologies and provides remote booting capability.

Figure 2-10: Ethernet/Fast Ethernet Connector

This connector supplies 10Base-T/100Base-TX signal interfacing to the Ethernet controller. The Ethernet connector is realized as an RJ45 unshielded twisted-pair connector. The interface provides automatic detection and switching between 10Base-T and 100Base-TX data transmission.



2.5.9.1 Ethernet Connector BU1 Pinout

Table 2-15: Ethernet Connector BU1 Pinout

RJ45	Signal	Function
1	TX+	Transmit +
2	TX-	Transmit –
3	RX+	Receive +
4	N/C	--
5	N/C	--
6	RX-	Receive –
7	N/C	--
8	N/C	--

2.5.10 Serial Port Interface

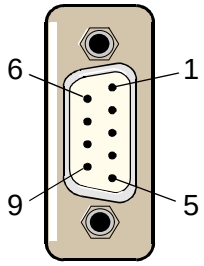


Figure 2-11: PC-Compatible D-Sub Serial Connector

The 9-pin serial port male DSUB connector COM1 allows the connection of RS232 devices to the CP600/CP610 board. One, or, in the case of the double-width version, four PC-compatible serial 9-pin DSUB ports are available with 5V charge-pump technology eliminating the need for a +12V and -12V supply.

The RS232 interface COM1, and, in the case of the double-width version of the CP600/CP610, the serial interfaces COM2..COM4 include a complete set of handshaking and modem control signals, maskable interrupt generation and data transfers of up to 460.8 kB/s..

Note:

When the board is used with a transition module, additional serial ports are available (for details, please see section 2.8.1 “Transition Module Serial Ports” in this chapter).

When a rear I/O module is used, an additional and/or alternative serial interface is available on the module (for further information please see section 4.1.1 in chapter 4, “Rear I/O Module”).

2.5.10.1 Serial Port Connector COM1 (BU3) Pinout

Table 2-16: Serial Port Connector COM1 Pinout

DSUB 9	Signal	Function	In/Out
1	DCD	Data carrier detect	In
2	RXD	Receive data	In
3	TXD	Transmit data	Out
4	DTR	Data terminal ready	Out
5	GND	Signal ground	--
6	DSR	Data set ready	In
7	RTS	Request to send	Out
8	CTS	Clear to send	In
9	RI	Ring indicator	In

2.5.11 Flash Disk

Module Versions

Different flash module versions are available. In order to achieve flexibility at low cost the FLASH disk is not soldered, but connected via a special module of M-Systems (Disk-on-Chip 2000).

- Standard flash memory of up to 512 KB in a 32-pin DIL package
  - AMD29F010
  - AMD29F040
- Standard EPROM memory in a 32-pin DIL package
  - AMD27C010
  - AMD27C020
- Disk-on-Chip flash memory:
  - 2 - 24 MB (dimensions 41.7 x 17.9 x 5.6mm);
  - 40 - 144 MB (dimensions 42.0 x 18.3 x 11.8mm).

For higher flash disk capacity it is recommended to use an ATA flash disk.

2.5.11.1 FLASH Type Selection

This solder jumper selects the FLASH type to be installed on the FLASH socket IC11.

Table 2-17: Jumper J9 — Flash Type Selection

J9	Function
Closed	4 Mbit Flash type
Open	*2 Mbit Flash type*

The default setting is indicated by italics.

2.5.12 CompactPCI Rear I/O Connector P3

2.5.12.1 CompactPCI Rear I/O Connector P3 Pinout

The CP600/CP610 is capable of conducting most I/O signals through the rear I/O connector P3. The same pinout applies to the matching rear I/O connector J3 of the rear I/O module CP-RIO6-10. For convenience this table is presented both here and in the “Rear I/O” chapter.

Table 2-18: CompactPCI Rear I/O Connector P3

Pin	Z	A	B	C	D	E	F
19	GND	IDE.PWRGD	IDE.IOCS16#	IDE.IOCHRDY	IDES.IRQ	IDEP.IRQ	GND
18	GND	IDES.CS3#	IDES.CS1#	IDEP.CS3#	IDEP.CS1#	IDES.DAK#	GND
17	GND	IDEP.D15	IDEP.D14	IDEP.D13	IDEP.D12	IDES.DRQ	GND
16	GND	IDEP.D11	IDEP.D10	IDEP.D9	IDEP.D8	IDEP.DAK#	GND
15	GND	IDEP.A0	IDEP.A1	VCC	IDEP.A2	IDEP.DRQ	GND
14	GND	IDEP.D7	IDEP.D6	IDEP.D5	IDEP.D4	IDEP.IOW#	GND
13	GND	IDEP.D3	IDEP.D2	IDEP.D1	IDEP.D0	IDEP.~IOR	GND
12	GND	FD.DS0#	FD.MSEN0	FD.MTR0#	FD.INDEX#	FD.WDATA#	GND
11	GND	FD.DS1#	FD.DSKCHG#	FD.MTR1#	FD.DENSEL	FD.RDATA#	GND
10	GND	FD.WP#	FD.HDSEL#	FD.DIR#	FD.TRK0#	FD.STEP#	GND
9	GND	FD.WGATE#	IDES.D15	IDES.D14	IDES.D13	USB+	GND
8	GND	IDES.D12	IDES.D11	VCC	IDES.D10	USB-	GND
7	GND	IDES.D9	IDES.D8	IDES.D7	IDES.D6	IDES.IOW#	GND
6	GND	IDES.D5	IDES.D4	IDES.D3	IDES.D2	IDES.IOR#	GND
5	GND	ABORT#	MSDAT	SPKR	KBDAT	RSV	GND
4	GND	PRST#	MSCLK	VCC	KBCLK	S1RXD	GND
3	GND	S1CTS	S1RTS	S1DSR	S1DCD	S1TXD	GND
2	GND	IDES.D1	IDES.D0	S1RIN	S1DTR	S2RXD	GND
1	GND	IDES.A0	IDES.A1	IDES.A2	RSV	S2TXD	GND

Legend:

- IDE primary and shared primary/secondary signals
- IDE secondary signals
- Floppy-disk signals
- COM1, COM2, and USB serial signals
- Mouse, keyboard, reset, speaker, and reserved signals

2.6 Miscellaneous Baseboard Jumper Settings/Pinouts

2.6.1 External BIOS

It is possible to re-direct the first CPU fetch from the on-board flash to the Flash socket IC11

2.6.1.1 External BIOS Jumper Setting

Table 2-19: Jumper J2 — BIOS Selection

J2	Function	Notes
Closed	External BIOS	To be set only in the event that the on-board FLASH does not function.
Open	*Internal BIOS*	*Normal boot from the on-board BIOS*

The default setting is indicated by italics.

2.6.2 Fan Power Supply

The onboard cooling fan for cooling the CPU may be connected via the power connector J4.

2.6.2.1 Fan Power Supply Pinout

Table 2-20: Fan Power Supply Pinout

J4	Description
2	+5V
1	GND
3	+12V

2.7 Baseboard General Features

2.7.1 Battery

The CP600/CP610 is provided with a 3.0V “coin cell” lithium battery for the RTC.

To replace the battery please proceed as follows:

- Switch power off
- Remove the battery
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. Suitable batteries include the VARTA CR2025 and PANASONIC BR2020

Important

- Care must be taken to ensure that the battery is correctly replaced.
- The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer’s instructions.
- The typical life expectancy of a 170 mAh battery (VARTA CR2025) is 4 - 5 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.
  To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 3 - 4 years.
- **The CMOS setting is backed up inside the EEPROM which means that *the board will operate without a battery*, however, it should be noted that the RTC will not operate without a battery.**

2.7.2 Reset

The CP600/CP610 is automatically reset by a precision voltage monitoring circuit that detects when the supply is below the acceptable operating limit of 4.725 V for the 5V line and below 3.0V for the 3.3V line, or in the event of a power failure of the DC/DC converter. Other reset sources include the watchdog timer and local push-button switch. Jumper setting for the local push-button switch is given in table 2-17 below. The CP600/CP610 responds to any of these sources by initializing local peripherals and issuing the PCIRST* signal on the CompactPCI bus.

Note:

To generate a reset, the push button must be pressed for longer than 2 seconds.

2.7.2.1 External Reset Jumper Setting

An external reset button placed on the front panel of the tower or rack may be connected to this jumper.

Table 2-21: Jumper J1 — External Reset

J1	Function
Open	*Normal operation*
Closed	System reset

2.8 Transition Module TR1

The CP600/CP610 transition module carries three additional serial ports and one parallel port, the jumper settings and pinouts for all of which are detailed below. The serial ports COM2, COM3 and COM4 can alternatively support an RS232, RS422 or RS485 interface. The standard configuration is RS232. Note that there is no jumper setting required for the parallel port.

2.8.1 Transmission Module Serial Port Interfaces

In addition to the serial port of the single-width version of the CP600/CP610, the double width version is provided with an additional three PC-compatible serial 9-pin DSUB ports, making a total of four. These ports support the same 5V charge-pump technology in order to eliminate the need for a +12V and -12V supply. Every port includes a complete set of handshaking and modem control signals, maskable interrupt generation and data transfers of up to 460.8 kB/s. For an illustration of the serial port please see Figure 2-11 on page 2-26.

The additional COM2, COM3 and COM4 interfaces of the double-width version may be configured as an RS232, RS422 or RS485 port by setting the appropriate solder jumpers. The standard settings of these interfaces envisage the RS232 configuration.

2.8.1.1 Transition Module Serial Port Connector Pinouts

Table 2-22: TR1 Serial Port Connector COM2, COM3 and COM4 Pinouts

Pins	RS232	RS422*	RS485
1	DCD	+RXD	N/C
2	RXD	+CTS	N/C
3	TXD	+TXD	+TRXD
4	DTR	+RTS	N/C
5	GND	GND	GND
6	DSR	-RXD	N/C
7	RTS	-CTS	N/C
8	CTS	-TXD	-TRXD
9	RI	-RTS	N/C

* The RS422 pinout is *PEP*-specific. With this interface the signals “DTR” and “DCD” are not pinned out

2.8.1.2 Transition Module Serial Port Jumper Settings

The additional serial ports COM2, COM3 and COM4 of the CP600/CP610 transition module can be set to either RS232, RS422 or RS485 mode by setting solder jumpers J1 through J57 of the module. The standard configuration is RS232.

Table 2-23: Transition Module Serial Port Jumper Settings

COM2	COM3	COM4	RS232	RS422	RS485*
J1	J46	J57	*Open*	Closed	Closed
J2	J36	J47	*Open*	Open	Closed
J3	J37	J48	*Open*	Open	Closed
J4	J38	J49	*Open*	Closed	Open
J5	J39	J50	*Open*	Closed	Open
J6	J20	J28	*2 - 1*	3 - 1	3 - 1
J7	J21	J29	*2 - 1*	3 - 1	3 - 1
J8	J22	J30	*2 - 1*	3 - 1	3 - 1
J9	J23	J31	*2 - 1*	3 - 1	3 - 1
J10	J24	J32	*2 - 1*	3 - 1	3 - 1
J11	J25	J33	*2 - 1*	3 - 1	3 - 1
J12	J26	J34	*2 - 1*	3 - 1	3 - 1
J13	J27	J35	*2 - 1*	3 - 1	3 - 1
J14	J44	J55	*Open*	Open	Closed
J15	J42	J53	*Open*	Open	Closed
J16	J43	J54	*Open*	Open	Closed
J17	J45	J56	*Open*	Open	Closed
J18	J40	J51	*Open*	Closed	Open
J19	J41	J52	*Open*	Closed	Open

The default setting is indicated by italics.

**** Please see overleaf for notes on the RS485 settings.***

Notes on the RS485 settings:

To enable the 390 Ohm termination of the +TRXD line to VCC, close J14 for COM2, J44 for COM3 or J55 for COM4.

To enable the 150 Ohm termination between the two lines +TRXD and -TRXD, close J15 and J16 for COM2, J42 and J43 for COM3 or J53 and J54 for COM4.

To enable the 390 Ohm termination of the -TRXD line to GND, close J17 for COM2, J45 for COM3 or J56 for COM4.

2.8.1.3 Module Combinations, Serial Interface Functionality and Drivers

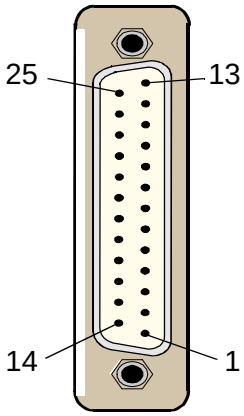
The functionality of the rear I/O module and main board/transition module serial interfaces depends on whether the rear I/O module is used in combination with a transition module (double-width board) or not (single-width board). Therefore, if a rear I/O module is used in combination with a transition module, either the drivers for the serial interface on the rear I/O module or the drivers for COM2 on the transition module must be disabled to ensure proper functioning.

Main Board+Rear I/O Module (Single-Width Version)	The COM1 interface on the baseboard front panel and the COM2 interface on the Rear I/O front panel may be used simultaneously.
Main Board+Transition Module+Rear I/O Module (Double-Width Version)	The transition module serial interface COM2 signals are routed to the rear I/O module interface COM2. Only one serial port can be used at a time.

2.8.2 Transition Module Parallel Port Interface

Figure 2-12: PC-Compatible D-Sub Parallel Port Connector

The double-width version of the CP600/CP610 is provided with an IEEE1284, ECP/EPP-compatible parallel port/printer interface. The parallel port is a 25-pin DSUB female connector mounted on the front panel.



2.8.2.1 Transition Module Parallel Port Connector Pinout

Table 2-24: 25-Pin DSUB Parallel Port Connector Pinout

DSUB Pin	Signal	Description	Direction	DSUB Pin	Signal	Description	Direction
1	-STB	Strobe data	Out	14	-AFD	Auto feed	Out
2	PD0	LSB of printer data	Out	15	-ERR	Printer error	In
3	PD1	Printer data 1	Out	16	-INIT	Initialize printer	Out
4	PD2	Printer data 2	Out	17	-SLIN	Select printer	Out
5	PD3	Printer data 3	Out	18	GND	Signal ground	N/A
6	PD4	Printer data 4	Out	19	GND	Signal ground	N/A
7	PD5	Printer data 5	Out	20	GND	Signal ground	N/A
8	PD6	Printer data 6	Out	21	GND	Signal ground	N/A
9	PD7	Printer data 7	Out	22	GND	Signal ground	N/A
10	-ACK	Character accepted	In	23	GND	Signal ground	N/A
11	BSY	Busy	In	24	GND	Signal ground	N/A
12	PE	Paper end	In	25	GND	Signal ground	N/A
13	SLCT	Ready to receive	In	N/A	GND	Signal ground	N/C

2.8.2.2 Transition Module Connection Interface

The connector located on the baseboard is a 2-row, 50-pin female connector. A matching male connector is placed on the transition module to allow transmission of signals between the two boards.

2.9 Software Configuration

2.9.1 IRQ Routing

The CP600/CP610 board uses a standard AT IRQ routing (8259 Controller).

Table 2-25: Interrupt Routing

Controller 1			Controller 2	
IRQ0	Timer		IRQ8	Real-time controller
IRQ1	Keyboard		IRQ9	PCI
IRQ2	Interrupt controller 2		IRQ10	PCI
IRQ3	COM2	← Input of Controller 2	IRQ11	PCI
IRQ4	COM1		IRQ12	PCI
IRQ5	Watchdog		IRQ13	Co-proces-sor error
IRQ6	Floppy		IRQ14	IDE 1
IRQ7	LPT1		IRQ15	IDE 2

2.9.2 Memory Map

The CP600/CP610 board uses the standard AT ISA memory map. The following table provides the memory map for the first Megabyte:

Table 2-26: First Megabyte Memory Map

Memory	Size	Function
0xE0000..0xFFFFF	128k	BIOS implemented in Flash EPROM Reset vector 0xFFFF0
0xD8000..0xDFFFF	32k	Flash
0xC8000..0xCFFFF	32k	Free
0xC0000..0xC7FFF	32k	BIOS of the VGA card.
0xA0000..0xBFFFF	128k	Normally used as video RAM as follows: CGA video: 0xB8000..0xBFFFF Monochrome video: 0xB0000..0xB7FFF EGA/VGA video: 0xA0000..0xAFFFF
0x000000..0x9FFFF	640k	DOS reserved memory space
0x00000..0x00501	1281	BIOS data area and interrupt space

2.9.3 Address Map for the I/O Area

The following table provides the address map for the I/O area:

Table 2-27: Address Map for I/O Area

Address Range	Device
0x000 - 0x00F	DMA controller #1
0x020 - 0x021	Interrupt controller #1
0x022 - 0x02F	Reserved
0x040 - 0x043	Timer
0x060 - 0x063	Keyboard interface
0x070 - 0x071	RTC port
0x080 - 0x08F	DMA page register
0x0A0 - 0x0A1	Interrupt controller #2
0x0C0 - 0x0DF	DMA controller #2
0x0E0 - 0x0EF	Reserved
0x0F0 - 0x0FF	Math co-processor
0x170 - 0x17F	Hard disk secondary
0x1F0 - 0x1FF	Hard disk primary
0x278 - 0x27F	Parallel port LPT2
0x280	Watchdog trigger
0x282	Watchdog time
0x284	Interrupt routing
0x286	I/O status
0x288	Board version
0x289	Hardware index
0x28A	Jumper status
0x28B	Logic index
0x28C	PCI interrupt routing
0x28E	MMU
0x2E8 - 0x2EF	Serial port COM4
0x2F8 - 0x2FF	Serial port COM2
0x370 - 0x371	Super-I/O #2 command register
0x378 - 0x37F	Parallel port LPT1
0x3BC - 0x3BF	Parallel port LPT3
0x3E8 - 0x3EF	Serial port COM3
0x3F0 - 0x3F7	Floppy Disk + Super-I/O #1 Com.
0x3F8 - 0x3FF	Serial port COM1

Legend:

CP600/CP610-specific registers

2.9.4 Special Registers

The following registers are special registers for the CP600/CP610 to watch the on-board hardware special features and the CompactPCI control signals.

2.9.4.1 Hardware Index

The hardware index will signal to the software when differences in the hardware require different handling by the software. It starts with the value 0 and will be incremented with each change in hardware as development continues.

I/O location 0x289

Table 2-28: Hardware Index

Bits	Type	Default	Function
7-0	R	--	Revision ID 0 = Index 0000 1 = Index 0001

2.9.4.2 Logic Version

The logic version register may be used to identify the logic status of the board by software. It starts with the value 0 and will be incremented with each logic update.

I/O location 0x28B

Table 2-29: Logic Version

Bits	Type	Default	Function
7-0	R	--	Logic version 0 = Index 0000

2.9.4.3 Watchdog

The CP600/CP610 has one watchdog timer. This timer is provided with a programmable timeout ranging from 125 msec to 256 sec. Failure to strobe the watchdog timer within a set time period results in a system reset, NMI or an interrupt. This can be configured via the register 0x284.

To enable the watchdog bit “4” of the register 0x282 must be set. If the watchdog is enabled via bit “4” this bit cannot then be cleared. With a read or write access to the register 0x280 the watchdog is retriggered.

2.9.4.4 Watchdog Trigger

A write access triggers the watchdog. The I/O location for the watchdog trigger is 0x280.

2.9.4.5 Watchdog Configuration

The I/O location for the watchdog configuration is 0x282.

Table 2-30: Watchdog Configuration

Bits	Type	Default	Function
7-5	R	0	Reserved
4	RW	0	1 = enable watchdog (W) 0 = watchdog disabled (R)
3-0	RW	0	0 = 125 msec 1 = 250 msec 2 = 500 msec 3 = 1 sec 4 = 2 sec 5 = 4 sec 6 = 8 sec 7 =16 sec 8 = 32 sec 9 = 64 sec A= 128 sec B= 256 sec C - F reserved

2.9.4.6 Interrupt Configuration Register

The interrupt configuration register holds a series of bits defining the interrupt routing for the watchdog, the power control derate signal and the CompactPCI enumeration signal.

If the watchdog timer fails, it can generate three independent hardware events: reset, NMI and interrupt.

The enumeration signal is generated by a hotswap compatible board after insertion and prior to removal. The system uses this interrupt signal to force software to configure the new board.

The derate signal indicates that the power supply is beginning to derate its power output.

The I/O location for the interrupt configuration is 0x284.

Table 2-31: On-Board Interrupt Configuration

Bits	Type	Default	Function
7-5	R	0	Reserved
4	RW	0	CPCI enum signal IRQ routing (IRQ5) 1 = enable IRQ 0 = disable IRQ
3	RW	0	CPCI derate signal IRQ routing (IRQ5) 1 = enable IRQ 0 = disable IRQ
2	RW	0	Watchdog hardware reset 1 = enable reset 0 = disable reset
1	RW	0	Watchdog IRQ routing (IRQ5) 1 = enable IRQ 0 = disable IRQ
0	RW	0	Watchdog NMI routing 1 = enable NMI 0 = disable NMI

2.9.4.7 I/O Status

This register describes the local and CompactPCI control signals. The watchdog status bit indicates the status of the watchdog timer. If the timer is not retriggered within the previously set time period, the bit is set to “0” and the watchdog LED lights up. The fail signal is an output of the power supply indicating a power supply failure.

For a description of the derate and enumeration signals please see section 2.9.4.6, “Interrupt Configuration Register on the preceding page.

The I/O location for the I/O status is 0x286.

Table 2-32: Local and CompactPCI Control Inputs

Bits	Type	Default	Function	Available on
7	R	--	Watchdog status 0 = watchdog impulse generated	CP600/610
6	R	--	P4/P5 system enumeration hot swap 0 = new board	CP610 only
5	R	--	P4/P5 supply fail signal of CompactPCI 0 = fail	CP610 only
4	R	--	P4/P5 derating signal of CompactPCI 0 = derated	CP610 only
3	R	--	System slot identification 0 = system slot	CP600/610
2	R	--	P1/P2 system enumeration hot swap 0 = new board	CP600/610
1	R	--	P1/P2 supply fail signal of CompactPCI 0 = fail	CP600/610
0	R	--	P1/P2 derating signal of CompactPCI 0 = derated	CP600/610

2.9.4.8 Board ID

Memory mapped I/O location 0x288.
This register describes the hardware and the board index.

Table 2-33: Board ID

Bits	Type	Default	Function
7 - 0	R	1	Board version 0 = reserved 1 = CP610 17 = CP610 Index 1 2 = CP312 18 = CP312 Index 1 3 = CP600 19 = CP600 Index 1 4 = CP611 20 = CP611 Index 1 5 = CP612 21 = CP612 Index 1 32 = CP602

2.9.4.9 Jumper Status

These registers can be used to read the on-board jumper configuration.

The I/O location for the jumper status is 0x28A.

Table 2-34: On-Board Jumper Status and Clock Setting

Bits	Type	Default	Function
7	R	1	Boot jumper 1 = on-board flash 0 = socket flash
6	R	--	Reserved
5	R	--	Reserved
4	R	--	Reserved
3-2	R	--	Reserved
1	R	1	Reserved
0	R	1	Reserved

2.9.4.10 PCI Interrupt Routing

This register is used by the CPU to control the PCI interrupt routing. Every interrupt line of the backplane can be enabled or disabled. The interrupt mask register bits enable the appropriate bits when low and disable them when high. The default configuration is “all interrupts enabled”.

The I/O location for the PCI interrupt routing is 0x28C.

Table 2-35: PCI Interrupt Routing

Bits	Type	Default	Function
7	RW	0	P4/P5 INTD
6	RW	0	P4/P5 INTC
5	RW	0	P4/P5 INTB
4	RW	0	P4/P5 INTA
3	RW	0	P1/P2 INTD
2	RW	0	P1/P2 INTC
1	RW	0	P1/P2 INTB
0	RW	0	P1/P2 INTA

2.9.4.11 Memory Management of Flash Socket

This register controls the higher address lines for the Flash socket. The 32 kB of flash memory space is mapped from 0xD80000 - 0xDFFFF.

The I/O location of the memory management unit is 0x28E.

Table 2-36: Memory Management

Bits	Type	Default	Function
7-4	R	--	Reserved
3	RW	0	Address A18
2	RW	0	Address A17
1	RW	0	Address A16
0	RW	0	Address A15

2.10 Software Support

Real-time operating systems such as QNX and VxWorks are supported. The standard PC features supported by the BIOS also allow the use of PC operating systems such as MS-DOS, Windows 9x, Windows 2000, Windows NT, OS-2, or UNIX.

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Chapter 3

Installation

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3. Installation

3.1 Board Installation

Caution!

If your board type is not specifically qualified as hotswap capable, please switch off the CompactPCI system before installing the board in a free CompactPCI slot. Failure to do so could endanger your life/health and may damage your board or system.

Note:

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure your system is provided with an appropriate free slot to insert the board.

ESD Equipment!

Your CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

Chapters 2 and 4 of this manual describe the hardware and software setup of the controller board CP600/CP610, and also the CPU and the following devices relating to it:

- serial ports COM1 and COM2
- floppy-disk interface
- two IDE hard-disk interfaces
- keyboard/mouse interface on the front panel
- VGA
- USB
- Fast Ethernet
- parallel port
- PMC interface

PEP Advantage

One or more of the above mentioned mass storage and I/O devices may be connected to your CP600/CP610 controller board. However, none of these devices need necessarily be installed, as the CP600/CP610 is designed to be bootstrapped solely from the FLASH device.

3.1.1 Placement of the CP600/CP610

The *PEP* CompactPCI system configuration is characterized by the fact that its system slot (slot 1) is on the right end of the backplane, thus allowing for physical CPU growth (heat sink, cooling fan etc.) associated with higher performance processors.

Important!

Please ensure that your controller board is inserted in the system slot and not in one of the peripheral slots.

3.1.2 IDE Interfaces.

The CP600/CP610 board is equipped with two IDE interfaces, a primary one, IDE1, and a secondary one, IDE2. Both are placed on the motherboard.

The two interfaces allow installation of up to four hard disks (two master-slave pairs). If installed, the hard disks are automatically recognized by the BIOS at system “power on”.

Important!

Each of the two interfaces, IDE1 and IDE2, supports a maximum of two hard-disks connected in the master-slave mode. To configure the first as a master disk and the second as a slave disk, please refer to the hard-disk manufacturer’s documentation.

Hard-Disk Installation

To install a hard-disk, it is necessary to perform the following operations in the given order:

1. Install the hardware;
2. Initialize the software necessary to run the chosen operating system.

Warning!

The incorrect connection of power or data cables may result in damage to your hard-disk unit and/or CP600/CP610 board.

3.1.3 Keyboard/Mouse Connector

The CP600/CP610 uses a PC/AT standard keyboard/mouse connection realized as a 6-pin shielded mini-DIN connector. To connect both a mouse and keyboard to your mini-DIN connector, a suitable keyboard/mouse Y-adapter may be used.

Warning!

Any incorrect pinning of your keyboard/mouse connector may result in damage to your CP600/CP610 board.

3.2 Software Installation

The installation of the Ethernet and all other on-board peripheral drivers is described in detail in the relevant Driver Kit files.

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Chapter 4

Rear I/O Module

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4. Rear I/O Module

4.1 Introduction

All 6U CPU boards provided with a P3 rear I/O connector can be upgraded with the rear I/O module CP-RIO6-10 which is inserted at the back of the system. It is plugged into the backplane CompactPCI connector P3 in line with the CPU board.

If a rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interfaces. Thus, the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

The size of the 6U rear I/O module CP-RIO6-10 is as follows:

- 233.35mm x 80mm

The rear I/O module CP-RIO6-10 is provided with the following rear panel interfaces:

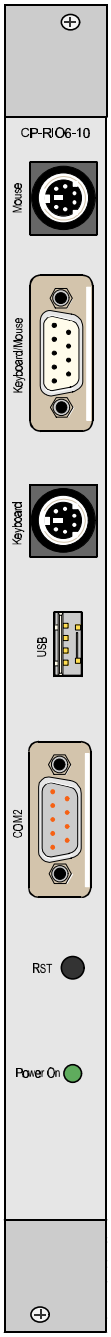
- serial interface COM2
- USB port
- PS/2 mouse connector
- PS/2 keyboard and/or mouse connector
- keyboard/ mouse connector for rugged applications
- reset button
- green LED indicating "Power On"

In addition, the rear I/O module CP-RIO6-10 is provided with the following internal interfaces:

- rear I/O connector
- floppy-disk connector
- two IDE connectors
- universal connector (signals from front panel elements)
- on-board speaker

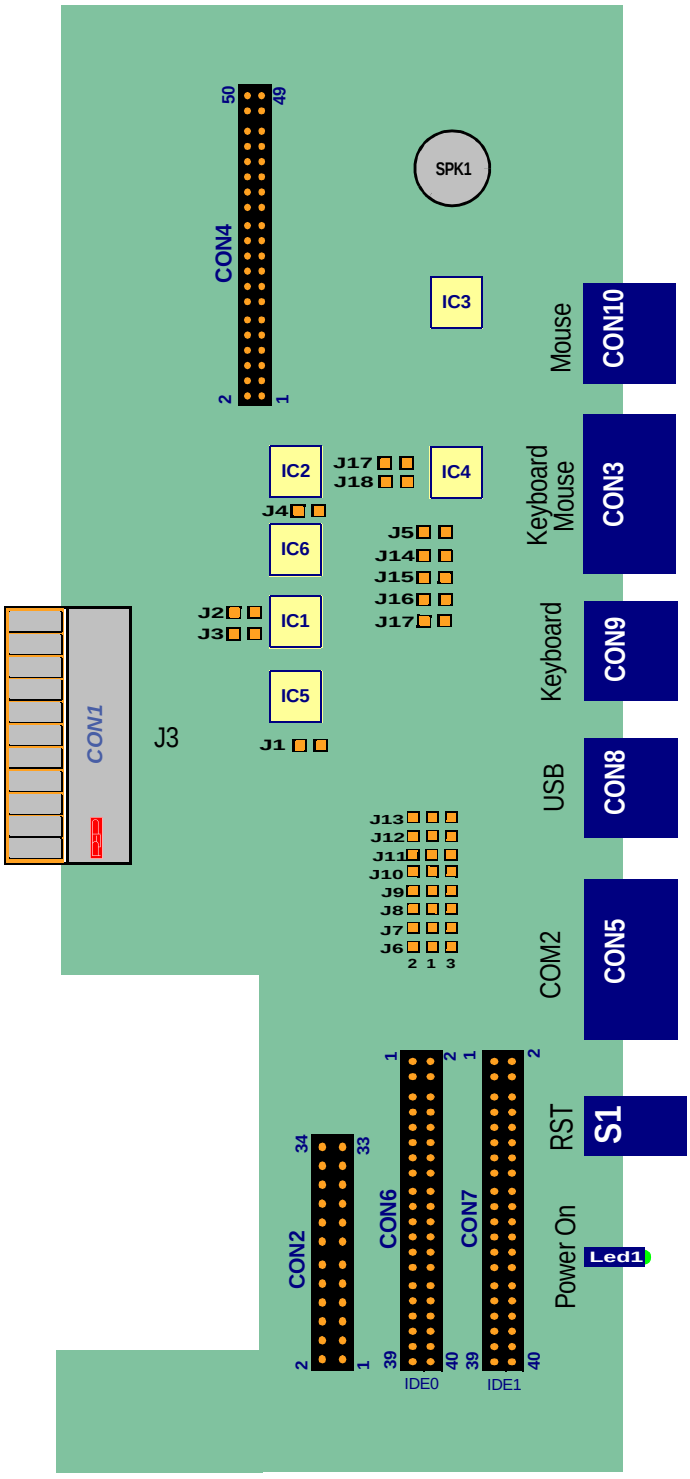
4.2 Front Panel

Figure 4-1: Front Panel View of CP-RIO6-10 Rear I/O Module



4.3 Board Layout

Figure 4-2: CP-RIO6-10 Rear I/O Module Layout



4.4 Rear I/O Module Interfaces

The CP-RIO6-10 rear I/O module is provided with the front panel and internal interfaces described below. If a rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interfaces..

Note:

If the functionality of a main board/front panel interface is routed to the respective module interfaces, any of these connectors may be used, but only one connector at a time.

4.4.1 CompactPCI Rear I/O Connector J3 (CON1)

The rear I/O module CP-RIO6-10 is provided with a 2 mm x 2 mm pitch female rear I/O connector J3. The same pinout applies to the matching rear I/O connector P3 of the CP600/CP610 baseboard. For convenience this table is presented both here and in the "Functional Description and Configuration" chapter.

Table 4-1: CompactPCI Rear I/O Connector J3 (CON1)

Pin	Z	A	B	C	D	E	F
19	GND	IDE.PWRGD	IDE.IOCS16#	IDE.IOCHRDY	IDES.IRQ	IDEP.IRQ	GND
18	GND	IDES.CS3#	IDES.CS1#	IDEP.CS3#	IDEP.CS1#	IDES.DAK#	GND
17	GND	IDEP.D15	IDEP.D14	IDEP.D13	IDEP.D12	IDES.DRQ	GND
16	GND	IDEP.D11	IDEP.D10	IDEP.D9	IDEP.D8	IDEP.DAK#	GND
15	GND	IDEP.A0	IDEP.A1	VCC	IDEP.A2	IDEP.DRQ	GND
14	GND	IDEP.D7	IDEP.D6	IDEP.D5	IDEP.D4	IDEP.IOW#	GND
13	GND	IDEP.D3	IDEP.D2	IDEP.D1	IDEP.D0	IDEP.~IOR	GND
12	GND	FD.DS0#	FD.MSEN0	FD.MTR0#	FD.INDEX#	FD.WDATA#	GND
11	GND	FD.DS1#	FD.DSKCHG#	FD.MTR1#	FD.DENSEL	FD.RDATA#	GND
10	GND	FD.WP#	FD.HDSEL#	FD.DIR#	FD.TRK0#	FD.STEP#	GND
9	GND	FD.WGATE#	IDES.D15	IDES.D14	IDES.D13	USB+	GND
8	GND	IDES.D12	IDES.D11	VCC	IDES.D10	USB-	GND
7	GND	IDES.D9	IDES.D8	IDES.D7	IDES.D6	IDES.IOW#	GND
6	GND	IDES.D5	IDES.D4	IDES.D3	IDES.D2	IDES.IOR#	GND
5	GND	ABORT#	MSDAT	SPKR	KBDAT	RSV	GND
4	GND	PRST#	MSCLK	VCC	KBCLK	S1RXD	GND
3	GND	S1CTS	S1RTS	S1DSR	S1DCD	S1TXD	GND
2	GND	IDES.D1	IDES.D0	S1RIN	S1DTR	S2RXD	GND
1	GND	IDES.A0	IDES.A1	IDES.A2	RSV	S2TXD	GND

Legend:

- IDE primary and shared primary/secondary signals
- IDE secondary signals
- Floppy-disk signals
- COM1, COM2, and USB serial signals
- Mouse, keyboard, reset, speaker, and reserved signals

4.4.2 Rear I/O Serial Port Interface

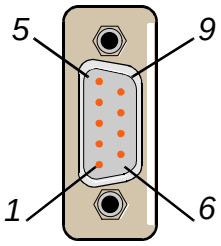


Figure 4-3: PC-Compatible D-Sub Serial Connector COM2

Depending on whether the rear I/O module is used with the single-width or double-width version of the 6U CPU board, an additional and/or alternative 9-pin male connector, COM2, is available on the module which can alternatively support an RS232, RS422 or RS485 interface, the standard configuration being RS232. This interface includes a complete set of handshaking and modem control signals, maskable interrupt generation and data transfers of up to 460.8 kB/s.

.

Table 4-2: Serial Interface Configuration with Rear I/O Module

Single-Width Board	COM1 and COM2 can be used simultaneously.
Double-Width Board	The main board serial interface COM2 signals are routed to the rear I/O module interface COM2. Only one serial port maybe used at a time.

Note:

The functionality of the rear I/O module and main board/transition module serial interfaces depends on whether the rear I/O module is used in combination with a transition module (double-width board) or not (single-width board). If a rear I/O module is used in combination with a transition module, either the drivers for the serial interface on the rear I/O module or the drivers for COM2 on the transition module must be disabled to ensure proper functioning.

4.4.2.1 Rear I/O Serial Port Connector COM2 Pinout

Table 4-3: Rear I/O Serial Port Connector COM2 Pinout

Pins	RS232	RS422*	RS485
1	DCD	+RXD	N/C
2	RXD	+CTS	N/C
3	TXD	+TXD	+TRXD
4	DTR	+RTS	N/C
5	GND	GND	GND
6	DSR	-RXD	N/C
7	RTS	-CTS	N/C
8	CTS	-TXD	-TRXD
9	RI	-RTS	N/C

* The RS422 pinout is *PEP*-specific. The signals “DTR” and “DCD” are not pinned out.

4.4.2.2 Rear I/O Serial Port Connector COM2 Jumper Settings

The serial port COM2 of the CPRIO6-10 rear I/O module may be set to either RS232, RS422 or RS485 mode by setting solder jumpers ”J1” through “J19” of the module. The standard configuration is RS232.

Table 4-4: Rear I/O Serial Port Connector Jumper Settings

Jumper	RS232	RS422	RS485
J1	*Open*	Closed	Closed
J2	*Open*	Open	Closed
J3	*Open*	Open	Closed
J4	*Open*	Closed	Open
J5	*Open*	Closed	Open
J6	*2 - 1*	3 - 1	3 - 1
J7	*2 - 1*	3 - 1	3 - 1
J8	*2 - 1*	3 - 1	3 - 1
J9	*2 - 1*	3 - 1	3 - 1
J10	*2 - 1*	3 - 1	3 - 1
J11	*2 - 1*	3 - 1	3 - 1
J12	*2 - 1*	3 - 1	3 - 1
J13	*2 - 1*	3 - 1	3 - 1
J14	*Open*	Open	Please refer to notes below for settings
J15	*Open*	Open	
J16	*Open*	Open	
J17	*Open*	Open	
J18	*Open*	Closed	Open
J19	*Open*	Closed	Open

The default setting is indicated by italics.

Notes on the RS485 settings:

To enable the 390 Ohm termination of the +TRXD line to VCC, close J14 for COM2.

To enable the 150 Ohm termination between the two lines +TRXD and -TRXD, close J15 and J16 for COM2.

To enable the 390 Ohm termination of the -TRXD line to GND, close J17 for COM2.

4.4.3 Rear I/O Keyboard/Mouse Connectors

The rear I/O module is provided with three keyboard and/or mouse connectors; two normal and one ruggedised..

Table 4-5: Rear I/O Keyboard/Mouse Connectors

6-Pin Mini-DIN for Mouse	CON 10
6-Pin Mini-DIN for Keyboard/Mouse	CON 9
9-Pin Female DSUB for Keyboard/Mouse	CON 3

4.4.3.1 Normal Keyboard/Mouse PS/2 Interfaces

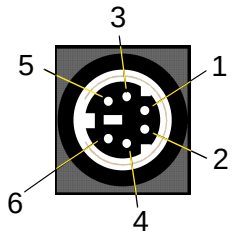


Figure 4-4: Keyboard/Mouse PS/2 Connector

The rear I/O module is provided with two PC/AT standard keyboard/mouse connectors realized as PS/2-type 6-pin shielded mini-DIN connectors. The keyboard power supply unit is protected by a 500 mA fuse. All signal lines are EMI-filtered.

4.4.3.2 Ruggedized Keyboard/Mouse Interface CON3

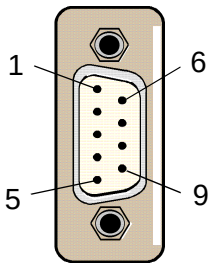


Figure 4-5: Keyboard/Mouse DSUB Connector CON3

A special 9-pin female DSUB connector is provided on the rear I/O module for rugged industrial applications where there is danger of disconnection of ordinary connectors due to vibration. All the signals from the keyboard/mouse connectors CON9 and CON10 are routed to this connector.

.

Note:

To use the keyboard/mouse connector CON3 a special cable is necessary (for pinout please see table 4-6 on page 11 of this chapter).

4.4.3.3 Rear I/O Module Keyboard/Mouse Connector Pinouts

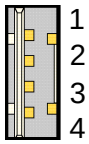
The pinouts of the rear I/O module keyboard/mouse connectors are described in the following table.

Table 4-6: Rear I/O Module Keyboard/Mouse Connector Pinouts

Pin	CON10	CON9	CON3
1	MDATA	KDATA	MDATA
2	NC	MDATA	GND
3	GND	GND	VCCPS2
4	VCCPS2	VCCPS2	NC
5	MCLK	KCLK	KCLK
6	NC	MCLK	MCLK
7	--	--	GND
8	--	--	VCCPS2
9	--	--	KDATA

4.4.4 USB Interface

Figure 4-6: USB Connector CON8



If the rear I/O module is used, the signals from pins 1 through 4 of the main board connector BU7 are routed to the module interface CON8.

One USB interface with a maximum transfer rate of 12 Mbit each is provided. The USB power supply feeding the connector is protected by a 1.5 A fuse. All signal lines are EMI-filtered..

Note:

Only one USB connector is accessible from the rear I/O module front panel.

4.4.4.1 Rear I/O Module USB Connector CON8 Pinout.

Table 4-7: Rear I/O Module USB Connector CON8 Pinout

Pin	Name	Function	In/Out
1	VCC	VCC signal	--
2	UV0-	Diff. USB-	--
3	UV0+	Diff. USB+	--
4	GND	GND signal	--

4.4.5 IDE Interfaces

If a rear I/O module is used, the main board IDE interfaces IDE1 and IDE2 are routed to the module interfaces IDE0, IDE1 respectively.

4.4.5.1 IDE Interface CON6 and CON7 Pinouts

Table 4-8: Pinout of AT Standard Connectors CON6 and CON7

Pin	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out

Table continued on following page

Table 4-8: Pinout of AT Standard Connectors CON6 and CON7

Pin	Signal	Function	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	N/C	--	--
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--

4.4.6 Rear I/O Module Universal Interface CON4

This 50-pin 2.54mm connector provides all the signals for the front panel elements and for the speaker as set out below.

Table 4-9: Rear I/O Module Universal Connector CON4 Pinouts

Pin	Signal	FP Element	Pin	Signal	FP Element
1	COM, Pin 1	COM	2	COM, Pin 6	COM
3	COM, Pin 2	COM	4	COM, Pin 7	COM
5	COM, Pin 3	COM	6	COM, Pin 8	COM
7	COM, Pin 4	COM	8	COM, Pin 9	COM
9	GND	COM	10	GND	COM
11	NC	--	12	NC	--
13	VCCUSB	USB	14	VCCUSB	USB
15	UV0-	USB	16	UV0+	USB
17	GNDUSB	USB	18	GNDUSB	USB
19	NC		20	NC	
21	MDATA	Key-board/Mouse	22	MCLK	Key-board/Mouse
23	VCCPS2	Key-board/Mouse	24	VCCPS2	Key-board/Mouse
25	KDATA	Key-board/Mouse	26	KCLK	Key-board/Mouse
27	GND	Key-board/Mouse	28	GND	Key-board/Mouse
29	NC	--	30	NC	--
31	RST	Reset button	32	GND	Reset button
33	NC		34	NC	
35	VCC	Speaker	36	SPKR	Speaker
37	NC	--	38	NC	--
39	NC	--	40	NC	--
41	VCC	--	42	VCC	--
43	VCC	--	44	VCC	--
45	NC	--	46	NC	--
47	GND	--	48	GND	--
49	GND	--	50	GND	--

4.4.7 Floppy-Drive Interface

The rear I/O module CP-RIO6-10 is provided with a 34-pin, 2.54-mm pitch pin-row connector.

Warning!

If the floppy-disk drive connection cable is inverted (pin 1 in place of pin 34), at “power on”, the floppy-disk drive will work uninterruptedly, with consequent risk of damaging the floppy-disk inserted.

4.4.7.1 Floppy Drive Connector CON2 Pinout

Table 4-10: Floppy Drive Connector CON2 Pinout

Pin	Signal	Function	In/Out
2	RWC	Write precompensation	Out
4	N/C	--	--
6	N/C	--	--
8	INDEX	Index pulse	In
10	MOTEN1	Motor 1 enable	Out
12	DRVSEL2	Driver select 2	Out
14	DRVSEL1	Driver select 1	Out
16	MOTEN2	Motor 2 enable	Out
18	DIRECTION	Step direction	Out
20	STEP	Step pulse	Out
22	WRDATA	Write data	Out
24	WREN	Write enable	Out
26	TRACK0	Track 0 signal	In
28	WRPROT	Write protect	In
30	RDDATA	Read data	In
32	HEADSEL	Head select	Out
34	DSKCHG	Disk change	In
ODD NR.	GND	Ground signal	--

More detailed information about the floppy-disk connector, in particular its configuration, is available in section 2.5.6 in chapter 2, “Functional Description and Configuration”.

Chapter 5

CMOS Setup

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5. CMOS Setup

This chapter describes the Award BIOS Setup program, EliteBIOS, version 4.51PG. The Setup program lets you modify basic system configuration settings.

5.1 Proprietary Notice

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5.2 Introduction to Setup

This manual describes the Award BIOS Setup program. The Setup program lets you modify basic system configuration settings. The settings are then stored in a dedicated battery-backed memory, called CMOS RAM, that retains the information when the power is turned off.

A special feature of *PEP's* CompactPCI boards is that all Setup information is additionally saved in a non-volatile serial EEPROM. This feature provides the user with enhanced data security in comparison with a standard PC board, because setup data will not be lost should the battery fail.

The Award BIOS in your computer is a customized version of an industry-standard BIOS for IBM PC AT–compatible personal computers. It supports the Intel®x86 and compatible processors. The BIOS provides critical low-level support for the system central processing, memory, and I/O subsystems.

The Award BIOS has been customized by adding important, but nonstandard, features such as virus and password protection, power management, and detailed fine-tuning of the chipset controlling the system.

The rest of this manual is intended to guide you through the process of configuring your system using Setup.

Starting Setup

The Award BIOS is immediately activated when you first turn on the computer. The BIOS reads system configuration information in CMOS RAM and begins the process of checking out the system and configuring it through the Power-on Self Test (POST).

When these preliminaries are finished, the BIOS seeks an operating system on one of the data storage devices (hard drive, floppy drive, etc.). The BIOS launches the operating system and hands control of system operations to it.

During POST, you can start the Setup program in one of two ways:

- By pressing <Del> immediately after switching the system on, or
- By pressing the <Del> key or by simultaneously pressing <CTRL>, <ALT>, and <ESC> keys when the following message appears briefly at the bottom of the screen during POST:

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the RESET button on the system case. You may also restart by simultaneously pressing <CTRL>, <ALT>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message appears and you are again asked to

Press F1 to continue, DEL to enter SETUP

Setup Keys

The following table describes how to navigate in Setup using the keyboard.

Table 5-1: Keyboard Commands

Up Arrow	Move to previous item
Down Arrow	Move to next item
Left Arrow	Move to the item to the left
Right Arrow	Move to the item to the right
Esc Key	Main Menu: Quit without saving changes into CMOS RAM. Status Page Setup Menu and Option Page Setup Menu: Exit current page and return to Main Menu
PgUp Key	Increase the numeric value or make changes
PgDn Key	Decrease the numeric value or make changes
+ Key	Increase the numeric value or make changes
- Key	Decrease the numeric value or make changes
F1 Key	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2 Key **Shift-F2**	Change color from total of 16 colors. F2 to select color forward, Shift-F2 to select color backward
F3 Key	Calendar, only for Status Page Setup Menu
F4 Key	Reserved
F5 Key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 Key	Load the default CMOS RAM value from BIOS default table, only for Option Page Setup Menu
F7 Key	Load the default
F8 Key	Reserved
F9 Key	Reserved
F10 Key	Save all the CMOS changes, only for Main Menu

Getting Help

Press F1 and a small help window pops up that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer is no longer able to boot, the Award BIOS supports an override to the CMOS settings that resets your system to its default configuration.

You can invoke this override by immediately pressing <Insert> when you restart your computer. You can restart by either using the ON/OFF switch, the RESET button or by pressing <CTRL>, <ALT> and <Delete> at the same time.

The best advice is to only alter settings that you thoroughly understand. In particular, do not change settings in the Chipset screen without good reason. The Chipset defaults have been carefully chosen by *PEP Modular Computers* for optimum performance and reliability. Even a seemingly small change to the Chipset setup may result in the system becoming unstable.

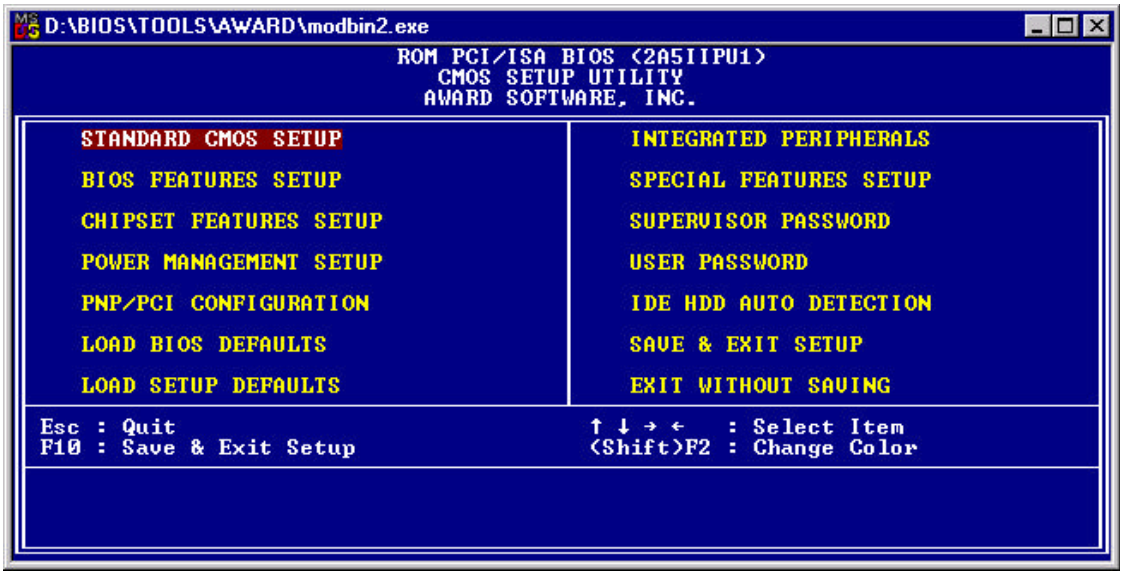
Setup Variations

Not all systems have the same Setup. While the basic look and function of the Setup program remains the same for all systems, the appearance of your Setup screens may differ from the screens shown here. Each system design and chipset combination require customized configurations. In addition, the final appearance of the Setup program depends on your system designer. Your system designer may decide that certain items should not be available for user configuration and remove them from the Setup program.

5.3 Main Setup Menu

When you enter the Award BIOS CMOS Setup Utility, a Main Menu, similar to the one shown below, appears on the screen. The Main Menu allows you to select from several Setup functions and two exit choices. Use the arrow keys to select items and press ↵ to accept and enter the sub-menu.

Figure 5-1: CMOS Setup Utility Main Menu — Screen Display



A brief description of each highlighted selection appears at the bottom of the screen.

Following is a brief summary of each Setup category.

Standard CMOS Setup

Options in the original PC AT-compatible BIOS.

BIOS Features Setup

Award enhanced BIOS options.

Chipset Features Setup

Options specific to your system chipset.

Power Management Setup

Advanced Power Management (APM) options.

PNP/PCI Configuration

PlugandPlay standard and PCI Local Bus configuration options.

Integrated Peripherals

I/O subsystems, that depend on the integrated peripherals controller in your system.

Special Features Setup

Items related to features of this board, which are not common to standard motherboard designs.

Supervisor/User Password

Change, set, or disable a password. In BIOS versions that allow separate user and supervisor passwords, only the supervisor password permits access to Setup. The user password generally allows only power-on access.

IDE HDD Auto Detection

Automatically detect and configure IDE hard disk parameters.

Load BIOS Defaults

BIOS defaults are factory settings for the most stable, minimal-performance system operations.

Load Setup Defaults

Setup defaults are factory settings for optimal-performance system operations.

Save & Exit Setup

Save settings in non-volatile CMOS RAM and exit Setup.

Exit Without Save

Abandon all changes and exit Setup.

5.4 Standard CMOS Setup

In the Standard CMOS menu you can set the system clock and calendar, record disk drive parameters and the video subsystem type, and select the type of errors that stop the BIOS POST.

Date

The BIOS determines the day of the week from the other date information. This field is for information only.

Press the → or ← key to move to the desired field (date, month, year). Press the “PgUp” or “PgDn” key to increment the setting, or type the desired value into the field.

Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the → or ← key to move to the desired field. Press the PgUp or PgDn key to increment the setting, or type the desired value into the field.

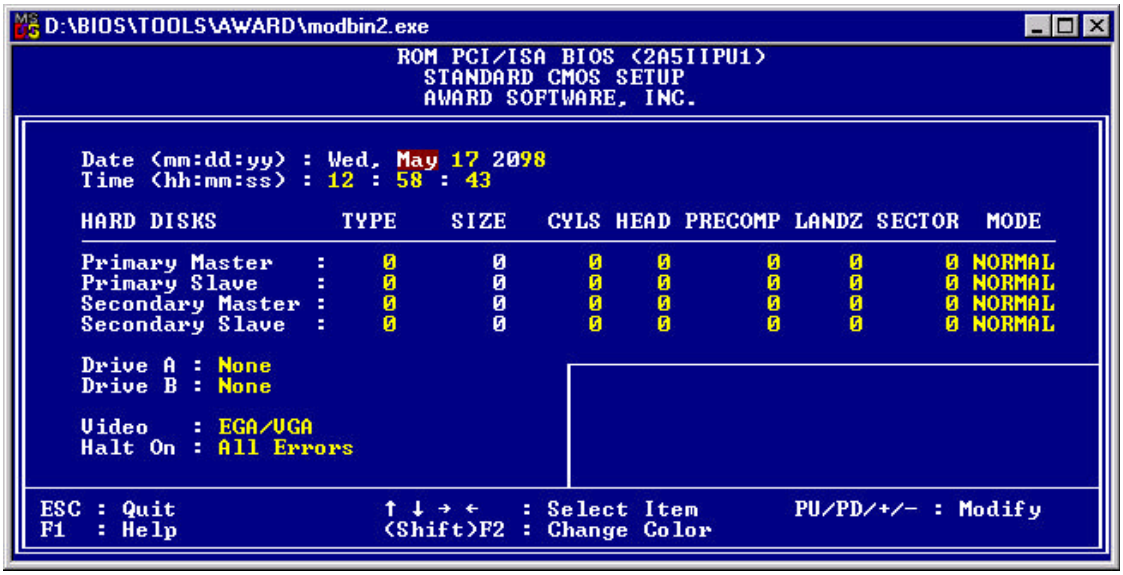
Hard Disks

The BIOS supports up to four IDE drives. This section does not show information relating to other IDE devices, such as a CD-ROM drive, or about other hard drive types, such as SCSI drives.

Important!

We recommend that you select the AUTO type for all drives.

Figure 5-2: Standard CMOS Setup Menu — Screen Display



The BIOS has the capability to automatically detect the specifications and optimal operating mode of almost all IDE hard drives. When you select type AUTO for a hard drive, the BIOS detects its specifications during POST, every time the system boots.

If you do not want to select drive type AUTO, other methods of selecting the drive type are available as follows:

1. Match the specifications of your installed IDE hard drive(s) with the pre-programmed values for drive types 1 through 45.
2. Select USER and enter values into each drive parameter field.
3. Use the IDE HDD AUTO DECTECTION function in “Setup”.

The following table provides a brief explanation of drive specifications:

Table 5-2: Description of Drive Specifications

Spec.		Description
Type		The BIOS contains a table of pre-defined drive types. Each defined drive type has a specified number of cylinders, number of heads, write pre-compensation factor, landing zone, and number of sectors. Drives whose specifications do not accommodate any pre-defined type are classified as type USER.
Size		Disk drive capacity (approximate). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.
Cyls.		Number of cylinders
Head		Number of heads
Precomp.		Write pre-compensation cylinder
Landz		Landing zone
Sector		Number of sectors
Mode	Auto	Auto: The BIOS automatically determines the optimal mode.
	Normal	The maximum number of cylinders, heads, and sectors supported are 1024, 16, and 63 respectively.
	Large	For drives that do not support LBA and have more than 1024 cylinders.
	LBA	During drive accesses, the IDE controller transforms the data address described by sector, head, and cylinder number into a physical block address, significantly improving data transfer rates. For drives with greater than 1024 cylinders.

Drive A / Drive B

Selects the correct specifications for the diskette drive(s) installed in the computer.

Table 5-3: Diskette Drives

None	No diskette drive installed
360K, 5.25 in	5-1/4 inch PC-type standard drive; 360 kilobyte capacity
1.2M, 5.25 in	5-1/4 inch AT-type high-density drive; 1.2 megabyte capacity
720K, 3.5 in	3-1/2 inch double-sided drive; 720 kilobyte capacity
1.44M, 3.5 in	3-1/2 inch double-sided drive; 1.44 megabyte capacity
2.88M, 3.5 in	3-1/2 inch double-sided drive; 2.88 megabyte capacity

Video

Selects the type of primary video subsystem in your computer. The BIOS usually detects the correct video type automatically. The BIOS supports a secondary video subsystem, however, this is not selected in Setup.

Table 5-4: Primary Video Subsystem Selection

EGA/VGA	Enhanced Graphics Adapter/Video Graphics Array. For EGA, VGA, SEGA, SVGA or PGA monitor adapters.
CGA 40	Color Graphics Adapter, power-up in 40 column mode
CGA 80	Color Graphics Adapter, power-up in 80 column mode
MONO	Monochrome adapter, includes high resolution monochrome adapters

Halt On

During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can program the BIOS to ignore certain errors during POST and continue the boot-up process. The possible selections are listed in the following table.

Table 5-5: POST Specific Commands

Command	POST Action
No errors	POST does not stop for any errors.
All errors	If the BIOS detects any non-fatal error, POST stops and prompts you to take corrective action.
All, But Keyboard	POST does not stop for a keyboard error, but stops for all other errors.
All, But Diskette	POST does not stop for diskette drive errors, but stops for all other errors.
All, But Disk/Key	POST does not stop for a keyboard or disk error, but stops for all other errors.

Memory

You cannot change any values in the Memory fields; they are only for your information. The fields show the total installed random access memory (RAM) and amounts allocated to base memory, extended memory, and other (high) memory. RAM is counted in kilobytes (KB: approximately one thousand bytes) and megabytes (MB: approximately one million bytes).

RAM is the computer's working memory, where the computer stores programs and data currently being used, so they are accessible to the CPU. Modern personal computers may contain up to 64 MB, 128 MB, or more.

Base Memory

Typically 640 KB. Also called conventional memory. The DOS operating system and conventional applications use this area.

Extended Memory

Above the 1 MB boundary. Early IBM personal computers could not use memory above 1 MB, but current PCs and their software can use extended memory.

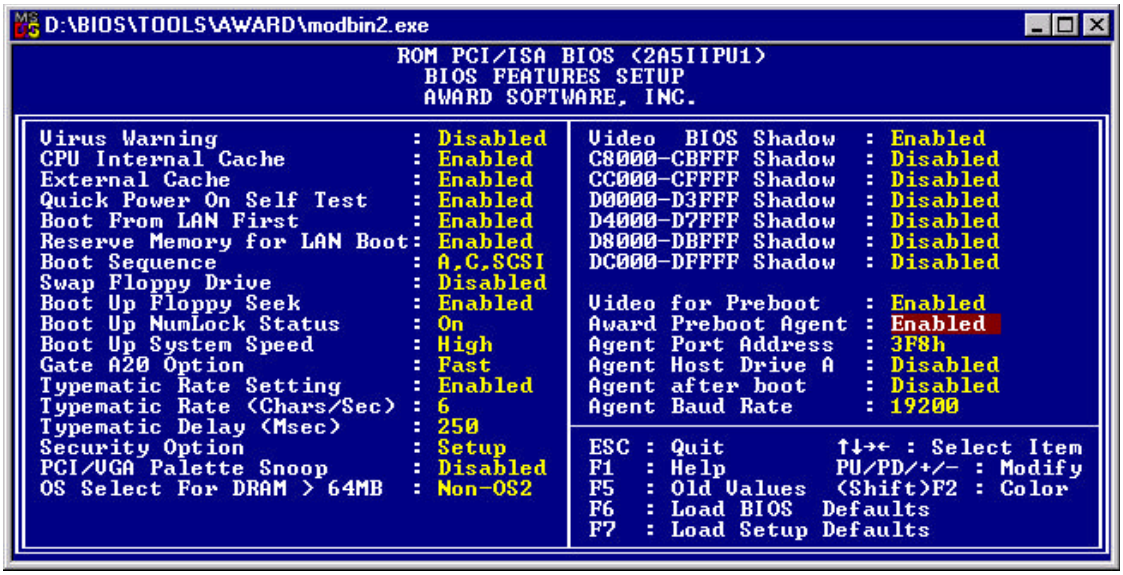
Other Memory

Between 640 KB and 1 MB; often called High Memory. DOS may load terminate-and-stay-resident (TSR) programs, such as device drivers, in this area, to free as much conventional memory as possible for applications. Lines in your CONFIG.SYS file that start with LOADHIGH load programs into high memory.

5.5 BIOS Features Setup

This screen contains industry-standard options additional to the core PC AT BIOS. This section describes all fields presented by Award Software in this screen. The example screen below may vary somewhat from the one in your Setup program; your system board designer may omit or modify some fields

Figure 5-3: BIOS Features Setup — Screen Display



CPU Internal Cache / External Cache

Cache memory is additional memory that is much faster than conventional DRAM (system memory). CPU's from 486-type on up contain internal cache memory, and most, but not all, modern PC's have additional (external) cache memory. When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU.

The External Cache field may not appear if your system does not have external cache memory.

CPU L2 Cache ECC Checking

When you select *Enabled*, memory checking is enabled when the external cache contains ECC SRAM's.

Quick Power-on Self Test

Select Enabled to reduce the amount of time required to run the power-on self-test (POST). A quick POST skips certain steps. We recommend that you normally disable quick POST. Better to find a problem during POST than lose data during your work.

Boot from LAN first

If your BIOS if capable of Booting from LAN via DHCP/BOOTP – protocol (option), you can switch this option on/off here.

Boot Sequence

The original IBM PC's loaded the operating system from drive A (floppy disk), so IBM PC-compatible systems are designed to search for an operating system first on drive A, and then on drive C (hard disk). However, modern computers usually load the operating system from the hard drive, and may even load it from a CD-ROM drive. The BIOS now offers 10 different boot sequence options of three drives each. In addition to the traditional drives A and C, options include IDE hard drives D, E and F; plus an SCSI hard drive and a CD -ROM drive.

Swap Floppy Drive

This field is effective only in systems with two floppy drives. Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.

Boot Up Floppy Seek

When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360-KB floppy drives have 40 tracks; drives with 720 KB, 1.2 MB, and 1.44 MB capacity all have 80 tracks. Because very few modern PC's have 40-track floppy drives, we recommend that you set this field to Disabled to save time.

Boot Up Numlock Status

Toggle between On or Off to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.

Boot Up System Speed

Select High to boot at the default CPU speed; select Low to boot at the speed of the AT bus. Some add-in peripherals or old software (such as old games) may require a slow CPU speed. The default setting is High.

Gate A20 Option

Gate A20 refers to the way the system addresses memory above 1 MB (extended memory). When set to Fast, the system chipset controls Gate A20. When set to Normal, a pin in the keyboard controller controls Gate A20. Setting Gate A20 to Fast improves system speed, particularly with OS/2 and Windows.

Typematic Rate Setting

When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system.

When Enabled, you can select a typematic rate and typematic delay.

Typematic Rate (Chars/Sec)

When the typematic rate setting is enabled, you can select a typematic rate (the rate at which a character repeats when you hold down a key) of 6, 8, 10, 12, 15, 20, 24 or 30 characters per second.

Typematic Delay (ms)

When the typematic rate setting is enabled, you can select a typematic delay (the delay before key strokes begin to repeat) of 250, 500, 750 or 1000 milliseconds.

Security Option

If you have set a password, select whether the password is required every time the System boots, or only when you enter Setup.

PS/2 Mouse Function Control

If your system has a PS/2 mouse port and you instal a serial pointing device, select *Disabled*.

PCI/VGA Palette Snoop

Your BIOS Setup may not contain this field. If the field is present, leave at Disabled.

OS Select for DRAM>64MB

Select OS2 only if you are running the OS/2 operating system with greater than 64 MB of RAM in your system.

Report No FDD for WIN 95

Select *Yes* to release IRQ6 when the system contains no floppy drive, for compatibility with Windows 95 logo certification. In the **Integrated Peripherals** screen, select *Disabled* for the **Onboard FDC Controller** field.

Shadow

Software that resides in a read-only memory (ROM) chip on a device is called *firmware*. The Award BIOS permits *shadowing* of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals, such as, for example, a SCSI adaptor.

Shadowing copies firmware from ROM into system RAM, where the CPU can read it through the 16-bit or 32-bit DRAM bus. Firmware not shadowed must be read by the system through the 8-bit X-bus. Shadowing improves the performance of the system BIOS and similar ROM firmware for expansion peripherals, but it also reduces the amount of high memory (640 KB to 1 MB) available for loading device drivers, etc.

Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option.

Video BIOS shadows into memory area C0000-C7FFF. The remaining areas shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.

Socket Window Page

The CP600/CP610 is equipped with a 32-pin socket to take additional Flash-ROM. This Flash-ROM may be addressed by a paging mechanism. The size of one Flash page can be set at this point as follows:

Table 5-6: Setting Flash Page Size

Page Size	Address Space used by Socket Flash EPROM
32 KB	0xD8000 - 0xDFFFF

Award Preboot Agent

Agent software may be enabled and disabled. The default is Disabled.

Agent Port Address

Select which UART address Agent software should use. Note to have set a UART in the INTEGRATED PERIPHERALS page to one of the below allowed settings. Recommended is 03F8h, which means COM1 (03F8h / IRQ 4); “auto” must not be selected.

The Agent system must have a serial (RS-232C) peripheral subsystem, to support a null modem (direct) connection.

If the Agent and host connect, but a session is not established, check the Agent COM port settings which should read as follows:

3F8h - IRQ4
2F8h - IRQ3
3E8h - IRQ4
2E8h - IRQ3

Agent Host Drive A

When the administrative host is using the Preboot Manager application, the Agent can boot and run applications from host floppy drive A. INT13 calls intended for the Agent floppy drive A are redirected by the Agent extension to the host floppy drive A. All other INT13 calls are passed along to the original interrupt handler. The Manager application can receive the Agent drive A interrupt and interpret the commands. It then calls its own INT13 handler to read or write the requested sectors to host drive A. Both Manager and Agent serial version software use Xmodem protocol for all transfers.

The floppy drive redirection feature permits support personnel to remotely administer two vital tools on the Agent system:

- PC DIAG diagnostics package from Unicore Software (available through Award Software as part of the Manager application).
- AWDFLASH BIOS flash upgrade utility. (in batch mode, this means giving the parameters at the command line; e.g. awdflash <filename> /Sn/Py, DO NOT USE INTERACTIVE MODE!!!)

Select Enabled to enable this feature, default is Disabled.

Agent after Boot

In the "standard" Agent product, Agent software continues to function after the operating system loads. However, some non-DOS operating systems are not compatible with the Agent BIOS extension, so the Agent should disable when the OS loads. Selecting Disabled turns off the Agent software just as the BIOS transfers control to the operating system. Default is Disabled.

Award Baud Rate

Select the speed at which the UART is to operate. Default is 19200. When using the Preboot Manager on the host, always select 19200 baud.

Null-Modem Cable Pinout

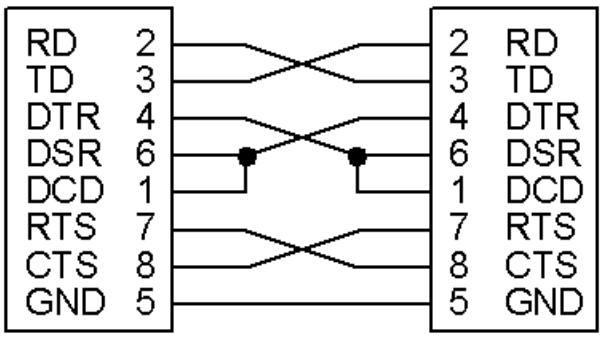


Figure 5-4: Null-Modem Cable Connection

A null-modem cable is a serial cable designed to connect two PC's. Each end has a 9-pin, female RS-232C connector. If you are creating your own 9-pin cable, connect the two ends through the cable as shown here.

Further Information

For further information please refer to the manual for the Award Preboot Agent™ 2.0 which accompanies the manual for the Award Preboot Manager™ 2.0.

5.6 Chipset Features Setup

This section describes features of the PIIX4 PCIset. If your system contains a different chipset, this section will bear little resemblance to what you see on your screen..

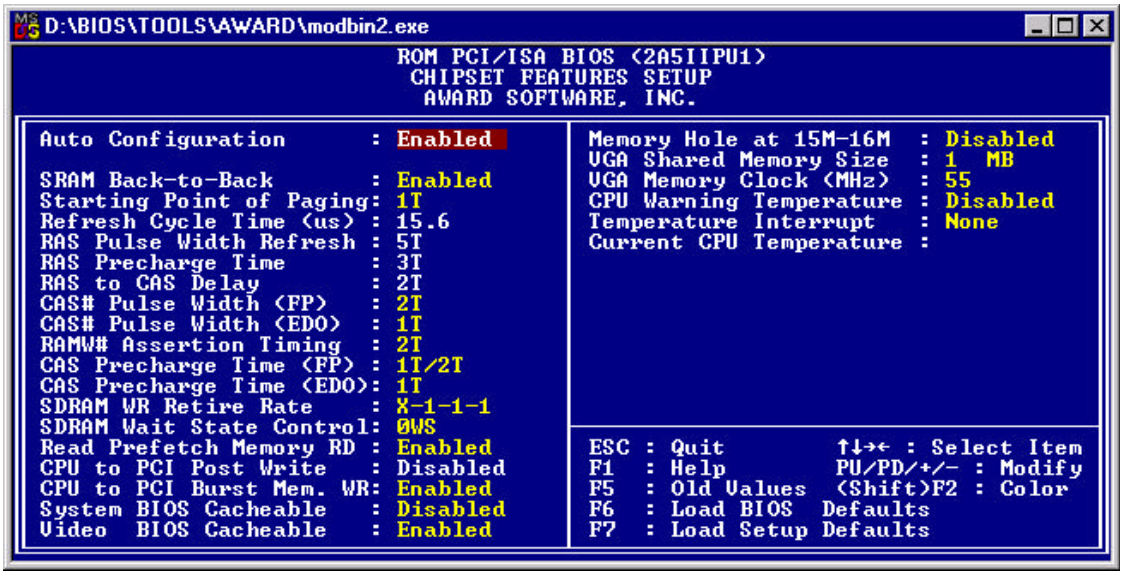
PEP Advantage

This section describes all the fields presented on this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Advanced Options

The parameters in this screen are for system designers, service personnel, and technically competent users only. Do not reset these values unless you understand the consequences of your changes.

Figure 5-5: Chipset Features Setup — Screen Display.



SDRAM Control by Manual / Auto

Auto Configuration selects predetermined optimal values for chipset parameters. When *Disabled*, chipset parameters revert to setup information stored in the CMOS. Many fields in this screen are not available when Auto Configuration is *Enabled*.

SDRAM RAS To CAS Delay

Select the RAS to CAS delay time. See Refresh Cycle Time for information about the Auto Configuration of this value.

SDRAM RAS Precharge Time

The precharge time is the number of cycles it takes for the RAS to accumulate its charge before DRAM refresh. If insufficient time is allowed, refresh may be incomplete and the DRAM may fail to retain data.

SDRAM CAS Latency Time

When synchronous DRAM is installed, you can control the number of CLK's between the SDRAM's sample of a read command and the time when the controller samples read data from the SDRAM's. Do not reset this field from the default value specified by the system designer.

SDRAM Precharge Control

When *Enabled*, all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface.

DRAM Data Integrity Mode

Select *Non-ECC* or *ECC* (error-correcting code), according to the type of installed DRAM.

System BIOS Cacheable

Selecting *Enabled* allows caching of the system BIOS ROM at 0xF0000 to 0xFFFFF, resulting in better system performance. However, if any program writes to this memory area, a memory access error may result.

Video BIOS Cacheable

Selecting *Enabled* allows caching of the video BIOS ROM at 0xC0000 to 0xC7FFF, resulting in better video performance. However, if any program writes to this memory area, a memory access error may result.

Video RAM Cacheable

Selecting *Enabled* allows caching of the video memory (RAM) at 0xA0000 to 0xAFFFF, resulting in better video performance. However, if any program writes to this memory area, a memory access error may result.

8/16-bit I/O Recovery Time

The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is so much faster than the ISA bus.

These two fields let you add recovery time (in bus clock cycles) for 16-bit and 8-bit I/O.

Memory Hole at 15M-16M

You can reserve this area of system memory for ISA adaptor ROM. When this area is reserved, it cannot be cached. The user information for peripherals that need to use this area of system memory usually discusses their memory requirements.

Passive Release

When *Enabled*, CPU to PCI bus accesses are allowed during passive release. Otherwise, the arbiter only accepts another PCI master access to local DRAM.

Delayed Transaction

The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select *Enabled* to support compliance with PCI specification version 2.1.

AGP Aperture Size (MB)

Select the size of the Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation. See http://www.agpforum.org for AGP information.

CPU Warning Temperature

Select the combination of lower and upper limits for CPU temperature, if your computer contains an environmental monitoring system. If the CPU temperature extends beyond either limit, any warning mechanism programmed into your application is activated.

Current CPU Temperature

This field displays the *current* CPU temperature, if your computer contains an environmental monitoring system.

Current CPU Fan 1

Monitors the on-board Fan mounted on the CPU heat sink, if available.

Current CPU Fan 2

Monitors the Fan signal routed to the rear I/O connector.

Voltage Monitor

Displays all onboard voltages for diagnostic purposes.

Shutdown Temperature

Select the combination of lower and upper limits for the system shutdown temperature, if your computer contains an environmental monitoring system. If the temperature extends beyond either limit, the system shuts down.

Recommendation for optimizing performance:

With only 64/128 MB onboard SDRAM is installed, use the following settings:

SDRAM RAS-to-CAS Delay: 2

SDRAM RAS Precharge Time: 2

SDRAM CAS latency Time: 2

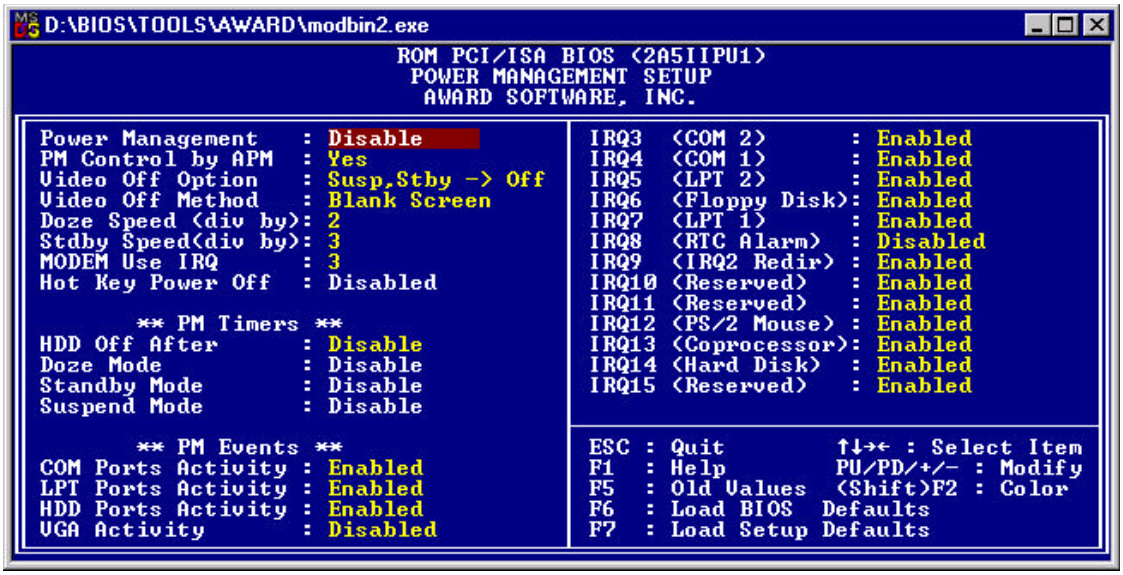
If additional RAM is installed in the SODIMM socket, automatic SDRAM Control is recommended.

5.7 Power Management

PEP Advantage

This section describes all fields presented on this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Figure 5-6: Power Management Setup — Screen Display.



ACPI Function

Select *Enabled* only if your computer's operating system supports the Advanced Configuration and Power Interface (ACPI) specification. Currently, Windows 98, Windows 2000 and Windows NT support ACPI.

Power Management

This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. See the section *PM Timers* for a brief description of each mode.

The following table describes each power management mode:

Table 5-7: Power Management Modes

Mode	Description
Max. Saving	Maximum power savings. **Only Available for SL CPU's**. Inactivity period is 1 minute in each mode.
User Defined	Sets each mode individually. Select time-out periods in the *PM Timers* section, which follows.
Min. Saving	Minimum power savings. Inactivity period is 1 hour in each mode (except the hard drive).

PM Control by APM

If Advanced Power Management (APM) is installed in your system, selecting *Yes* gives improved power savings.

Video-Off Method

Determines the manner in which the monitor is blanked.

Table 5-8: Video-Off Commands

V/H SYNC+Blank	System switches off vertical and horizontal synchronization ports and writes blanks to the video buffer.
DPMS Support	Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values.
Blank Screen	System writes blanks only to the video buffer.

Video-Off Option

This item determines the power management modes the monitor will enter before entering the Off-state as defined by the Video Off Method below. The Video Off Option moves from the low (doze) to the medium (standby) to high (suspend) power saving modes.

Modem Use IRQ

Name the interrupt request (IRQ) line assigned to the modem (if any) on your system. Activity by the selected IRQ always awakens the system.

5.8 PM Timers

The following modes are Green PC power saving functions. They are user-configurable only during User Defined Power Management mode.

Doze Mode

After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at a slower speed while all other devices still operate at full speed.

Stand-By Mode

After the selected period of system inactivity (1 minute to 1 hour), the fixed disk drive and the video shut down while all other devices still operate at full speed.

Suspend Mode

After the selected period of system inactivity (1 minute to 1 hour), all devices except the CPU shut down.

HDD Power Down

After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active.

Throttle Duty Cycle

When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of the time that the clock runs.

Soft-Off by PWR-BTTN

When you select *Instant Off* or *Delay 4 Sec*., turning the system off with the on/off button places the system in a very low power usage state, either immediately or after 4 seconds, with only enough circuitry receiving power to detect power button activity or Resume by Ring activity.

Power-on by Ring

When *Enabled*, an input signal on the serial Ring Indicator (RI) line (in other words, an incoming call on the modem) awakens the system from a soft off state.

Resume by Alarm

When *Enabled*, you can set the date and time at which the RTC (real-time clock) alarm awakens the system from suspend mode.

Date (of Month) Alarm

Select a date in the month when you want the alarm to go off.

Time (hh:mm:ss) Alarm

Set the time at which you want the alarm to go off.

IRQ8 Break (Event From) Suspend

You can select *Enabled* or *Disabled* for monitoring of IRQ8 (the Real Time Clock) so that it does not awaken the system from Suspend mode.

Reload Global Timer Events

When Enabled, an event occurring on each of the devices listed below restarts the global timer for Standby mode:

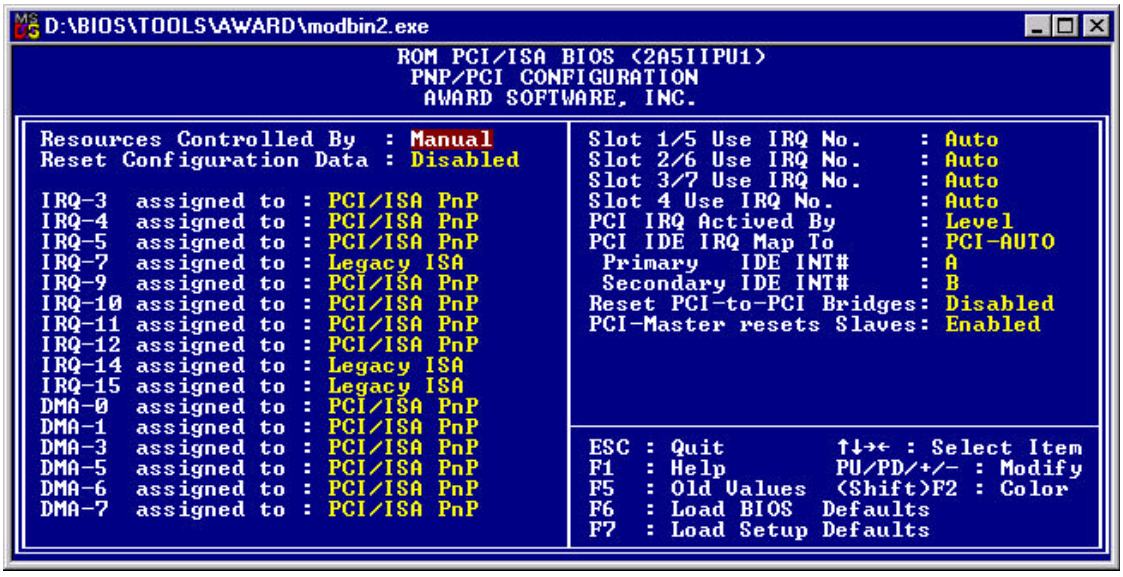
- IRQ§-7, 9-15, NM1,
- Primary IDE 0,
- Primary IDE 1,
- Secondary IDE 0,
- Secondary IDE 1,
- Floppy Disk,
- Serial Port,
- Parallel Port, and
- IRQ9 (IRQ2 Redir).

5.9 PNP/PCI Configuration

PEP Advantage

This section describes all the fields presented by this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Figure 5-7: PNP/PCI Configuration — Screen Display



PNP OS Installed

Select “Yes” if the system operating environment is PlugandPlay aware (e.g. Win 95).

Resources Controlled by

The Award PlugandPlay BIOS can automatically configure all the boot and PlugandPlay-compatible devices. If you select *Auto*, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

Reset Configuration Data

Normally this field is left *Disabled*. Select *Enabled* to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system re-configuration has caused such a serious conflict that the operating system cannot boot.

IRQ *n* Assigned to

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt.

Legacy ISA	Devices compliant with the original PC AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).
PCI/ISA PnP	Devices compliant with the PlugandPlay standard, whether designed for PCI or ISA bus architecture.

DMA *n* Assigned to

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt.

Legacy ISA	Devices compliant with the original PC AT bus specification, requiring a specific DMA channel
PCI/ISA PnP	Devices compliant with the PlugandPlay standard, whether designed for PCI or ISA bus architecture.

PCI IDE IRQ Map to

This field lets you select PCI IDE IRQ mapping or PC AT (ISA) interrupts. If your system does not have one or two PCI IDE connectors on the system board, select values according to the type of IDE interface(s) installed in your system (PCI or ISA). Standard ISA interrupts for IDE channels are IRQ14 for primary and IRQ15 for secondary.

Primary/Secondary IDE INT#

Each PCI peripheral connection is capable of activating up to four interrupts: *INT# A*, *INT# B*, *INT# C* and *INT# D*. By default, a PCI connection is assigned *INT# A*. Assigning *INT# B* has no meaning unless the peripheral device requires two interrupt services rather than just one. Because the PCI IDE interface in the chipset has two channels, it requires two interrupt services. The primary and secondary IDE INT# fields default to values appropriate for two PCI IDE channels, with the primary PCI IDE channel having a lower interrupt than the secondary.

Reset PCI-to-PCI Bridges

The BIOS may reset the PCI-to-PCI Bridges in the system using a software reset mechanism. Especially in conjunction with Hotswap compatible boards, it should be disabled. Default is disabled.

PCI Class Code FFh:

Some PCI boards generate a class code 0FFh. Although this code does not conform with the PCI standard, boards of this kind are distributed by some vendors.

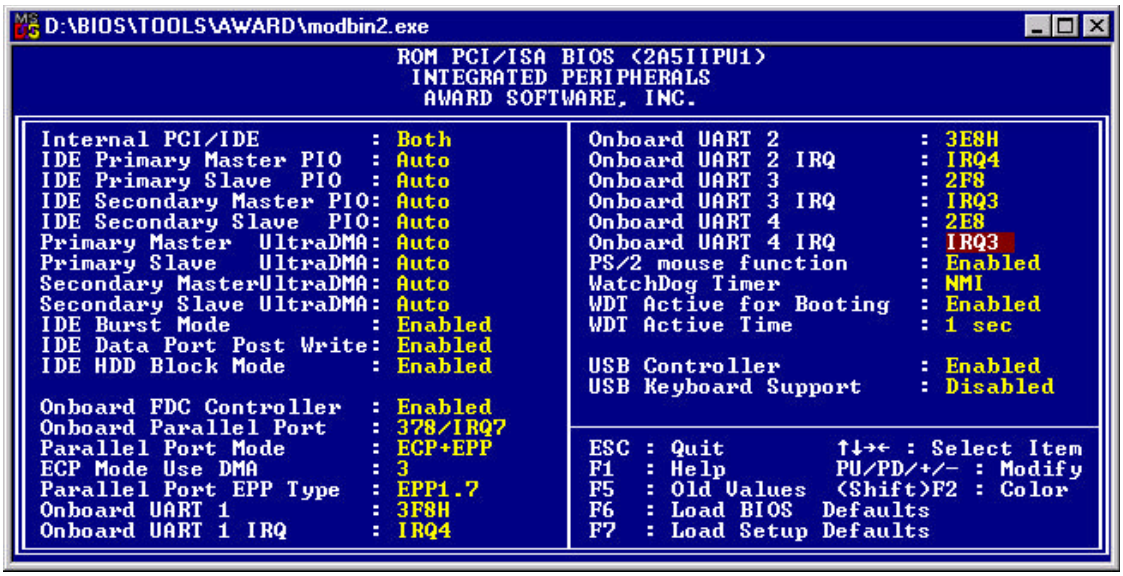
By setting this field to configure, these non-standard boards will be ignored
By setting this field to ignore, these non-standard boards will also be configured by the BIOS and made operable.

5.10 Integrated Peripherals

Important!

This section describes all the fields presented by Award Software in this screen display. Please note that your system board designer may omit or modify some fields.

Figure 5-8: Integrated Peripherals — Screen Display



PCI IDE 2nd Channel

Used to enable the 2nd PCI IDE interface

IDE HDD Block Mode

Select *Enabled* only if your hard drives support block mode.

IDE 32-bit Transfer Mode

Enables or disables 32-bit Data transfers.

On-Chip PCI IDE (Primary/Secondary)

The Intel® 82C440BX chipset contains a PCI IDE interface with support for two IDE channels. Select *Enabled* to activate the primary and/or secondary IDE interface. Select *Disabled* to deactivate this interface if you instal a primary and/or secondary add-in IDE interface.

IDE PIO Modes (Primary/Secondary Master/Slave)

The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of up to four IDE devices that the internal PCI IDE interface supports. Modes 0 through 4 provide successively increased performance. In *Auto* mode, the system automatically determines the best mode for each device.

IDE Primary/Secondary Master/Slave UDMA

UDMA (Ultra DMA) is a DMA data transfer protocol that utilizes ATA commands and the ATA bus to allow DMA commands to transfer data at a maximum burst rate of 33 MB/s. When you select *Auto* in the four IDE UDMA fields (for each of up to four IDE devices that the internal PCI IDE interface supports), the system automatically determines the optimal data transfer rate for each IDE device.

USB Keyboard Support

Select *Enabled* if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard.

Init Display First

Initialize the AGP video display before initializing any other display device on the system. Thus the AGP display becomes the primary display.

On-board FDC Controller

Select *Enabled* if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install an add-on FDC or the system has no floppy drive, select *Disabled* in this field.

On-board Serial Ports: 1, 2

Select a logical COM port address and corresponding interrupt for the first and second serial ports.

On-board Parallel Port

Select a logical LPT port address and corresponding interrupt for the physical parallel port.

Parallel Port Mode

Select an operating mode for the on-board parallel port. Select *Normal* unless you are certain that both your hardware and software support one of the other available modes.

ECP Mode Use DMA

Select a DMA channel for the parallel port for use during ECP mode.

Watchdog Timer

Select the watchdog routing.

WDT Active for Booting

Select *Enable* if the watchdog timer requires to be started before the operating system is booted from the BIOS.

WDT Active Time

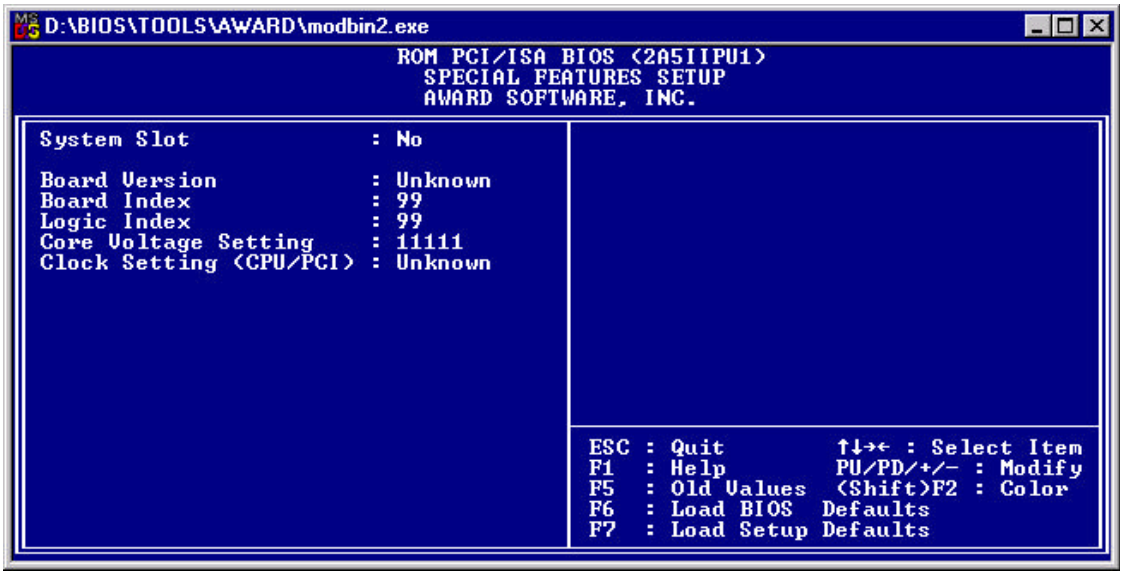
Select the time after which the action selected occurs, if the watchdog timer is not retriggered.

5.11 Special Setup Features

Important!

This section describes all the fields presented by Award Software in this screen display. Your system board designer may omit or modify some fields.

Figure 5-9: Special Features Setup — Screen Display



System Slot

This is a display only field. Yes indicates that this CPU is the system controller configuring the backplane and handling all interrupts relating to the backplane. No indicates that this CPU is a slave CPU.

Board Version

This is a display only field, which reflects the value of an on-board register. This must always correspond with the CPU on which the BIOS is installed.

Board Index

This is a display only field, which reflects the value of an on-board register. It shows the index of the hardware.

Logic Index

This is a display only field, which reflects the value of an on-board register. It shows the index of the on-board logic. When the Board Index is 00 this item is not displayed.

5.12 Password Setting

When you select this function, the following message appears at the center of the screen:

`Enter password:`

Type the password, up to eight characters in length, and press "↵". Typing a password clears any previously entered password from the CMOS memory.

After having pressed "↵" the message changes to:

`Confirm password:`

Type the password again and press "↵". To abort the process at any time, press "Esc".

In the "Security Option" item in the "BIOS Features Setup" screen, select `System` or `Setup`:

Table 5-9: Security Options

System	Enter a password each time the system boots and whenever you enter Setup.
Setup	Enter a password whenever you enter Setup.

Important!

To clear the password, simply press "↵" when asked to enter a password. Then the password function is disabled.

5.13 POST Messages

During the Power-on Self Test (POST), the BIOS displays a message whenever it detects a correctable error. Any error message is followed by this prompt:

```
Press “F1” to continue, “Ctrl-Alt-Esc” or “Del” to enter setup.
```

Following is a list of POST error messages for both the ISA and the EISA BIOS.

CMOS Battery Has Failed

The CMOS battery is no longer functional. It should be replaced.

CMOS Checksum Error

Checksum of CMOS is incorrect. This can indicate that the CMOS has become corrupted. This error may have been caused by a weak battery. Check the battery and replace it, if necessary.

Disk Boot Failure, Insert System Disk and Press Enter

No boot device was found. This could mean that either a boot drive was not detected or that the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

Diskette Drives or Types Mismatch Error - Run Setup

Type of floppy-disk drive installed in the system is different from the CMOS definition. Run “Setup” to reconfigure the drive type correctly.

Display Switch is Set Incorrectly

Display switch on the motherboard can be set to either monochrome or color. This error message indicates that the switch has a setting other than that indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

Display Type Has Changed Since Last Boot

Since the last powering-down of the system, the display adapter has been changed. You must configure the system for the new display type.

EISA Configuration Checksum Error - Please Run EISA Configuration Utility

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupted or the slot has been configured incorrectly. Ensure also that the card is installed firmly in the slot.

EISA Configuration Is Not Complete - Please Run EISA Configuration Utility

The slot configuration information stored in the EISA non-volatile memory is incomplete.

Note:

When either of the above EISA error messages appears, the system boots in ISA mode so that you can run the EISA Configuration Utility.

Error Encountered Initializing Hard-Drive

Hard drive cannot be initialized. Make sure that the adapter is installed correctly and that all cables are correctly and firmly attached. Ensure also that the correct hard drive type is selected in “Setup”.

Error Initializing Hard-Disk Controller

Cannot initialize controller. Make sure that the cord is correctly and firmly installed in the bus. Ensure also that the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

Floppy-Disk Controller Error or No Controller Present

Cannot find or initialize the floppy drive controller. Make sure that the controller is installed correctly and firmly. If there are no floppy drives installed, ensure that the floppy-disk drive selection in “Setup” is set to NONE.

Invalid EISA Configuration - Please Run EISA Configuration Utility

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupted. Re-run EISA configuration utility to correctly program the memory.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Keyboard Error or No Keyboard Present

Cannot initialize the keyboard. Make sure that the keyboard is attached correctly and that no keys are being pressed during the boot process.

If you are deliberately configuring the system without a keyboard, set the “Error Halt” condition in “Setup” to HALT ON ALL, BUT KEYBOARD. This causes the BIOS to ignore the missing keyboard and continue the boot process.

Memory Address Error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Parity Error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Size Has Changed Since Last Boot

Memory has been added or removed since the last boot. In EISA mode use the configuration utility to reconfigure the memory configuration. In ISA mode enter “Setup” and enter the new memory size into the memory fields.

Memory Verify Error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

Offending Address not Found

This message is used in conjunction with the “I/O Channel Check” and “RAM Parity Error” messages whenever the segment that has caused the problem cannot be isolated.

Offending Segment

This message is used in conjunction with the “I/O Channel Check” and “RAM Parity Error” messages whenever the segment that has caused the problem has been isolated.

Press a Key to Reboot

This message appears at the bottom of the screen when an error occurs that requires you to reboot. Press any key to reboot the system.

Press “F1” to Disable NMI, “F2” to Reboot

When the BIOS detects a non-maskable interrupt condition during boot, you can disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM Parity Error - Checking for Segment ...

Indicates a parity error in the random access memory.

Should Be Empty But EISA Board Found - Please Run EISA Configuration Utility

A valid board ID was found in a slot that was configured as having no board ID.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Should Have EISA Board but not Found - Please Run EISA Configuration Utility

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Slot not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

System Halted, <CTRL-ALT-DEL> to Reboot ...

Indicates that the present boot attempt has been aborted and that the system must be rebooted. Press and hold down the “CTRL” and “ALT” keys and press “DEL”.

Wrong Board in Slot - Please Run EISA Configuration Utility

The board ID does not match the ID stored in the EISA non-volatile memory.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

5.14 POST Codes

ISA and PCI POST codes are routed to port address 80H.

Table 5-10: Early POST Codes before System BIOS is Shadowed

POST Code	Action
Reset	RTC & KBC initialization
0CFh	Early CPU Detection
0C0h	Early Chipset initialization
0C1h	Memory presence test: detects memory modules and programs chipset accordingly
0C6h	L2 Cache sizing test
0C3h	Decompresses Bios
0C5h	Shadows Main Bios and jumps to POST

Table 5-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
03h	Set 40h, 72h to 1234h if it was a warm boot
04h	Reserved
05h	SuperIO early programming Clear Screen Initializes KBC
06h	Tests whether F000-Segment read/writeable Detects flash type
07h	Tests CMOS access If supported: Test if overide key (Insert) pressed during reset
08h 0BEh	-- Programs chipset defaults
09h	Reads CPU ID Cache initialization if necessary If supported: Restores CMOS from flash backup if required
0Ah	Initializes interrupt vectors Copies CMOS to stack If supported: Checks for dual processor

Table 5-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
0Bh	Detects Coprocessor Initializes Power Management chipset Updates CPU microcode if P6 CPU Reads existing ESCD Scans PCI devices and busses, assigns I/O and Memory to PCI devices Initializes Clock generator Initializes Hardware monitoring / temperature sensor
0Ch	Initializes keyboard buffer in BDA
0Dh 0BFh 0Dh	-- Program chipset Measures CPU core speed Initializes VGA video If VGA video not found: Checks for CGA If none found: Beepcode -..
0Eh	If CGA video found: Checks video memory If supported: Tries to init Award preboot agent If supported: Shows graphic logo, otherwise shows EPA logo If not full screen graphic logo, shows copyright message and CPU type and speed If ISA VGA video: Switches on ISA video ROM shadowing
0Fh	Tests DMA Channel 0
10h	Tests DMA Channel 1
11h	Tests DMA Page Registers
12h	--
13h	--
14h	Tests and init timer (8254)
15h	If not warm boot: tests MasterPIC mask register bits
16h	If not warm boot: tests SlavePIC mask register bits
17h	--
18h	Tests PIC’s by use of timer. Restores timer
19h	--
1Ah	--
1Bh	--
1Ch	--
1Dh	--
1Eh	--
30h	Measures total memory size

Table 5-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
31h	Initialize USB Tests all memory above 1MB, shows memory size
32h	Scans for ISA PnP devices, isolates and assigns CSN to ISA PnP devices Disables SuperIO COM/LPT ports Detects and records COM/LPT ports Programs Super IO according to setup and probably detected other COM/LPT ports Programs Audio system Initializes chipset IDE channels
33h	--
34h	--
35h	--
36h	--
37h	--
38h	--
39h	--
3Ah	--
3Bh	--
3Ch	Enables going to setup
3Dh	Installs PS/2 mouse if present If ACPI supported: checks for compressed ACPI table
3Eh	Attempts to enable L2 Cache
3Fh	--
40h	--
41h 0BFh	-- Programs chipset Chipset auto configuration if required SuperIO COM/LPT auto configuration if required Records system device nodes Assigns resources to ISA PnP devices Installs Floppy disk
42h	Installs IDE hard disk and ATAPI drives
43h	Checks and initializes COM/LPT ports
44h	--
45h	Initializes coprocessor
46h	--
47h	Saves boot_sector_buffer

Table 5-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
48h	--
49h	--
4Ah	--
4Bh	--
4Ch	--
4Dh	--
4Eh	Checks for USB keyboard Displays previously detected POST errors. If any, checks for "Halt on" condition setting and if necessary, waits for keys "F1" or "Del".
4Fh	Checks for password entry if necessary
50h	Saves CMOS values in stack back to CMOS
51h	Switches all ISA PnP devices into "Wait For Key" state
52h	USB final initialization Decompresses embedded PCI Option ROM's Assigns IRQ's to PCI devices Programs onboard SCSI if present and activated If ACPI supported: Decompresses and installs ACPI table Checks for and runs non-video option ROM's Switches on ISA option ROM shadowing Fetches and runs embedded SCSI Option ROM's Fetches and runs embedded ISA Option ROM's Disables unused shadow areas Releases lower 32KB of E000 Segment
53h	--
54h	--
55h	--
56h	--
57h	--
58h	--
59h	--
5Ah	--
5Bh	--
5Ch	--
5Dh	--
5Eh	--
5Fh	--

Table 5-11: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
60h	Prepares IDE/ATAPI/SCSI for boot
61h	Sets speed turbo/deturbo Final chipset initialization Final power management initialization Clears screen Shows system info
62h	Programs keyboard numlock/typerate
63h	Builds ESCD and saves ESCD in flash Checks for correct century in CMOS Setup timer tick in BDA Clears any pending keys in BDA Flushes cache Releases upper 32KB of E000 Segment if Award Preboot Agent not present and active
0FFh	Boot

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