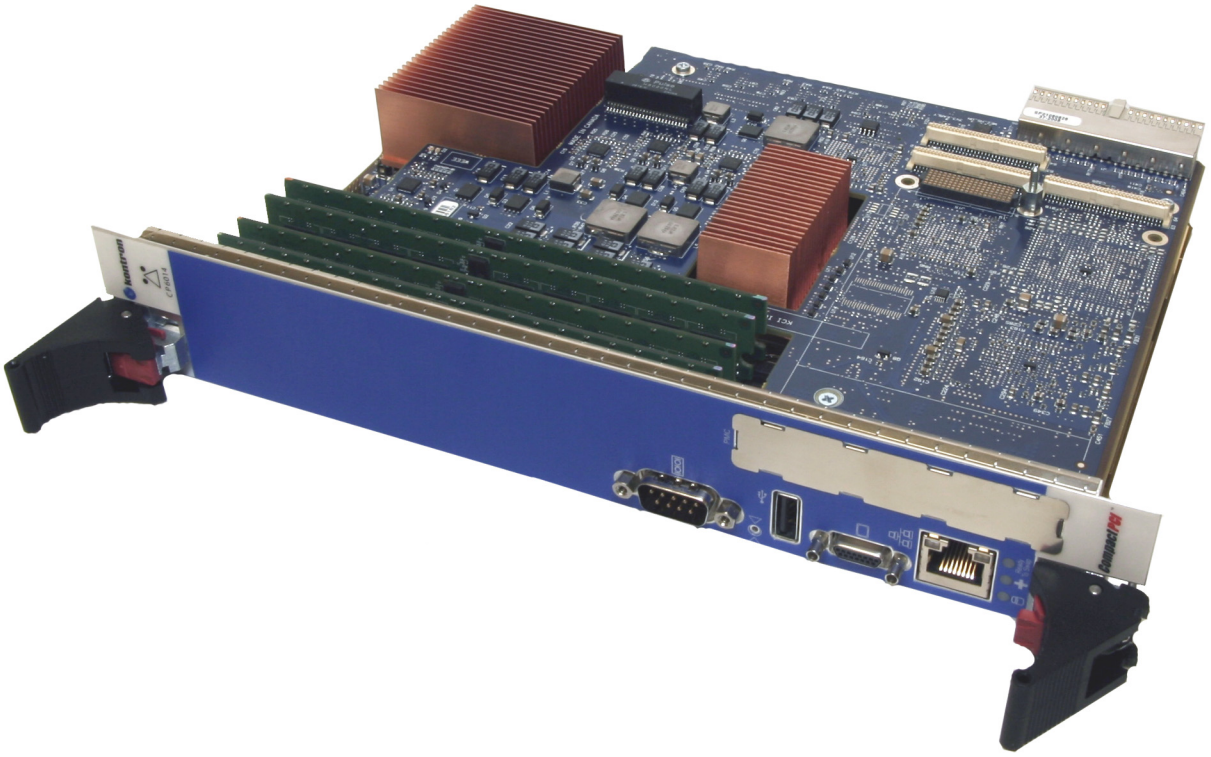
kontron

»Kontron User's Guide«

CompactPCI™



CP6014

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Safety Instructions

Before You Begin

Before handling the board, read the instructions and safety guidelines on the following pages to prevent damage to the product and to ensure your own personal safety. Refer to the "Advisories" section in the Preface for advisory conventions used in this user's guide, including the distinction between Warnings, Cautions, Important Notes, and Notes.

- Always use caution when handling/operating the computer. Only qualified, experienced, authorized electronics service personnel should access the interior of the computer. The power supplies produce high voltages and energy hazards, which can cause bodily harm.
- Use extreme caution when installing or removing components. Refer to the installation instructions in this user's guide for precautions and procedures. If you have any questions, please contact Kontron Technical Support

WARNING

High voltages are present inside the chassis when the unit's power cord is plugged into an electrical outlet. Turn off system power, turn off the power supply, and then disconnect the power cord from its source before removing the chassis cover. Turning off the system power switch does not remove power to components.

Preventing Electrostatic Discharge

Static electricity can harm system boards. Perform service at an ESD workstation and follow proper ESD procedure to reduce the risk of damage to components. Kontron strongly encourages you to follow proper ESD procedure, which can include wrist straps and smocks, when servicing equipment.

Take the following steps to prevent damage from electrostatic discharge (ESD):

- When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the component in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This will discharge any static electricity that may have built up in your body.
- When transporting a sensitive component, first place it in an antistatic container or packaging.
- Handle all sensitive components at an ESD workstation. If possible, use antistatic floor pads and workbench pads.
- Handle components and boards with care. Don't touch the components or contacts on a board. Hold a board by its edges or by its metal mounting bracket.
- Do not handle or store system boards near strong electrostatic, electromagnetic, magnetic, or radioactive fields.
- When you want to remove the protective foil (if present), make sure you are properly grounded and that you touch a metalic part of the board.

CAUTION

The back cover offers only a mechanical protection of the bottom components. The board should always be manipulated following proper ESD practices to avoid damages caused by static discharge

Working with Batteries

Care and Handling Precautions for Lithium Batteries

Your computer board has a standard, nonrechargeable lithium battery.

- Do not short circuit
- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Always observe proper polarities

Replacing Lithium Batteries

Exercise caution while replacing lithium batteries!

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries, following manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel. Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Puede explotar si la pila no este bien reemplazada. Solo reemplazca la pila con tipas equivalentes segun las instrucciones del manifacturo. Vote las pilas usads segun las instrucciones del manifacturo.

Preface

How to Use This Guide

This user's guide is designed to be used as step-by-step instructions for installation, and as a reference for operation, troubleshooting, and upgrades.

For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

The following is a summary of chapter contents:

- Chapter 1, Product Description
- Chapter 2, Board Features
- Chapter 3, Installing the board
- Chapter 4, Integrated Switch Setup
- Chapter 5, Software Setup
- Appendix A, Memory & I/O Maps
- Appendix B, Extension Registers
- Appendix C, Connector Pinout
- Appendix D, BIOS Setup Error Codes
- Appendix E, Software Update
- Appendix F, Getting Help
- Appendix G, Glossary

Customer Comments

If you have any difficulties using this user's guide, discover an error, or just want to provide some feedback, please send a message to: Tech.Writer@ca.kontron.com. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user's guide on our Web site. Thank you.

Advisory Conventions

Seven types of advisories are used throughout the user guides to provide helpful information or to alert you to the potential for hardware damage or personal injury. They are Note, Signal Paths, Jumpers Settings, BIOS Settings, Software Usage, Cautions, and Warnings. The following is an example of each type of advisory. Use caution when servicing electrical components.

Note:
Indicate information that is important for you to know.

Signal Path:
Indicate the places where you can find the signal on the board.

Jumper Settings:
Indicate the jumpers that are related to this sections.

BIOS Settings:
Indicate where you can set this option in the BIOS.

Software Usage:
Indicates how you can access this feature through software.

CAUTION
Indicate potential damage to hardware and tells you how to avoid the problem.

WARNING
Indicates potential for bodily harm and tells you how to avoid the problem.

ESD Sensitive Device:
This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.
Please read also the section "Special Handling and Unpacking Instructions".

CE Conformity:
This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section "Regulatory Compliance Statements" in this manual.

Disclaimer: We have tried to identify all situations that may pose a warning or a caution condition in this user's guide. However, Kontron does not claim to have covered all situations that might require the use of a Caution or a Warning.

Unpacking

Follow these recommendations while unpacking:

- Remove all items from the box. If any items listed on the purchase order are missing, notify Kontron customer service immediately.
- Inspect the product for damage. If there is damage, notify Kontron customer service immediately.
- Save the box and packing material for possible future shipment.

Powering Up the System

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

If you encounter a problem, verify the following items:

- Make sure that all connectors are properly connected.
- Verify your boot devices.
- If the system does not start properly, try booting without any other I/O peripherals attached.

Make sure your system provides the minimum DC voltages required at the board's slot, especially if DC power is carried by cables.

If you are still not able to get your board running, contact our Technical Support for assistance.

Adapter Cables

Because adapter cables come from various manufacturers, pinouts can differ. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

Storing Boards

Electronic boards are sensitive devices. Do not handle or store device near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Regulatory Compliance Statements

FCC Compliance Statement for Class B Devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generated, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experience radio/TV technician for help.

WARNING

This is a Class B product. If not installed in a properly shielded enclosure and used in accordance with this User's Guide, this product may cause radio interference in which case users may need to take additional measures at their own expense.

Safety Certification

All Kontron equipment meets or exceeds safety requirements based on the IEC/EN/UL/CSA 60950-1 family of standards entitled, "Safety of information technology equipment." All components are chosen to reduce fire hazards and provide insulation and protection where necessary. Testing and reports when required are performed under the international IECEE CB Scheme. Please consult the "Kontron Safety Conformity Policy Guide" for more information. For Canada and USA input voltage must not exceed -60Vdc for safety compliance.

CE Certification

The product(s) described in this user's guide complies with all applicable European Union (CE) directives if it has a CE marking. For computer systems to remain CE compliant, only CE-compliant parts may be used. Maintaining CE compliance also requires proper cable and cabling techniques. Although Kontron offers accessories, the customer must ensure that these products are installed with proper shielding to maintain CE compliance. Kontron does not offer engineering services for designing cabling systems. In addition, Kontron will not retest or recertify systems or components that have been reconfigured by customers.

Limited Warranty

Kontron grants the original purchaser of Kontron's products a TWO YEAR LIMITED HARDWARE WARRANTY as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron.

Kontron warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long- term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than Kontron or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

Kontron provides for repair or replacement of any part, assembly or sub-assembly at their own discretion, or to refund the original cost of purchase, if appropriate. In the event of repair, refunding or replacement of any part, the ownership of the removed or replaced parts reverts to Kontron, and the remaining part of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" issued by Kontron with the repaired or replaced item.

Kontron will not accept liability for any further claims resulting directly or indirectly from any warranty claim, other than the above specified repair, replacement or refunding. In particular, all claims for damage to any system or process in which the product was employed, or any loss incurred as a result of the product not functioning at any given time, are excluded. The extent of Kontron liability to the customer shall not exceed the original purchase price of the item for which the claim exists.

Kontron issues no warranty or representation, either explicit or implicit, with respect to its products reliability, fitness, quality, marketability or ability to fulfil any particular application or purpose. As a result, the products are sold "as is," and the responsibility to ensure their suitability for any given task remains that of the purchaser. In no event will Kontron be liable for direct, indirect or consequential damages resulting from the use of our hardware or software products, or documentation, even if Kontron were advised of the possibility of such claims prior to the purchase of the product or during any period since the date of its purchase.

Please remember that no Kontron employee, dealer or agent is authorized to make any modification or addition to the above specified terms, either verbally or in any other form, written or electronically transmitted, without the company's consent.

Chapter 1

Product Description

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1. Product Description

1.1 Product Overview

The CP6014 is a highly integrated, high performance 8HP (Dual slot) 6U CompactPCI CPU board incorporating leading-edge technology with a high performance processor and an appropriate chipset (“server” throughput) to take advantage of the processor performance.

Features include:

- High performance embedded processor – Xeon Dual Core and Xeon Quad Core
- Intel® 5100 MCH – server-performance chipset
- Highly integrated I/O hub - ICH9R

New technology compared to previous 6U Dual CPUs are:

- Dual / Quad Core technology
- DDR2 667 MHz Memory
- XMC support
- Local PCIExpress bus

1.2 What’s Included

This board is shipped with the following items:

- One CP6014 board
- One PMC gap filler
- One Video Adaptor cable (1015-9396)
- Cables that have been ordered

If any item is missing or damaged, contact the supplier.

1.3 Board Specifications

Table 1-1:Board Specifications

Features	Description
Processors	• Intel® Dual-Core LV5138 with 4MB on-die L2 cache • Intel® Quad-Core L5408 with 12MB (2x6MB) on-die L2 cache • Passive heatsink
Chipset	• Intel® 5100 MCH chipset & Intel® I/O Controller Hub 9R
Bus Interfaces	• Front Side bus of 1066MHz
Expansion Slots	• XMC/PMC • Local PCI-X 64-bit / 133MHz on PMC-slot or a PCIExpress X4 on the XMC
System Memory	• Supports up to 32GB DDR2 memory (4 DIMMs sockets) at 667MHz • IOAT (I/O Acceleration Technology) DMA for fast data transfer
CompactPCI Bus interface	• System bridge or stand alone operation • PCI 64/66 MHz; VIO 3.3V or 5V
Flash Memory	• Solid State Drive Module (SSD) available in different sizes
I/O Connectors	• 1x 10/100/1000 Front and 2x 10/100/1000 available through the rear I/O or PICMG 2.16 • Three USB 2.0 ports (one at front and two at rear I/O) • VGA controller to support CRT on Front (VGA mini DSub15 connector) or Rear • 2 SATA on Rear I/O • 1 x COM port front and rear; or two COM ports at rear
BIOS Features	• Recovery Boot Block Flash BIOS. • Field-updateable BIOS for Linux OS • LAN Boot (flexible use of PXE-Boot or EtherBoot) • Video-less operation • Quick boot support (fast memory initialization of <5-7sec) • Parameter saving in non-volatile RAM • Support of Ethernet all speed grades (LAN Boot, front IO, rear IO) • Support of Watchdog (with dual stage NMI/Reset; with logging of reset origin.), • Support of USB (USB2.0: Keyboard, Mouse, Floppy, CD-ROM, HDD) • Support of Serial Ports (RS232, serial console redirection) • Support of VGA (CRT) • Support of the onboard RTC • Support of Boot Devices (generic USB device, USB-Flash drive, USB-memory stick, LAN, SATA Devices) • Setup console redirection to serial port (VT100 mode) with CMOS setup access • IO-APIC integration (required for Linux), ACPI-compliant
IPMI Features	• Extensive Management Controller compliant to IPMI v1.5, PICMG 2.9 and design to meet PICMG 2.50 • Standard IPMI Watchdog (with pre-timeout interrupt) with reset/power cycle action • Standard IPMI host interface (interrupt driven KCS interface) • Serial over LAN (provides LAN access to BIOS menu) and IPMI over LAN (provides remote control such as power down/cycle) • Extensive sensors monitoring and external IPMB event generation on threshold, including overheat alarms • Standard IPMI System Even Log (SEL) for external or internal events • IPMI firmware is field updatable with fail safe rollover capability compliant to PICMG HPM.1 • Redundant IPMB communication path using cPCI IPMB1

Features	Description
Board Specifications	• PICMG2.0R3.0 (core specification) • PICMG2.1R2.0 (hot swap specification) • PICMG2.9R1.0 (system management) • PICMG2.10R1.0 (keying of CPCI boards) • PICMG2.16R1.0 (packet switching) • PICMG 2.50 vD0.8 (cTCA specification)
OS Compatibility	• Red Hat Enterprise Linux 5 • Windows Server 2003 • Other OS available on request
Mechanical	• 266.7 x 160 x 41 mm / 10.5 x 6.3 x 1.6 in, 6U x 8HP (dual slot) • Weight: 1,24 kg / 2,75 lbs • Conforms with PICMG2.0R3.0
Power Requirements	• 5 V CPU: LV5138 Idle: 5A / 25W Max: 16A / 80W • 5 V CPU: L5408 Idle: 5A / 25W Max: 22A / 110W • 3.3V CPU: Any 4x1GB Idle: 11A / 36.3W Max: 14A / 46.2W • 3.3V CPU: Any 4x2GB Idle: 13A / 42.9W Max: 16.8A / 55.5W • 3.3V CPU: Any 4x4GB Idle: 15,2A / 50.2W Max: 18.8A / 62W • 3.3V CPU: Any 4x8GB Idle: 15,3A / 50.5W Max: 19.4A / 64W Note: These 5V absolute maximum values are obtained using Maxpower, but should be considered impossible to attain in real-life applications. A more realistic maximum should be estimated to be at 80% of these values. Any additional SATA HDD adds 1.5A on 5V (7.5W).
Environmental Temperature	• Operating: 0-55°C/32-131°F with 27,5 CFM/400LFM airflow • Storage and Transit: -40 to +70°C/-40 to 158°F
Environmental Humidity	• Operating: 5% to 93% @40°C/104°F non-condensing • Storage and Transit: 5% to 95% @ 40°C/104°F non-condensing
Environmental Altitude*	• Operating: 4,000 m / 13,123 ft • Storage and Transit: 15,000 m / 49,212 ft
Environmental Shock	• Operating: 3G each axis • Storage and Transit: 18G each axis
Environmental Vibration	• Operating: 5-200Hz. 0.2G, each axis • Storage and Transit: 5 Hz to 20 Hz @ 1 m2/s3 (0.01 g2 /Hz) (flat) 20 Hz to 200 Hz @ -3 dB/oct (slop down)
Safety / EMC*	• Safety: CE Mark to EN 60950-1:2001. Meets or exceeds IEC60950-1,UL 60950-1/CSA C22.2 No 60950-1-07. • Designed to meet GR-1089-CORE • EMI/EMC: FCC 47 CFR Part 15, Class B; CE Mark to EN55022/EN55024/EN300386

* Designed to meet or exceed

1.4 Compliance

This product conforms to the following specifications:

- PICMG2.0R3.0 (core specification)
- PICMG2.1R2.0 (hot swap specification)
- PICMG2.9R1.0 (system management)
- PICMG2.10R1.0 (keying of CPCI boards)
- PICMG2.16R1.0 (packet switching)
- PICMG 2.50 vD0.8 (cTCA specification)

1.5 Hot-Plug Capability

The CP6014 supports Full Hot Plug capability as per PICMG3.0R2.0 ECN001 & ECN 002. It can be removed from or installed in the system while it is on (without powering-down the system). Please refer to the PICMG2.1R2.0 specification for additional details.

1.6 Interfacing with the Environment

1.6.1 Rear I/O

The RTM-CP6014 is a single slot (8HP) cPCI Rear I/O. This module provides additional connectivity for CP6014 CPU front blade.

1.6.1.1 Serial Port Feature

- Two serial ports available on the rear I/O face plate through two DB9 connectors. COM1 is available either on the CP6014 or on the Rear I/O.
- RS-232 signal levels at rear I/O face plate connector.
- Serial port speed capability is: 9.6kbits/s to 115.2kbits/s.

1.6.1.2 Video Features

- One DB15 video connector available on the rear I/O face plate.

1.6.1.3 Ethernet Connections

- Two Gigabyte Ethernet connections on the rear I/O face plate through two RJ-45 connectors (These Rear I/O ports are not available when using a PICMG 2.16 chassis).

1.6.1.4 USB

- Two USB 2.0 connectors available on the rear I/O face plate.

1.6.2 Mezzanine

The CP6014 has one PMC/XMC bay. Using a mezzanine allows to add I/O not provided on board. Only a PMC or an XMC mezzanine can be used at the time.

1.6.2.1 PMC Expansion

The PMC bay provides a local PCI-X 64bit/133MHz expansion.

1.6.2.2 XMC Expansion

The XMC bay provides a local PCIExpress x4 expansion.

Chapter 2

Board Features

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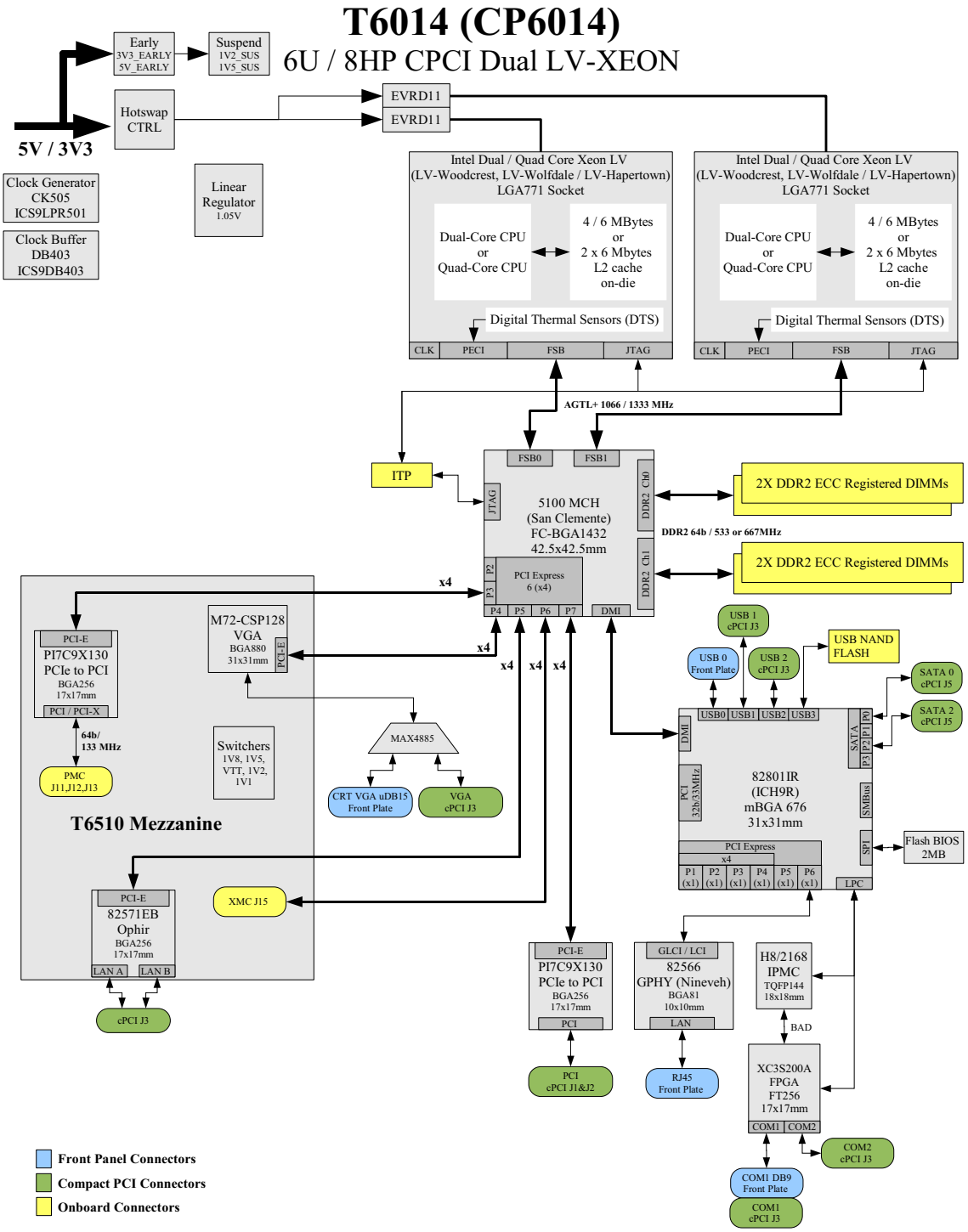
2. Board Features

2.1 Block Diagram

Figure 2-1:Block Diagram



2.2 System Core

2.2.1 Processors

The CP6014 supports the Intel® Dual-Core LV 5138 and the Intel® Quad-Core L5408 processors. Processors main features are described below.

2.2.1.1 Intel® Dual-Core LV 5138 CPU main features

- Dual-Core processing with Intel Core microarchitecture
- Processor core speeds of 2.13Ghz based on 65nm technology
- AGTL+ signaled 1066 MHz FSB speed, offering 8.5 GBytes/s data transfers rates respectively.
- On-Die 32-KB Level 1 instruction and 32-KB Level 1 data Cache per core
- On-Die 4-MB Level 2 Cache shared between cores, with Advanced Transfer Cache Architecture
- Socketed FC-LGA package with 771 lands which includes an integrated heat spreader (IHS)
- Platform Environmental Control Interface (PECI) to monitor processor's internal digital thermometer
- Advanced Dynamic Execution, Streaming SIMD Extensions 2 (SSE2) and Streaming SIMD Extensions 3 (SSE3).
- Intel Virtualization Technology
- Intel 64 Technology

2.2.1.2 Intel® Quad-Core L5408 CPU main features

- Quad-Core processing with Intel Core microarchitecture
- Processor core speeds of 2.13Ghz based on 45nm technology
- AGTL+ signaled 1066 MHz FSB speed, offering 8.5 GBytes/s data transfers rates respectively.
- On-Die 32-KB Level 1 instruction and 32-KB Level 1 data Cache per core
- On-Die 12-MB(2 x 6MB) Level 2 Cache with Advanced Transfer Cache Architecture
- Socketed FC-LGA package with 771 lands which includes an integrated heat spreader (IHS)
- Platform Environmental Control Interface (PECI) to monitor processor's internal digital thermometer
- Advanced Dynamic Execution, Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3), and Streaming SIMD Extensions 4.1 (SSE4.1).
- Intel Virtualization Technology
- Intel 64 Technology

2.2.2 Intel 5100 Chipset

The chipset used on the CP6014 is the Intel 5100 Chipset. This chipset contains two main components, the 5100 Memory controller Hub(MCH) and the ICH9R I/O Controller Hub(ICH).

2.2.2.1 MCH Description

The MCH used is the 5100 MCH. It is designed for systems based on the Dual-Core Intel Xeon processor 5100, Quad-Core Intel Xeon 5400 processor series. Main features used on the CP6014 are the following:

- Supports 2 processors on dual independent point-to-point FSB operating at 266MHz(1066MT/s) or 333MHz(1333MT/s).
- Supports 2 DDR2 memory channels, running at 667Mhz and supporting up to 32GB of ECC memory.
- Provides 6 x4 PCIe(PCI Express) bus interfaces to : Intel 82571EB, 2 PCIe-PCI bridges (to CPCI and PMC), XMC, VGA controller
- Provides 1 x4 lane Direct Media Interface (DMI) to the ICH9R.
- 2 SMBus interfaces for system management: one for Serial Presence Detect of DIMMs, one as slave device on ICH SMBus

2.2.2.2 ICH Description

The ICH used is the ICH9R which provides extensive I/O support on the CP6014. The main features used on the CP6014 are the following:

- Provides a Low Pin Count Interface (LPC) : acts as master
- 1 x4 lane Direct Media Interface (DMI) to the MCH
- 2 USB 2.0 EHCI supporting 3 external USB 2.0 ports (1 on front plate and 2 on rear I/O) and 1 to an internal flash disk device.
- Enhanced DMA controller
- 2 SATA ports with a data transfer rate up to 3.0Gb/s on rear I/O
- 1 Integrated Gigabit Lan Controller with Gigabit Lan Connect Interface (GLCI) : connected to the GPHY for front plate GbE connectivity
- 1 Platform Environmental Control Interface (PECI) for thermal monitoring of 1 CPU
- SMBus interface: master connected to CK505, DB403, MCH and CMOS EEPROM slaves.
- Firmware Hub interface supports up to 8MBytes BIOS memory size for mezzanine BIOS
- 4-pin Serial Peripheral Interface (SPI) to a 16 MBytes SPI flash, clocked at 33MHz, used in descriptor mode
- 32KHz clock generator (SUSCLK) used to clock early FPGA logic

2.3 Serial ATA (SATA)

The CP6014 has two SATA ports. They are integrated in the Intel ICH9R and available only on the rear I/O connector.

Main features of the controller are listed below.

- Supports SATA data transfers of 1.5Gbit/s
- Supports SATA data transfers of 3Gbit/s

BIOS Settings:
Advanced --> Drive Configuration

2.4 Onboard Flash Storage

The flash disk is a USB Flash solid-state disk module. It is socketed on 2x5 header attached to the CP6014 PCB and is connected to USB 2.0 port (#3) of the ICH9.

The flash disk is located on the baseboard, under the mezzanine, near the baseboard edge in order to allow an easy access for the end user. For details on how to install it, consult section 3.

The board includes a USB mass storage controller. The BIOS supports this as a boot device. This device is available for any OS that supports the standard USB mass storage interface.

2.5 USB 2.0 Interfaces

The CP6014 embeds a USB controller. This controller is compliant to USB 2.0. A USB connector is available on the frontpanel and two are available through the J3 rear I/O connector.

USB features include:

- Capability to daisy chain devices
- Fast bi-directional
- Isochronous/asynchronous interface
- 480 Mbs transfer rate
- Retro compatible with USB 1.1 devices

USB supports Plug and Play and hot-swapping operations (OS level). These features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.

Table 2-1:USB Connector Pinouts

Pin	Signal
1	VCC
2	DATA-
3	DATA+
4	GND

Signal Path:
- 2 USB 2.0 on rear I/O connector (J3)
- 1 USB 2.0 on front panel (J13)

BIOS Settings:
Advanced --> USB Configuration

2.6 Ethernet Interfaces

2.6.1 i82571EB Ethernet Controller

The onboard GbE controller is the Intel 82571EB. It connects to the MCH with a PCIe x4 interface and to the J3 backplane connector with two 10/100/1000Base-T interfaces.

The main features/capabilities of the Intel 82571EB used for this design are:

- Auto-negotiation support
- PCIe x4 connection to MCH
- Integrated PHY for 10/100/1000 Mbps operation
- Checksum offloading
- Packet filtering (RMCP/RMCP+ filtering)
- VLAN support
- 1 Fast Management Link to IPMC registers via FPGA
- Activity and link indicator outputs to J3
- Supports jumbo frames up to 9KBytes.

The CP6014 has boot from LAN capability (PXE and Etherboot) on these ports. Enable the option from the BIOS Setup menu. Please refer to Section 5.1, AMI BIOS Set-up menu.

BIOS Settings:
Advanced --> On-Board Devices Configurations --> Ethernet LAN0 Expansion ROM
Advanced --> On-Board Devices Configurations --> Ethernet LAN1 Expansion ROM

WARNING
When using a 2.16 backplane, the two ethernet ports on the rear I/O will not work.

2.6.2 i82566 Ethernet Controller

The front plate ethernet controller is the 82566 Gigabit Platform LAN Connect. It connects to the ICH9 using the GLCI/LCI link.

The main features of the GPHY used are:

- 10/100/1000Mb connectivity
- GLCI/LCI
- LED outputs
- Auto-negotiation support

Signal Path:
The Ethernet Management RJ45 connector is on the faceplate.

BIOS Settings:
Advanced --> On-Board Devices Configurations --> Front plate LAN Expansion ROM

2.7 Serial Ports

The UART has two serial ports, COM1 and COM2. COM1 is connected to the front plate DB9 connector and to the cPCI J3. COM2 is only available on cPCI J3.

Both serial ports support hardware flow control and FIFO mode. Maximum FIFO size for each direction is 16 bytes on each port. Supported transfer rates are 9.6 Kbps, 19.2 Kbps, 38.4 Kbps, 57.6 Kbps and115.2Kbps.

Each serial port is specified as follows:

Table 2-2:Serial Ports Output Path

Designation	Communication Mode	Output Path
COM1	RS-232	Front plate serial port, rear I/O serial port A, IPMI firmware upgrade, serial over LAN
COM2	RS-232	Rear I/O serial port B

Note:
Both COM1 connectors are enabled at the same time; make sure both ports are not used simultaneously by two different devices.

UART registers are individually addressable and fully programmable.

2.7.1 COM1 (J12)

The serial port is connected to the FPGA that demuxes the signals to the ICH (via LPC bus and standard register set for serial ports) and to the IPMC (via dedicated signals). The COM1 is also available on J3 backplane connector. This port can be used as a console for field upgrade, management and debug. When no cable is connected into any COM1 connector, the console information can be redirected to a remote location using "Serial-Over-LAN"

Table 2-3:Serial Port Pinout

Pin	Signal
1	DCD#
2	RXD
3	TXD
4	DTR#
5	GND
6	DSR#
7	RTS#
8	CTS#
9	RI#

Signal Path:
The COM1 signals are always available in front access through J12 or through the IPMC.

BIOS Settings:
Advanced --> Remote Access Configuration

2.7.2 COM2

The Serial port 2 is connected to the rear I/O and is exclusively used by CPU applications. It can be configured as the console redirection port in BIOS settings; default is set to COM1.

BIOS Settings:
Advanced --> Remote Access Configuration

2.8 Video Interface

The video graphic adapter (VGA) located on the mezzanine provides video functionalities for the baseboard. The ATI RADEON E2400 device from AMD is used for that application.

It is a high-performance PCI Express visual processing unit. This device has 128MB of memory integrated in the package, so there is no need for external video memory.

The video controller is connected to MCH PCI-E x4 Port 4, located on the baseboard.

The video support is available to the end user through a micro DB-15 connector located on the baseboard faceplate or through the rear I/O via a regular DB-15 connector. The end user can connect a monitor for his 2D and 3D graphics applications.

Signal Path:
Video signals are available through J6 (Front panel connector) or from Rear I/O connector. The default output is on the rear I/O when present.

BIOS Settings:
Advanced --> On-board Devices Configuration --> On-board video output

Software Usage:
For optimal performances, when using Windows 2003, make sure video acceleration has been set to max.To set it, do: right click on the desktop, click on properties, go in Settings tab, click on Advanced button, go in Troubleshoot tab and slide the hardware acceleration to max.

2.8.1 Supported Resolutions

The maximum video resolution and performance depend directly on the drivers running with your software application. Resolution and number of colors specification are listed below:

Table 2-4:Supported Video Resolutions

Resolution	Number of Colors	Frequencies
800x600, 1024x768, 1280x1024, 1600x1200	16 bits	60, 75 & 85 Hz
800x600, 1024x768, 1280x1024, 1600x1200	32 bits	60, 75 & 85 Hz

2.8.2 Major Features Description

2.8.2.1 2D Graphics Engine

The 2D graphics engine is an advanced 32-bit, three-operand engine that accelerates BitBLTs as line draws, polygon draw, and polygon fill. The 2D graphics engine also performs video and bitmap scaling, and data overlay.

2.9 XMC Interface

The mezzanine has all the connections to support the following type of XMC:

- Single slot
- Single width

The XMC interface includes all the I/O signals according to VITA 42.0 and VITA 42.3 specification. The interface includes only the primary XMC connector (J15). The XMC connector is directly connected to the MCH PCI-E x4 Port 6, located on the baseboard.

2.10 PMC Interface

The mezzanine has all the connections to support the following type of PMC:

- Single slot
- Single width
- VIO 3.3V

The PMC interface includes all the I/O signals according to PICMG 2.3 R1.0 specification. The interface includes three (3) connectors: J11, J12 and J13 are for PCI interface.

The PCI interface (J11, J12 and J13) is provided by a PCI-Express to PCI bridge located on the mezzanine. The PCI bus connected to the PMC slot is a 64-bit PCI/PCI-X bus. The bus speed supported can be up to 133 MHz (PCI-X).

2.11 Real Time Clock

The CP6014 uses the ICH9R to implement the real time clock (RTC). The ICH9R contains a RTC with 256 bytes of battery-backed SRAM. The internal RTC module keeps date and time, and stores system data in its RAM when the system is powered down. An external 32.768 kHz crystal is connected to the ICH9R RTC internal module.

2.12 FPGA

The FPGA has many functions. One of them is to act as a companion chip to the IPMC. The states of all the critical signals controlled by the IPMC are memorized in the FPGA and are preserved while the IPMC firmware is being updated.

The FPGA is a RAM-based chip that is preloaded from a separate flash memory at power-up. Two such flash memory devices are provided; one that can only be programmed in factory and the other one that can be updated in the field. The factory flash is selected by inserting jumper JP2 pins 5-6. Field update leads to an automated power cycle of all non-early powers.

The appropriate procedure to upgrade the FPGA will be provided with the update code when needed.

2.13 Redundant IPMC/MMC Firmware & BootBlock

The IPMC/MMC runs a firmware from its internal 512KB flash. The BootBlock manager keeps the last two copies of the IPMC/MMC firmware in dedicated flash memories. It acts as a watchdog to the IPMC/MMC and can rollback a firmware update in the IPMC/MMC in case of problems.

Note:
The IPMC/MMC has an internal hardware watchdog.

Chapter 3

Installing the Board

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3. Installing the Board

3.1 Setting Jumpers

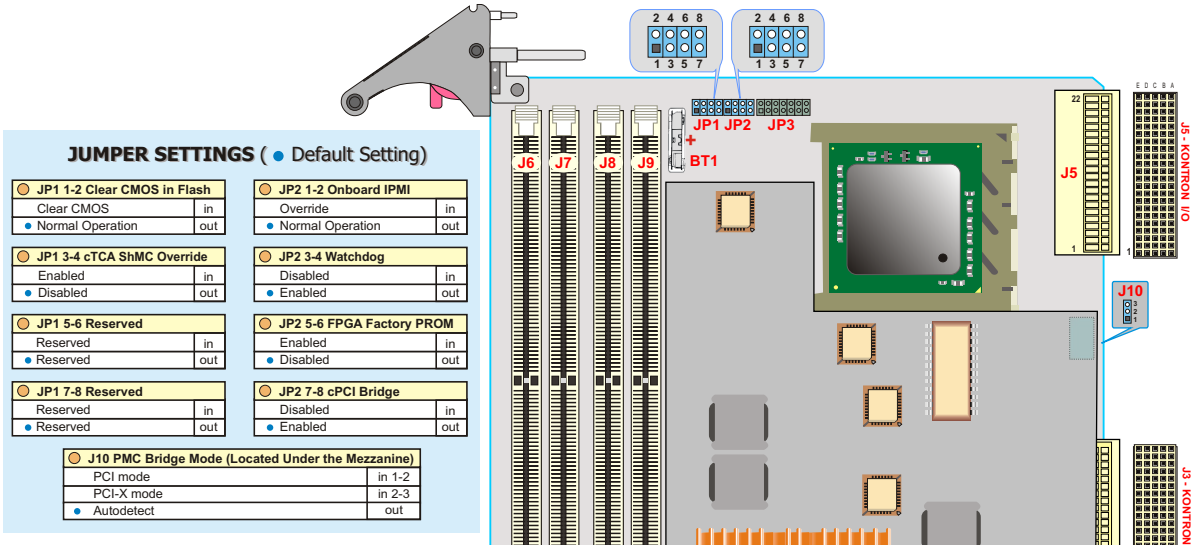
3.1.1 Jumper Description

Table 3-1:Jumper Description

Jumper	Pins	Name	Description (when jumper is in)
JP1	1-2	Clear CMOS in Flash	The BIOS clears the RTC registers at power up when the jumper is inserted.
JP1	3-4	cTCA ShMC Override	In cPCI mode: No effect In cTCA mode: Indicates the IPMC not to wait for Shelf management controller signals.
JP1	5-6	Reserved	Reserved
JP1	7-8	Reserved	Reserved
JP2	1-2	Onboard IPMI	Keeps the IPMC in reset. (FPGA)
JP2	3-4	Watchdog	Disables the FPGA and the IPMI watchdogs. (FPGA)
JP2	5-6	FPGA Factory PROM	Selects the factory PROM for the FPGA. (FPGA)
JP2	7-8	cPCI Bridge	Disables baseboard PCI bridge. It doesn't affect the PMC bridge.
J10 Located under the mezzanine	1-2-3	PMC Bridge Mode	PCI Mode enabled when jumper is in position 1-2 PCI-X Mode enabled when jumper is in position 2-3 Autodetect Mode enabled when jumper is not present

3.1.2 Setting Jumper & Locations

Figure 3-1:Setting Jumper & Locations



3.2 Processor

This product ships with the CPUs and a thermal solution installed. The thermal solution is custom and critical for passive cooling. Cooling performance can greatly be affected if manipulation is not handled within Kontron facility.

3.3 Memory

The main memory is composed of DDR2 memories with the following specifications:

- There are 2 independent DDR2 memory channels, composed of 2 DDR2 DIMMs per channel
- Each DDR2 DIMM can support up to 8GB of DDR2 667 memory, using 256 Mb to 8GB memory devices
- Supports only Registered ECC DIMMs
- Supports x4 and x8 devices
- Support for single or dual-rank modules
- Support up to 4 ranks per channel
- Theoretical memory Read Bandwidth is 10.6 GBytes/s total(2 channels x 5.3 GB/s for DDR 667)
- DIMM sparing capability on each channel
- Maximum total memory capacity is 32GB

All memory busses operate at 333 MHz clock speed with dual data rate. This means that data is transferred at 667 MHz.

The content of the SDRAM is not affected by a warm reset.

Only use validated memory with this product. Thermal issues or other problems may arise if you don't use recommended modules. At the time of publication of this user guide, the memories listed on Table 3-2 were confirmed functional with the product. As the memory market is volatile, this list is subject to change, please consult your local technical support for an up to date list.

3.3.1 Memory List and Characteristics:

Table 3-2:Memory List and Characteristics

Manufacturer Part Number	Description	Company
VL393T2953-E6S	DIMM DDR2-667 1GB 128M*72X8 REG ECC 1.2"	VIRTIUM
MT9HTF12872PY-667E1	DIMM DDR2-667 1GB 128M*72X8 REG ECC 1.2"	Micron Technology, Inc.
VL393T5750-E6S	DIMM DDR2-667 2GB 256M*72X4 REG ECC 1.2"	VIRTIUM
MT18HTF25672PY-667E1	DIMM DDR2-667 2GB 256M*72X4 REG ECC 1.2"	Micron Technology, Inc.
VL393T5160A-E6M	DIMM DDR2-667 4GB 512M*72X4 REG ECC 1.2"	VIRTIUM
MT36HTF51272PY-667E1	DIMM DDR2-667 4GB 512M*72X4 REG ECC 1.2"	Micron Technology, Inc.

WARNING

Because static electricity can cause damage to electronic devices, take the following precautions:

Keep the board in its anti-static package, until you are ready to install memory.

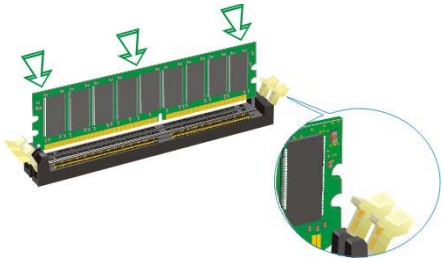
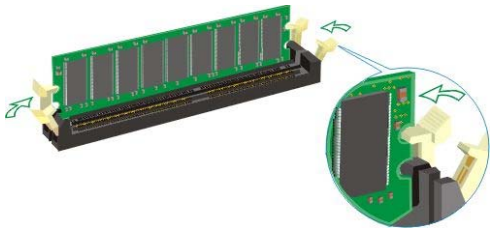
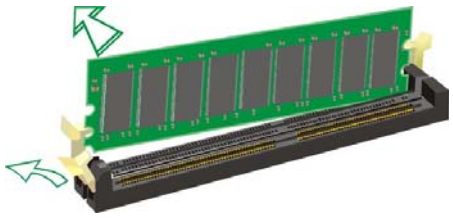
Wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.

Handle the board by the faceplate or its edges.

3.3.2 Installing Memory

Note:
Memory should be populated in pairs.
2 DIMMs configuration: J6 & J7; 4 DIMMs configuration: J6, J7, J8 & J9

Figure 3-2:Installing Memory

On an anti-static plane, place the board so that you face the DIMM sockets and the faceplate is facing you.	
Make sure both retaining clips are fully open. Insert the memory module into J6& J7 then in J8 & J9. To install the memory module, align the notches on the module with the socket's key inserts.	
Push down the memory module until the retaining clips clip on each side.	
Repeat these steps to add other memory modules.	
To remove a DIMM from a socket, push down the left retaining clip of the socket. Pull the module up from the left to remove.	

Note:
The right ejector won't be usable during the removal process because of mechanical restrictions due to the mezzanine.

Note:
Every time the memory configuration changes, a Clear CMOS must be done to allow the BIOS to do a new memory calibration. This step will take about 20 seconds.

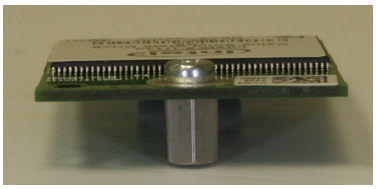
3.4 USB Flash Drive

3.4.1 Installing the USB Flash Drive

To install the Flash Drive:

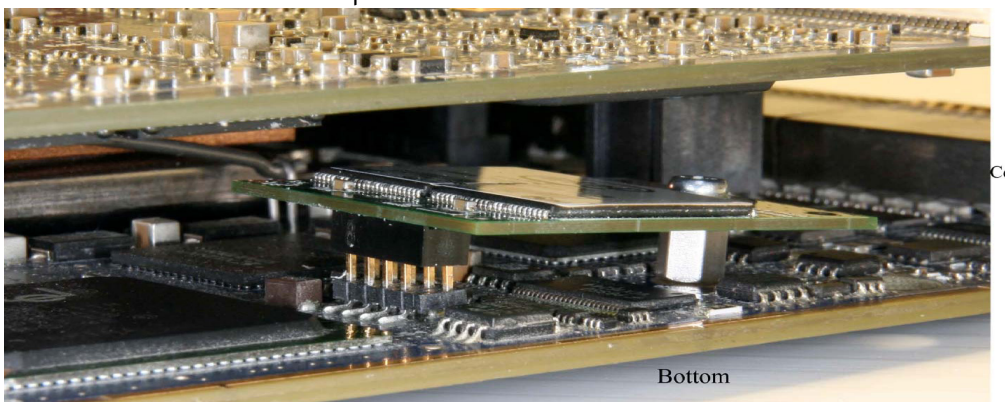
1 Install the standoff (Hexagonal female-female L=6 MM Thread: M2.5-0.45, Zinc plated) with a screw (Phillips, cheese head M2.5 x 4; Zinc plated).

Figure 3-3:Flash Disk Installation step 1



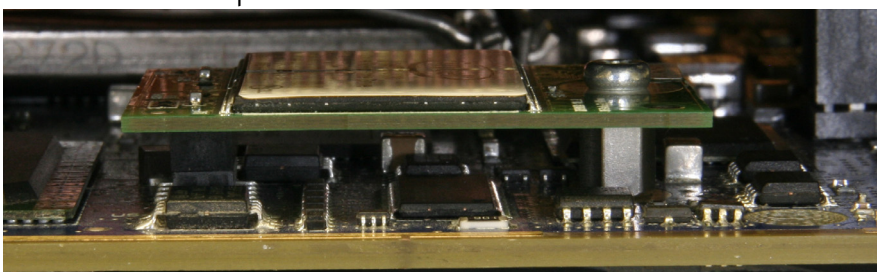
2 Insert the flash drive connector into J18, the USB Flash Connector and make sure the two connectors are properly aligned.

Figure 3-4:Flash Disk Installation step 2



3 Push down the USB flash drive.

Figure 3-5:Flash Disk Installation step 3



4 Flip the board to the back side and install an other screw to secure the flash drive. There is a special hole in the backcover to allow you to install the screw.

WARNING

Be careful when you install the USB Flash. There are sensitive devices around this connector.

3.4.2 Removing the USB Flash Drive

1 Remove the screw that is on the back of the board.

2 Pull out the flash drive gently to make sure the connector pins are not bending.

WARNING

Be careful when you remove the USB Flash. There are sensitive devices around this connector.

3.5 Onboard Interconnectivity

3.5.1 Onboard Connectors and Headers

Table 3-3:Onboard Connectors and Headers

Description	Connector	Comments
CompactPCI	J1	CPCI bus signals and power
CompactPCI	J2	64 bit extension, arbitration, clocks, reset and power.
CompactPCI	J3	Serial Ports A and B, LAN 0 and 1, PS/2 Keyboard and Mouse, VGA, and USB
CompactPCI	J5	
DDR2 Memory Sockets	J6 - J9	4 DDR2 Memory Sockets support up to 8Gb of memory per Socket
COM	J12	COM1 DB9 connector
USB	J13	USB connector
VGA	J14	Micro-DB15. An adaptor is required to connect a regular DB15 connector*
Ethernet	J15	RJ45 Ethernet Connector on Faceplate
USB Flash Drive Connector	J18	USB Flash Drive Connector located on the baseboard
Battery	BT1	Battery Socket (CR2032)
CompactPCI	J1 Mezzanine	
64-bit PCIX Mezzanine	J11-J13 Mezzanine	
XMC Mezzanine Connector	J15 Mezzanine	

* This adaptor is available from Kontron. PN:1015-9396

3.6 Board Hot Swap and Installation

Because of the high-density pinout of the hard-metric connector, some precautions must be taken when the board is connecting to or disconnecting from a backplane:

1 Rail guides must be installed on the enclosure to slide the board to the backplane.

2 Do not force the board if there is mechanical resistance while inserting the board.

3 Screw the frontplate to the enclosure to firmly attach the board to its chassis.

4 Use extractor handles to disconnect and extract the board from its slot.

WARNING

Always use a grounding wrist wrap before installing or removing the board from a chassis.

3.6.1 Installing the Board in the Chassis

To install a board in a chassis:

1 Remove the filler panel of the slot or see "Removing the Board" below.

2 Ensure the board is configured properly. (Make sure the battery protection tab is removed.)

3 Carefully align the PCB edges in the bottom and top card guide.

4 Insert the board in the system until it makes contact with the backplane connectors.

5 Using both ejector handles, engage the board in the backplane connectors until both ejectors are locked.

6 Fasten screws at the top and bottom of the faceplate.

3.6.2 Removing the Board

If you would like to remove a board from your chassis please follow carefully these steps:

1 Unscrew the top and the bottom screw of the front panel.

2 Unlock the lower handle latch, depending on the software step; this may initiate a clean shutdown of the operating system.

3 Wait until the blue LED is fully ON, this mean that the hot swap sequence is ready for board removal.

4 Use both ejectors to disengage the board from the backplane.

5 Pull the board out of the chassis.

3.6.3 Installing a PMC/XMC Card

To install a PMC/XMC card:

1 Remove the front EMI cap.

2 Carefully push the PMC/XMC to mate the three connectors.

3 Screw the four screws at the bottom of the PMC/XMC to fix it to the board.

4 Power up the board and verify the PMC/XMC functionality.

WARNING

PMC and XMC card cannot be installed at the same time

3.6.4 Removing a PMC/XMC Card

To remove a PMC/XMC card:

1 Unscrew the four screws at the bottom of the PMC/XMC.

2 Carefully pull out the PMC/XMC from the connectors.

3 Reinstall the front EMI cap.

3.6.5 Installing the RTM-CP6014

To install the rear I/O:

1 Shutdown your front board OS or extract the CP6014 board before installing the Rear I/O.

2 Remove the filler panel of the slot.

3 Ensure the rear I/O is configured properly.

4 Carefully align the PCB edges in the bottom and top card guide.

5 Align the rear I/O with the CPU board in the system and push it until it makes contact with the backplane.

6 Using both ejector handles, engage the board in the backplane's connectors.

7 Fasten screws at the top and bottom of the faceplate.

3.6.6 Removing the RTM-CP6014

To remove the Rear I/O:

1 Shutdown your front board OS or extract the CP6014 board before installing the Rear I/O.

2 Unscrew the top and the bottom screw of the faceplate.

3 Use both ejectors to disengage the board from the backplane.

4 Pull the board out of the chassis.

3.7 Battery Backup

An onboard 3V lithium battery is provided to back up BIOS setup values and the real time clock (RTC).

3.7.1 Operation and Preventative Maintenance

The operational battery voltage must be between 2.4 and 3.0 volts.

When the board is stored and is kept in it's original package, the battery must be replaced when the battery voltage is below 2.4 volts.

For preventive operational maintenance, we recommend to verify the battery voltage after 4 years. After that period, we recommend that the safety voltage is checked more often. The normal battery life expectancy depends on the utilisation of the board.

Battery description: CR2032 3V battery

3.7.2 Replacing the Battery

To replace the battery follow the procedure below:

1 Turn off the board and remove it from the backplane.

2 Remove the battery from the socket with your fingers. Do not use any metal tool.

3 Install a new battery in the socket and observe the correct polarity. (+ must face J5; - must face the DIMM connectors)

4 Reinstall the card in the chassis.

5 Enter the BIOS setup by pressing “F1” to restore the time and date configurations.

WARNING

There is a danger of explosion if you replace the battery incorrectly.

Replace the battery with the same or equivalent type .

Chapter 4

Hardware Management

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4. Hardware Management

4.1 Introduction

The purpose of the hardware management system is to monitor, control, assure proper operation and provide hot swap support of cPCI/cTCA Boards. The hardware monitoring is based on the IPMI specification 1.5.The hardware management system watches over the basic health of the system, reports anomalies, and takes corrective action when needed. The hardware management system can retrieve inventory information and sensor readings as well as receive event reports and failure notifications (in BMC mode) from other boards in the chassis. The hardware management system can also perform basic recovery operations such as power cycle or reset of managed entities.

The CP6014 is always equipped with a mezzanine. Since the mezzanine is always present and is not hot swappable, the mezzanine is considered as part of the main board and not a different FRU.

The CP6014 only has one IPMI FRU: FRU0. The rear I/O is considered a non-intelligent unmanaged FRU.

4.2 Architecture

4.2.1 Overview

The IPMC implements all mandatory modules to be full IPMI 1.5 rev 1.1 compliant. Some modules, like Serial-Over-LAN, do not exist in the IPMI 1.5 specification. In that case, the IPMI 2.0 specification is used.

The CP6014 is also compliant to the PICMG 2.9 R1.0 cPCI specification.

The CP6014 is designed to meet PICMG 2.50 cTCA specification. This specification is not signed yet. We cannot claim compatibility to an unsigned specification. However, all the useful functionalities and commands are implemented based on the current state of the PICMG 2.50 vD0.8 specification.

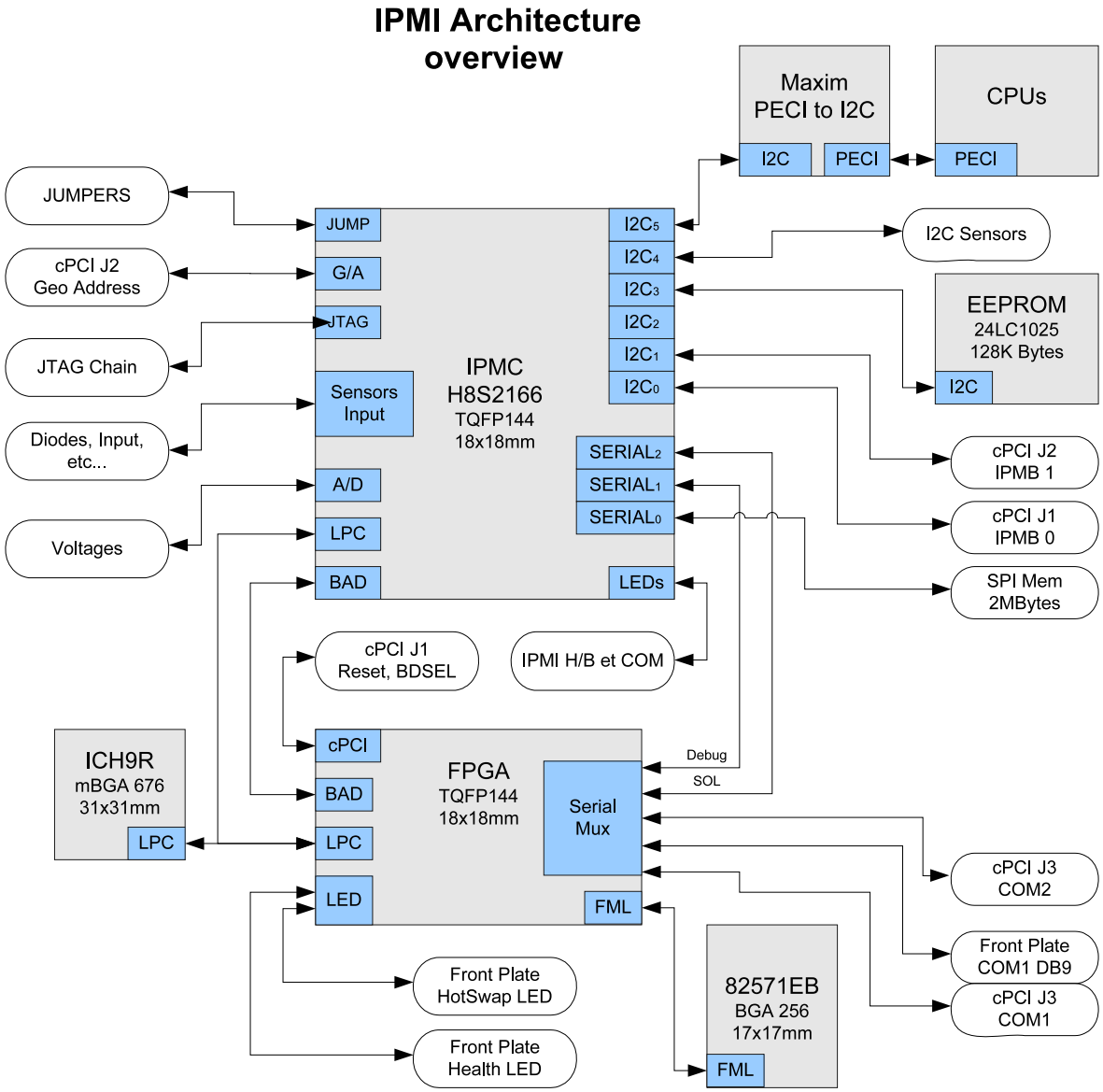
The CP6014 offers IOL/SOL functionality through the onboard Ethernet i82571EB TCO Passthrough FML interface.

CP6014 has many sensors (temperatures, voltages and others) available through A/D converter, I/O and I2C. The CP6014 introduces the new PECI interface to read digital CPU temperatures. Since the Renesas HD64F2166 does not have a PECI interface, a Maxim I2C to PECI converter is used.

For firmware redundancy, one memory bank is used and it can contain 2 firmware images. This bank is filled and managed by the IPMC.

4.2.2 Bloc Diagram

Figure 4-1:IPMI Bloc Diagram



4.2.3 cPCI vs cTCA

The CP6014 is compatible with the cPCI and cTCA specification. To be compatible with both specification, the cTCA specification proposes the reading of the PCI_Reset# line in J1 connector (PCI_Reset# is low for cTCA backplane). Based on the signal value that have been read at the insertion, the FPGA/IPMC knows if he has been inserted on a cTCA or legacy cPCI chassis. One of the main differences between cPCI and cTCA is the control of the payload power and reset after insertion. For cPCI, the handle is the only trigger to move into the different hot-swap states. In cTCA, the blade, along with handle, wait for commands from the shelf manager to move from different hot-swap states.

Under cPCI PCMIG2.0R3.0 architecture, it is common to see a chassis without a shelf manager. When operating within that environment, the board will function without any specific requirement. This legacy behaviour will be transparent to the user as it is designed to be compliant with.

While cTCA PICMG2.5 vD0.8 is still (at the general availability of the CP6014) in a draft format, the board has been designed to meet the current requirements. In the event where there is no shelf-manager present in a cTCA compliant chassis, jumper "cTCA ShMC Override" can be installed to allow activation of the CP6014.

4.2.4 IPMC Mode: BMC / SMC

In a cPCI/cTCA chassis, many blades can be inserted. Only one IPMC within the shelf can be the "Baseboard Management Controller" (BMC). This mode is normally reserved for the shelf-manager. Since the chassis is not always populated with a shelf-manager, the system integrator must select a BMC within the pool of IPMC present in the chassis. While the CP6014's IPMC is configured in SMC by default, it can also act as a chassis BMC. However, the CP6014 only cover the IPMC BMC functionality (SDRR, SEL, etc.) and does not replace a shelf-manager.

In BMC mode, the IPMC includes the following extra module: SDR Repository, SDR Repository Init Agent, SEL acting as the main SEL for the chassis (a local SEL is also provided in SMC mode) and retrieve Shelf-Address Information.

The CP6014 is pre-configured and ship in SMC mode.

An option is available in the BIOS to switch from BMC/SMC mode.

4.2.5 FRU Addressing

From the Front Blade Unit perspective, the PICMG cPCI 2.0 specification and PICMG cTCA 2.5 introduces four different kinds of addresses to locate a Front Blade Unit holding the IPM controller. These addresses are:

- Geographical Address - Unique within slot type, but not unique across different slot types. Defined and read through hardware signals from the backplane using 5 signals. Blades Geographical Addresses are from 1-30.
- IPMB Address - An address that the IPMC uses when sending or receiving information on the IPMB. IPMB Address is 8-bit long. IPMB address has a fixed mapping with the Geographical Address.
- Hardware Address - Generated from the IPMB address by dividing it by 2. The hardware address is present only to preserve compatibility with ATCA software.
- Physical Address - (Sometime referred as Physical Slot) describes the physical location of a FRU in the Shelf. The Physical Address is equivalent to the Physical Slot Number. Physical Slot Numbers start with 1, designating the leftmost physical slot, and incrementing toward the right. Physical Address consists of Site Number and Site Type. In case of blades, the Site Number is equivalent to the slot number where the blade is mounted. Site Type identifies the FRU type. Site Types are defined in [PICMG cTCA 2.5] Table 4-7.

All the addresses are set by the Shelf configuration and the Unit only reads the geographical address to adjust its own hardware and IPMB-0 address.

If the CP6014 is configured as a BMC, the geographical address is ignored and IPMB address is set to 20h.

Here is the list of addresses based on geographical addresses.

Table 4-1:Geographical Address Table

Geo.	IPMB	Hardware	Physical Address Site Number
1	B0h	58h	1
2	B2h	59h	2
3	B4h	5Ah	3
4	B6h	5Bh	4
5	B8h	5Ch	5
6	BAh	5Dh	6
7	BCh	5Eh	7
8	BEh	5Fh	8
9	C0h	60h	9
10	C4h	62h	10
11	C6h	63h	11
12	C8h	64h	12
13	CAh	65h	13
14	CCh	66h	14
15	CEh	67h	15
16	D0h	68h	16
17	D2h	69h	17
18	D4h	6Ah	18
19	D6h	6Bh	19
20	D8h	6Ch	20
21	DAh	6Dh	21
22	DCh	6Eh	22
23	DEh	6Fh	23
24	E0h	70h	24
25	E2h	71h	25
26	E4h	72h	26
27	E6h	73h	27
28	E8h	74h	28
29	EAh	75h	29
30	ECh	76h	30

4.3 Functionnality

The Front Blade Unit supports an "intelligent" hardware management system, based on the Intelligent Platform Management Interface Specification 1.5. The hardware management system of the Front Blade Unit provides the ability to monitor events, and to log events to a central repository.

4.3.1 Channels & Interfaces

4.3.1.1 Channels Support

The CP6014 implements 5 different channels of 3 different types. The IPMB-0 channel is mandatory and is used to communicate within a shelf between every IPM controllers. The second IPMB-1 channel is optional but implemented on the CP6014. This channel adds redundancy to the IPMB-0 channel when the line is stuck or unusable. The CP6014 also implements a KCS channel (system interface) to communicate from the payload to the IPMC. The last 2 channels are LAN channel that can be used to remotely access the IPMC. Using this channel, a remote user can use IPMI-Over-LAN and Serial-Over-LAN to communicate using the Ethernet chips connected to the chassis switch.

Since LAN channel are accessible without being physically close to the chassis, Session authentication is required to send packet to the IPMC. Integrity check and encryption can also be added to this channel for higher security.

The IPMC implements the following channels:

Table 4-2:IPMC Channels

IPMC Channels	Medium	Protocol	Session Support	ID	Privileges
IPMB-0 (active)	I2C	IPMB-1.0	No	0 (00h)	Full Privileges (Admin)
IPMB-1 (standby)	I2C	IPMB-1.0	No	1 (01h)	Full Privileges (Admin)
LAN Backplane 2.16 Channel 0	802.3 LAN	RMCP(+) RMCP	Yes	2 (02h)	Based on authentication and user rights
LAN Backplane 2.16 Channel 1	802.3 LAN	RMCP(+) RMCP	Yes	3 (03h)	Based on authentication and user rights
KCS - System Interface	System Interface	KCS	No	15 (0Fh)	Full Privileges (Admin)

4.3.1.2 IPMB

The main management-oriented link within a Shelf is a two-way implementation of the Intelligent Platform Management Bus (IPMB). IPMB is based on the inter-integrated circuit (I2C) bus and is part of the IPMI architecture. In cPCI/cTCA Shelves, the main IPMB is called IPMB-0. Shelf Managers attach to IPMB-0 through a variant IPM Controller called the Shelf Management Controller (ShMC). On cPCI/cTCA IPM Controllers, there is no mandatory backup IPMB. However, the CP6014 implements the IPMB-1 channel in backup to channel IPMB-0 when communication on IPMB-0 is no more possible (active/standby mode). CP6014 also implements an IPMB sensors and recovery mechanism to recover from faulty situation.

The IPMB is a private BUS between each intelligent IPMC within a chassis. The system management software does not have direct access to the IPMB bus. However, to reach another IPMC connected to the bus, the system management software can send a bridge command from another interface such as KCS or IOL.

4.3.1.3 System Interface (KCS)

The CP6014 implements a system interface to has access to the local IPMC through IO spaces. The CP6014 implements the KCS-SMS interface base on IPMI specifications 1.5. To communicate with the IPMC from the payload, some drivers and utility are available in different OS flavor. In Linux, the driver named OpenIPMI is available and offers a KCS driver. There is also a utility named IPMITool that can be used to send commands to IPMC directly using the KCS-SMS interface (and also through IPMI-Over-LAN). The CP6014 KCS-SMS interface can be configured to be interrupt driven. CP6014 is compatible with interrupt 10 and 11. Configuration of the interrupt is done in the BIOS.

4.3.1.4 IPMI-Over-LAN

The CP6014 implements a way to transfer IPMI messages between the IPMC and a remote management system (remote console) over an Ethernet LAN connection using UDP under IPv4. This interface is called IPMI-Over-LAN. IPMI request are encapsulated within a RMCP (or RMCP+) protocol.

There is two possible implementation of IPMI-Over-LAN. One is called IPMI-Over-LAN 1.5 (based on IPMI specification 1.5) and the second is called IPMI-Over-LAN 2.0 (based on IPMI specification 2.0). CP6014 implements both interface.

4.3.2 LEDs

The following table shows the LEDs controlled by the built-in IPMC.

Table 4-3:IPMI LEDs

PICMG ID	Name	Location	Color	Control	Descriptions
0	Blue LED	Face Plate	Blue	Hardware/IPMC	Local: FRU State (Hot Swap) Override: User
1	Health LED	Face Plate	Green/Off	Hardware/IPMC	Local Ctrl: Healthy Status Override: User
N/A	HDD/ Usr LED	Face Plate	Green/Off	BIOS/IPMC	Local ctrl : Selected HDD activity Override : User
N/A	IPMI Activity/ Hearthbeat	PCB	Green/Amber	IPMC	IPMC Heartbeat & Activity (Override is not possible)

The following lines describe the normal behavior of these LEDs. Note that each of them, except the IPMC Heartbeat & Activity LED, may be overridden and controlled using the PICMG LED API.

4.3.2.1 Blue LED

The BLUE LED (LED 0) provides basic feedback to the user during FRU maintenance. The Blue LED shows the current state of the FRU in the hot swap state machine. The Blue LED is the only mandatory LED in both cPCI and cTCA specification. See cTCA specification D0.8 section 4.2.5.1 for complete details about the Blue LED.

4.3.2.2 Health LED

The LED 1 is the health / power good LED. This LED reflects the state of the Health error sensor, a sensor built from an aggregation of critical sensors of the CPU engine. In normal condition, the Health error sensor is not asserted and the LED is green indicating that everything is fine. If the sensor is asserted for any reason, the LED is OFF, indicating a hardware problem. See column “Included in Heatlh LED Aggregate” Table 4-15: IPMI Sensors to see which sensors are aggregated to control the Health LED state.

4.3.2.3 IPMC LED

This LED gives the following information:

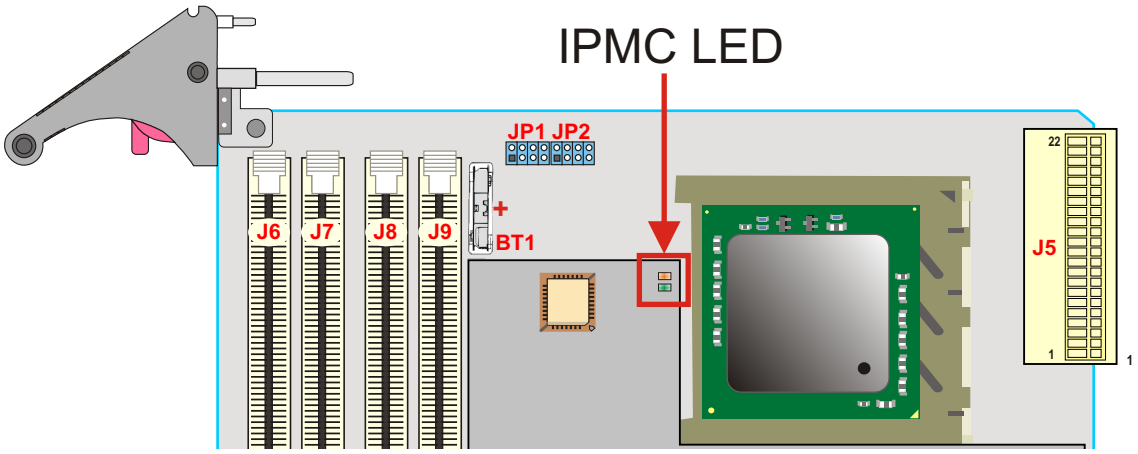
LED Color: Amber

Normal status:	Off
When Slow Blinking (100 msec ON, 1.4 sec OFF):	Occur when IPMI wants to communicate with the SMS/SMM but doesn't get an answer from it.
When Fast Blinking (8x - 150 msec ON, 50 msed OFF):	Occur when a packet is transmitted or received on the IPMB bus.

LED Color: Green

Normal status:	Slow Blinking (100 msec ON, 1.4 sec OFF)
When Slow Blinking (100 msec ON, 1.4 sec OFF):	Heartbeat, IPMI firmware runs normally.
When Fast Blinking (8x - 150 msec ON, 50 msed OFF):	Occur when a packet is transmitted or received on the KCS interface.

Figure 4-2:IPMC LED location



4.3.3 FRU

The CP6014 FRU is compliant to IPMI 1.5 and cTCA 2.5 specification. The FRU contain the standard COMMON, BOARD and PRODUCT area. Even though the cTCA specification includes the idea of E-keying, the CP6014 does not include any E-keying records. Since there is no E-keying, the Multi-Record area is not present. Board and product area information is written to the IPMC at production stage.

4.3.4 List of supported IPMI command

4.3.4.1 IPM Device Support

Table 4-4:IPM Device Support

IPM Device "Global" Commands	NetFn	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
Get Device ID	App	01h	Yes	Yes
Cold Reset	App	02h	Yes	Yes
Warm Reset	App	03h	No	No
Get Self Test Results	App	04h	Yes	Yes
Manufacturing Test On	App	05h	Yes	Yes
Set ACPI Power State	App	06h	Yes	Yes
Get ACPI Power State	App	07h	Yes	Yes
Get Device GUID	App	08h	Yes	Yes
Broadcast "Get Device ID"	App	01h	Yes	Yes

4.3.4.2 Watchdog Timer Support

Table 4-5:Watchdog Timer Support

Watchdog Timer Commands	NetFn (LUN 0)	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
Reset Watchdog Timer	App	22h	Yes	Yes
Set Watchdog Timer	App	24h	Yes	Yes
Get Watchdog Timer	App	25h	Yes	Yes

4.3.4.3 Device and Messaging Commands Support

Table 4-6:Device and Messaging Commands Support

Device and Messaging Commands	NetFn (LUN 0)	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
Set BMC Global Enables	App	2Eh	Yes	Yes
Get BMC Global Enables	App	2Fh	Yes	Yes
Clear Message Flags	App	30h	Yes	Yes
Get Message Flags	App	31h	Yes	Yes
Enable Message Channel Receive	App	32h	Yes	Yes
Get Message	App	33h	Yes	Yes
Send Message	App	34h	Yes	Yes
Read Event Message Buffer	App	35h	Yes	Yes
Get BT Interface Capabilities	App	36h	No	No
Get System GUID	App	37h	Yes	Yes
Get Channel Authentication Capabilities	App	38h	Yes	Yes
Get Session Challenge	App	39h	Yes	Yes
Activate Session	App	3Ah	Yes	Yes
Set Session Privilege Level	App	3Bh	Yes	Yes
Close Session	App	3Ch	Yes	Yes
Get Session Info	App	3Dh	Yes	Yes
Get Authentication Code	App	3Fh	No	No
Set Channel Access	App	40h	Yes	Yes
Get Channel Access	App	41h	Yes	Yes
Get Channel Info	App	42h	Yes	Yes
Set User Access	App	43h	Yes	Yes
Get User Access	App	44h	Yes	Yes
Set User Name	App	45h	Yes	Yes
Get User Name	App	46h	Yes	Yes
Set User Password	App	47h	Yes	Yes
Activate Payload	App	48h	Yes	Yes
Deactivate Payload	App	49h	Yes	Yes
Get Payload Activation Status	App	4Ah	Yes	Yes
Get Payload Instance Info	App	4Bh	Yes	Yes
Set User Payload Access	App	4Ch	Yes	Yes
Get User Payload Access	App	4Dh	Yes	Yes
Get Channel Payload Support	App	4Eh	Yes	Yes
Get Channel Payload Version	App	4Fh	Yes	Yes
Get Channel OEM Payload Info	App	50h	No	No
Master Write-Read	App	52h	Yes	Yes

Device and Messaging Commands	NetFn (LUN 0)	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
Get Channel Cipher Suites	App	54h	Yes	Yes
Suspend/Resume Payload Encryption	App	55h	Yes	Yes
Set Channel Security Keys	App	56h	No	No
Get System Interface Capabilities	App	57h	Yes	Yes

4.3.4.4 Event Support

Table 4-7:Event Support

Event Commands	NetFn (LUN 0)	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
Set Event Receiver	S/E	01h	Yes	Yes
Get Event Receiver	S/E	02h	Yes	Yes
Platform Event	S/E	03h	Yes	Yes

4.3.4.5 PEF And Alerting Support

PEF And Alerting Commands

Commands 10h-17h on NetFn Storage/Event (LUN 0) are not supported.

4.3.4.6 Sensor Device Support

Table 4-8:Sensor Device Support

Sensor Device Commands	NetFn (LUN 0)	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
Get Device SDR Info	S/E	20h	Yes	Yes
Get Device SDR	S/E	21h	Yes	Yes
Reserve Device SDR Repository	S/E	22h	Yes	Yes
Get Sensor Reading Factors	S/E	23h	No	No
Set Sensor Hysteresis	S/E	24h	Yes	Yes
Get Sensor Hysteresis	S/E	25h	Yes	Yes
Set Sensor Threshold	S/E	26h	Yes	Yes
Get Sensor Threshold	S/E	27h	Yes	Yes
Set Sensor Event Enable	S/E	28h	Yes	Yes
Get Sensor Event Enable	S/E	29h	Yes	Yes
Rearm Sensor Events	S/E	2Ah	No	No

Sensor Device Commands	NetFn (LUN 0)	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
Get Sensor Event Status	S/E	2Bh	No	No
Get Sensor Reading	S/E	2Dh	Yes	Yes
Set Sensor Type	S/E	2Eh	No	No
Get Sensor Type	S/E	2Fh	No	No

4.3.4.7 FRU Device Support

4.3.4.7.1 FRU Characteristics

8 KBytes is available for the FRU data.

Table 4-9:FRU Device Commands

FRU Device Commands	NetFn (LUN 0)	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
Get FRU Inventory Area Info	Storage	10h	Yes	Yes
Read FRU Data	Storage	11h	Yes	Yes
Write FRU Data	Storage	12h	Yes	Yes

4.3.4.8 SDRR Device Support

4.3.4.8.1 SDRR Characteristics

The SDRR can contain up to 1279 entries. SDRR repository is available in BMC mode only.

Table 4-10:SDRR Device Commands

SDR Repository Device Commands	NetFn (LUN 0)	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
Get SDR Repository Info	Storage	20h	Yes	No
Get SDR Repository Allocation Info	Storage	21h	Yes	No
Reserve SDR Repository	Storage	22h	Yes	No
Get SDR	Storage	23h	Yes	No
Add SDR	Storage	24h	No	No
Partial Add SDR	Storage	25h	Yes	No
Delete SDR	Storage	26h	Yes	No
Clear SDR Repository	Storage	27h	Yes	No
Get SDR Repository Time	Storage	28h	No	No

SDR Repository Device Commands	NetFn (LUN 0)	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
Set SDR Repository Time	Storage	29h	No	No
Enter SDR Rep Update Mode	Storage	2Ah	No	No
Exit SDR Repository Update Mode	Storage	2Bh	No	No
Run Initialization Agent	Storage	2Ch	Yes	No

4.3.4.9 SEL Device Support

4.3.4.9.1 SEL Characteristics

SEL is included in both BMC and SMC mode.

SEL has provision to store up to 2047 entries.

Table 4-11:SEL Device Command Support

SEL Device Commands	NetFn (LUN 0)	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
Get SEL Info	Storage	40h	Yes	Yes
Get SEL Allocation Info	Storage	41h	Yes	Yes
Reserve SEL	Storage	42h	Yes	Yes
Get SEL Entry	Storage	43h	Yes	Yes
Add SEL Entry	Storage	44h	Yes	Yes
Partial Add SEL Entry	Storage	45h	No	No
Delete SEL Entry	Storage	46h	Yes	Yes
Clear SEL	Storage	47h	Yes	Yes
Get SEL Time	Storage	48h	Yes	Yes
Set SEL Time	Storage	49h	Yes	Yes
Get Auxiliary Log Status	Storage	5Ah	No	No
Set Auxiliary Log Status	Storage	5Bh	No	No

4.3.4.10 LAN Device Support

Table 4-12:LAN Device Support

LAN Device Commands	NetFn (LUN 0)	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
Set LAN Configuration Parameters	Transport	01h	Yes	Yes
Get LAN Configuration Parameters	Transport	02h	Yes	Yes
Suspend BMC ARPs	Transport	03h	Yes	Yes
Get IP/UDP/RMCP Statistics	Transport	04h	Yes	Yes

4.3.4.11 SOL Device Support

Table 4-13:SOL Device Support

SOL Commands	NetFn (LUN 0)	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
SOL Activating	Transport	20h	No	No
Set SOL Configuration Params	Transport	21h	Yes	Yes
Get SOL Configuration Params	Transport	22h	Yes	Yes

4.3.4.12 PICMG (cTCA) Command Support

Table 4-14:PICMG (cTCA) Command Support

cTCA Commands	NetFn	CMD	Kontron BMC Mode Support	Kontron SMC Mode Support
Get PICMG Properties	PICMG	00h	Yes	Yes
Get Address Info	PICMG	01h	Yes	Yes
Get Shelf Address Info	PICMG	02h	No	No
Set Shelf Address Info	PICMG	03h	No	No
FRU Control PICMG	PICMG	04h	Yes	Yes
Get FRU LED Properties	PICMG	05h	Yes	Yes
Get LED Color Capabilities	PICMG	06h	Yes	Yes
Set FRU LED State	PICMG	07h	Yes	Yes
Get FRU LED State	PICMG	08h	Yes	Yes
Set FRU Activation Policy	PICMG	0Ah	Yes	Yes
Get FRU Activation Policy	PICMG	0Bh	Yes	Yes
Set FRU Activation	PICMG	0Ch	Yes	Yes
Get Device Locator Record ID	PICMG	0Dh	Yes	Yes
Set Port State	PICMG	0Eh	No	No
Get Port State	PICMG	0Fh	No	No
Compute Power Properties	PICMG	10h	No	No
Set Power Level	PICMG	11h	No	No
Get Power Level	PICMG	12h	No	No
Renegotiate Power	PICMG	13h	No	No
Get Fan Speed Properties	PICMG	14h	No	No
Set Fan Level	PICMG	15h	No	No
Get Fan Level	PICMG	16h	No	No
Bused Resource Control	PICMG	17h	No	No
FRU Control Capabilities (Based on ATCA specification)	PICMG	1Eh	Yes	Yes

4.3.5 IPMI Sensor Device and Sensor Data Record (SDR)

Every sensor on the baseboard is associated with a Sensor Data Record (SDR). Sensor Data Records contain information about the sensors identification such as sensor type, sensor name, sensor unit. SDR also contain the configuration of a specific sensor such as threshold/hysteresis, event generation capability that specifies sensor behavior. Some field of the sensor SDR are configurable through IPMI v1.5 command and are set to built-in initial value. Finally one field which is the sensor owner must reflect the baseboard addresses that allow the ShMc to identify the owner of the SDR when it is scanned from the satellite management controller and saved within the ShMc SDR repository.

The management controller is set up as a satellite management controller (SMC) by default and can be set up as BMC. It does support sensor devices. All SDRs can be queried using Device SDR commands to the firmware. Baseboard sensors that have been implemented are listed below.

4.3.5.1 IPMI Sensors

Table 4-15:IPMI Sensors detailed

ID	Sensor Name	BMC mode	SMC mode	Included in Health LED Aggregate	Description
0	XXX:FRU0 HotSwap	Yes	Yes	No	cTCA Board FRU HotSwap Sensor.
1	XXX:Temp Air In	Yes	Yes	Yes	Air Inlet Temperature
2	XXX:Temp CPU 0	Yes	Yes	Yes	CPU 0 Temperature
3	XXX:Temp CPU 1	Yes	Yes	Yes	CPU 1 Temperature
4	XXX:Temp MCH	Yes	Yes	Yes	MCH Temperature
5	XXX:Temp LANMngt	Yes	Yes	Yes	Front Plate Management LAN Temperature
6	XXX:Temp LAN BP	Yes	Yes	Yes	i82571EB Dual LAN (to backplane 2.16) Temperature
7	XXX:Temp VGA	Yes	Yes	Yes	VGA Temperature
8	XXX:Temp HDD	Yes	Yes	Yes	Storage HDD area Temperature
9	XXX:Temp DIMM	Yes	Yes	Yes	DIMM area Temperature
10	XXX:Temp Sw 1v8	Yes	Yes	Yes	Switch 1.8 volts Temperature
11	XXX:Pwr Good	Yes	Yes	Yes	Actual power status
12	XXX:Pwr Good Ev	Yes	Yes	Yes	Power status event that occur since the last power on or reset.
13	XXX:VCORE 0	Yes	Yes	Yes	CPU 0 Core Voltage
14	XXX:VCORE 1	Yes	Yes	Yes	CPU 1 Core Voltage
15	XXX:Vcc 5V	Yes	Yes	Yes	Voltage on 5v board power supply
16	XXX:Vcc 3.3V	Yes	Yes	Yes	Voltage on 3.3v board power supply
17	XXX:Vcc 3.3V SUS	Yes	Yes	Yes	Voltage on 3.3v suspend board power supply
18	XXX:Vcc 1.8V	Yes	Yes	Yes	Voltage on 1.8v board power supply
19	XXX:Vcc 1.5V	Yes	Yes	Yes	Voltage on 1.5v board power supply
20	XXX:Vcc 1.2V	Yes	Yes	Yes	Voltage on 1.2v board power supply
21	XXX:Vcc 1.1V	Yes	Yes	Yes	Voltage on 1.1v board power supply
22	XXX:Vcc VTT	Yes	Yes	Yes	Voltage on VTT
23	XXX:VBat Good	Yes	Yes	Yes	Indicates if voltage is good from the battery

ID	Sensor Name	BMC mode	SMC mode	Included in Health LED Aggregate	Description
24	XXX:Icc Board 5V	Yes	Yes	Yes	Current on 5v board power supply
25	XXX:Icc Board 3.3V	Yes	Yes	Yes	Current on 3.3v board power supply
26	XXX:Icc Mez 5V	Yes	Yes	Yes	Current on 5v Mezzanine power supply
27	XXX:Icc Mez 3.3V	Yes	Yes	Yes	Current on 3.3v Mezzanine power supply
28	XXX:Power 5V	Yes	Yes	No	FRU 0 5v Power consumption in watts
29	XXX:Power 3.3V	Yes	Yes	No	FRU 0 3.3v Power consumption in watts
30	XXX:Brd 5v OvCur	Yes	Yes	No	FRU 0 Board 5v Over Current event
31	XXX:Brd 3v3 OvCur	Yes	Yes	No	FRU 0 Board 3v3 Over Current event
32	XXX:Mez 3v3 OvCur	Yes	Yes	No	FRU 0 Mezzanine 3v3 Over Current event
33	XXX:PSU Status	Yes	Yes	Yes	Degrade / Fail Signal
34	XXX:RTM 5v PG	Yes	Yes	Yes	RTM 5V Power Good Present only when RTM is present
35	XXX:Board Reset	Yes	Yes	Yes	Board reset type and sources (See not at the end of this table)
36	XXX:EvRcvComLost	Yes	Yes	No	Event Receiver Communication Lost Indicates the state of communication with the shelf manager.
37	XXX:IPMI WD	Yes	Yes	Yes	IPMI watchdog
38	XXX:IPMB State	Yes	Yes	No	IPMB-0/1 fault detection sensor
39	XXX:IPMB1 Alert	Yes	Yes	No	Platform Alert / Digital Discrete
40	XXX:ACPI State	Yes	Yes	No	Advance Configuration and Power Interface State
41	XXX:Health Error	Yes	Yes		General health status, Aggregation of critical sensor
42	XXX:CPU 0 Status	Yes	Yes	No	CPU 0 Status
43	XXX:CPU 1 Status	Yes	Yes	No	CPU 1 Status
44	XXX:Memory	Yes	Yes	No	Memory Status
45	XXX:Post Value	Yes	Yes	No	Show current BIOS postcode value.
46	XXX:Post Error	Yes	Yes	Yes	U-BOOT System Firmware Progress
47	XXX:Critical Int	Yes	Yes	Yes	BIOS Critical Int.
48	XXX:Boot Error	Yes	Yes	No	BIOS memory Boot Error.
49	XXX:CMOS Memory	Yes	Yes	No	Indicates the error with the CMOS memory
50	XXX:Preboot Pswd	Yes	Yes	No	Indicates if an attempt was made without the right permission to access the BIOS menu CMOS password protected.
51	XXX:LAN 1 Link	Yes	Yes	No	LAN Channel 0 Link Status on 2.16 backplane interface
52	XXX:LAN 2 Link	Yes	Yes	No	LAN Channel 1 Link Status on 2.16 backplane interface
53	XXX:Power Denied	Yes	Yes	No	Indicates if shelf manager has denied power granting to the blade
54	XXX:FRU Agent	Yes	Yes	No	Indicates the current status of the FRU Init Agent and report failures
55	XXX:cTCA Chassis	Yes	Yes	No	Indicates if board is inserted in a cTCA chassis or a legacy cPCI chassis (No event)

ID	Sensor Name	BMC mode	SMC mode	Included in Health LED Aggregate	Description
56	XXX:PCI Present	Yes	Yes	No	Indicates if the backplane is PCI enabled(otherwise, PICMG 2.16 might be present) (No Event)
57	XXX:Brd HS Fault	Yes	Yes	Yes	Indicates on fault on the board hot swap controller.
58	XXX:Mez HS Fault	Yes	Yes	Yes	Indicates on fault on the board hot swap controller.
59	XXX:Board PwrOff	Yes	Yes	No	Indicates the state of the Board BD_SEL# line.
60	XXX:Mez PwrOff	Yes	Yes	No	Indicates the state of the Mezzanine
61	XXX:System Slot	Yes	Yes	No	Indicates wheter the board is inserted in a systems slot (asserted) or not (deasserted).
62	XXX:IPMC Storage	Yes	Yes	No	Management subsystem health: non volatile memory error.
63	XXX:FW Upg Mng	Yes	Yes	No	FirmWare Update Manager Status
64	XXX:Ipmc Reboot	Yes	Yes	No	IPMC reboot detection
65	XXX:Ver change	Yes	Yes		IPMC firmware upgrade detection
66	XXX:SEL State	Yes	Yes	No	Indicates the current state of the SEL.
67	XXX:InitAgent Err	Yes	No	No	Kontron OEM Initialization Agent status
68	XXX:IPMI Info-1	Yes	Yes	No	Internal IPMC firmware diagnostic
69	XXX:IPMI Info-2	Yes	Yes	No	Internal IPMC firmware diagnostic

In BMC mode, XXX will be replaced by BMC. Otherwise, it will be replaced by “S” followed by the slot number (i.e. Slot 2 will be S02)

Note:
ICH Full Reset is not supported by this board.A Full Reset will turn off the board and generate an Unexpected Deactivation event. To restart the board, cycle the lower handle.

4.3.5.2 IPMC sensors aggregation for health sensor

The table above contains a column that specify if the sensor is part of the IPMC sensors aggregation for the health led and sensors. When one of the sensors reports a fault, the health sensor become also faulty and the front health led will turn off.

4.3.5.3 OEM Sensors definition and Event trigger

The IPMI v1.5 specification describes most of the sensors on the CP6014. However, in some situation, the IPMI specification does not have adequate sensor definitions. To fill this gap, the IPMI specification provides the ability to create OEM sensor definition that fulfills specific needs. Using OEM sensor for the System Management Software requires a-priori knowledge of the OEM "sensor type" and OEM-defined "Event/ Reading Type Code" enumeration.

4.3.5.3.1 OEM Sensors Types

The following table shows the specific Sensor Type Code used by the CP6014

Table 4-16:OEM Sensors Types

OEM Sensor Type	OEM Number	Offset	Description
OEM Firmware Info	C0h	-	Contact Kontron Technical Support for more details.
OEM Board Reset Source	CFh	-	Event Data 2: Reset Type 00h: Warm reset 01h: Cold reset 02h: Forced Cold [Warm reset reverted to Cold] 03h: Soft reset [Software jump] Event Data 3: Reset Source 00h: IPMI Watchdog [cold, warm or forced cold] (IPMI Watchdog2 sensors gives additional details) 01h: IPMI commands [cold, warm or forced cold] (chassis control, FRU control) 02h: Processor internal checkstop 03h: Processor internal reset request 04h: Reset button [warm or forced cold] 05h: Power up [cold] 06h: Legacy Initial Watchdog / Warm Reset Loop Detection * [cold reset] 07h: Legacy Programmable Watchdog [cold, warm or forced cold] 08h: Software Initiated [soft, cold, warm of forced cold] 09h: Setup Reset [Software Initiated Cold] FFh: Unknown
OEM Init Agent Sensor	C2h	-	Sensor used to give the last error that occur in the RunInitAgent used with event/reading type code: - 0x03-IPMI Digital discrete Event Data 2: Contains OEM Init Agent error FFh: Error Fatal SDRR Reading FEh: Error Internal SDRR Reading FDh: Error Satellite Disable Event Receiver FCh: Error Internal Sensor FBh: Error Sensor Set Event Enable Command FAh: Error Sensor Set Type Command F9h: Error Sensor Set Hysteresis Command F8h: Error Sensor Set Threshold Command F7h: Unknown command error F6h: Error Satellite Enable Event Receiver Other: Reserved

OEM Sensor Type	OEM Number	Offset	Description
OEM Post Value Sensor	C6h	00h	Post Value Bit 0
		01h	Post Value Bit 1
		02h	Post Value Bit 2
		03h	Post Value Bit 3
		04h	Post Value Bit 4
		05h	Post Value Bit 5
		06h	Post Value Bit 6
		07h	Post Value Bit 7
		08h	Reserved
		09h	Reserved
		0Ah	Reserved
		0Bh	Reserved
		0Ch	Reserved
		0Dh	Reserved
		0Eh	Error Trig from Post Error
		0Fh	IPMI reserved
OEM FW Update Manager Status	CAh	00h	First Boot after upgrade
		01h	First Boot after rollback (error)
		02h	First Boot after errors (watchdog)
		03h	First Boot after manual rollback
		04h	Reserved
		05h	Reserved
		06h	Reserved
		07h	Reserved
		08h	Firmware Watchdog Bite, reset occur
		09h	Reserved
		0Ah	Reserved
		0Bh	Reserved
		0Ch	Reserved
		0Dh	Reserved
		0Eh	Debug Mode activated
		0Fh	IPMI reserved

4.3.5.3.2 OEM Event Reading Types

Table 4-17:OEM Event Reading Type

OEM Reading Type	Code	Offset	Descriptions
OEM Firmware Info 1	70h		Contact Kontron Technical Support for more details.
OEM Firmware Info 1	71h		Contact Kontron Technical Support for more details.
OEM Power Good	77h	00h 01h 02h 03h 04h 05h 06h 07h 08h 09h 0Ah 0Bh 0Ch 0Dh 0Eh 0Fh	VccGood 12V VccGood 5V VccGood 3.3V VccGood 2.5V VccGood 1.8V VccCore 1.5V VccGood 1.2V VccGood Core VccGood -5V VccGood 1.1V VccGood 1.05V Reserved Reserved Reserved Reserved IPMI reserved

4.3.6 IPMI Over LAN (IOL) support

The CP6014 provides IPMI Over LAN support over the 2 Ethernet connections of the backplane PICMG 2.16 interface. The 82571EB chip connected to the backplane PICMG 2.16 interface is also connected to the IPMC. The IPMI Over LAN solution is compatible with the IPMI 1.5 and IPMI 2.0 specification and support both RMCP and RMCP+ payload type.

The 2 channels are referred as channel 2 and channel 3. They can be accessed through those numbers when you use the IPMI commands related to channels. Only one channel can be activated at a time.

The implementation supports up to 4 simultaneous sessions (only one can enable SOL payload).

If a session is inactive for 1 minute it will be closed automatically.

The BIOS provides some basic functionality to see and configure the IPMI Over LAN. Using the BIOS, the following parameters can be seen/configured: IP address, MAC address, Subnet Mask, Gateway address, Active LAN channel. Theses settings are available in the BIOS section LAN configuration.

The recommended IPMI Over Lan / Serial Over LAN tool for Linux is IPMITool. This utility is available from the following web site: http://ipmitool.sourceforge.net/index.html.

4.3.6.1 Authentication, Integrity and Confidentiality

The CP6014 support 2 types of authentication for RMCP session connections: "None" and "Straight Password".

For RMCP+ session connections, the CP6014 support from Cipher ID 0 to Cipher Id 3. The following algorithms are supported:

- Authentication: RAKP-none, RAKP-HMAC-SHA1
- Integrity: None, HMAC-SHA1-96
- Confidentiality: None, AES-CBC-128

When RMCP authentication "NONE" or RMCP+ Cipher ID 0 is used, privilege level is limited to "User".

4.3.6.2 Users

Five users are available for IPMI Over LAN connections. The user 1 is defined by the IPMI specification and cannot be changed. The following tables show the pre-defined users. They can be changed using the proper IPMI commands .

Table 4-18:IPMI Users

User ID	User Name	Password	Can be modified	Privileges
1	NULL	NULL	No	User
2	“admin”	“admin”	Yes	Administrator
3	Undefined	Undefined	Yes	Undefined
4	Undefined	Undefined	Undefined	Undefined
5	Undefined	Undefined	Undefined	Undefined

4.3.7 Serial Over LAN support (SOL)

Serial Over LAN (SOL) is the name for the redirection of baseboard serial controller traffic over an IPMI Session. The IPMC has connections to the primary serial port connected to the front panel and to the Rear I/O Ethernet ports. The serial port is implemented in such way that if there is a cable connected to the RJ-45 connector, the traffic is directed to the cable and the IPMC only monitors traffic. If there is no cable connected, the traffic is directed to the IPMC. The CP6014 supports SOL payload within a RMCP+ connection as defined in the IPMI 2.0 specification.

To setup SOL, use the following procedure:

- Configure the IP address, Subnet Mask and Gateway address in the BIOS LAN configuration page.
- Set Active the LAN channel to use.
- In the BIOS menu Remote Access Configuration (See section 5.1), set the following parameters:

- Remote Access to "enabled".
- Primary Serial port number to COM1 or "both" for dual output (COM1 and COM2).
- Serial Port Mode to the desire speed.
- Flow control to "Software "or "hardware". (Flow control is required; do not use "None")
- Terminal type to the desired value.

The recommended IPMI Over Lan / Serial Over LAN tool for Linux is IPMITool. This utility is available from the following web site: http://ipmitool.sourceforge.net/index.html.

4.3.8 IPMC firmware upgrade

Kontron has participated with others as PICMG member group that has created the [HPM.1] Hardware Platform Management - IPM Controller Firmware Upgrade Specification. The current implementation of firmware upgrade on Kontron products is based on HPM.1 v1.0 of this specification. IPMC firmware can be updated through all the available channels and interfaces if proper privileges are acquired. On the CP6014, these include the IPMB, KCS, and LAN interface.

4.3.8.1 Firmware Upgrade Context

This section describes the firmware upgrade procedure context.

To perform a firmware upgrade, usually two applications are needed. These applications are:

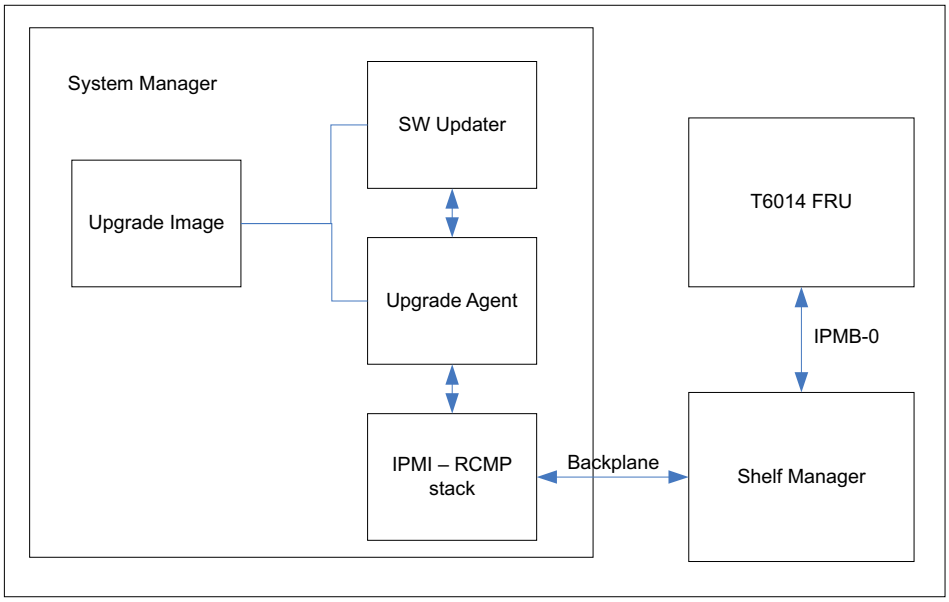
- The Upgrade Agent;
- The SW Updater;

The Upgrade Agent (UA) is a non-Kontron SW module, like ipmitool, performing independently the whole firmware upgrade procedure. This agent can be part of the System Manager Software to perform centralized upgrades for the whole system or cluster over the shelves. Upgrade Agent functionality shall be also part of the Shelf Manager functionality to perform upgrades of the FRUs and IPMCs at the shelf level. The Upgrade Agent implementation is out of this document scope.

The SW Updater is a non-Kontron application that can be a part of the SW platform and responsible for the SW updates. In the System Manager, this is the higher upgrade object provided by the SW Platform using the Upgrade Agent to perform upgrade procedure. Functionality of that object is out of the scope of this document.

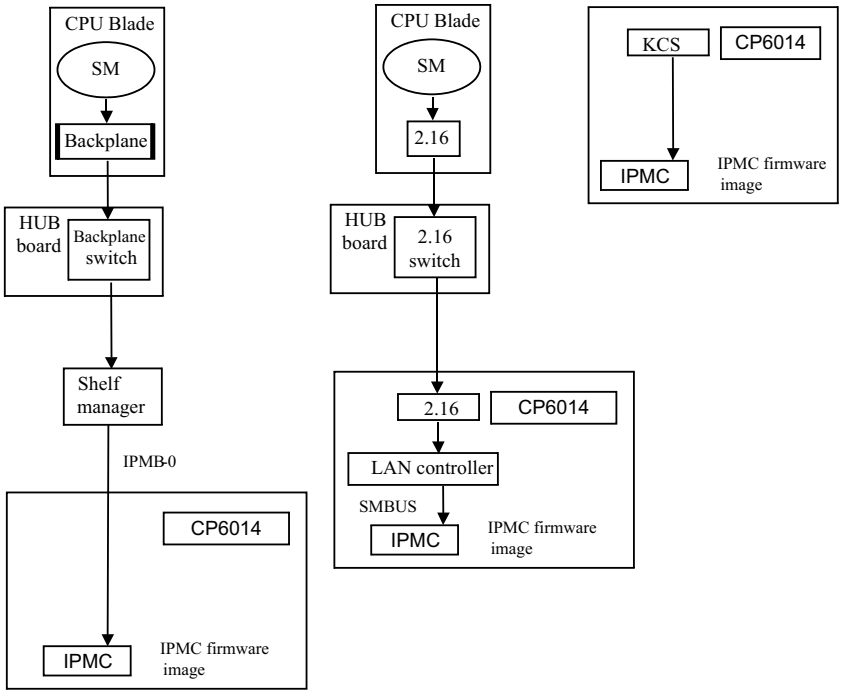
The following figure shows these two applications in the firmware upgrade context.

Figure 4-3:Firmware Upgrade



An Upgrade Agent can send upgrade related IPMI messages encapsulated to the RMCP messages to the Shelf Manager through the PICMG 2.16 backplane. When the Shelf Manager receives those messages, it forwards IPMI messages to the destination FRU through IPMB-0 bus. However, if the CP6014 payload is powered, it is possible to use IPMI Over LAN over the backplane to transfer messages directly to the IPMC. These two upgrade paths are illustrated below. The Upgrade Agent can also run directly on the target CP6014. This way, the Upgrade Agent can send firmware upgrade packet directly using the system interface (KCS).

Figure 4-4:Firmware Upgrade Paths



4.3.8.2 No Payload Impact

An upgrade of the IPMC firmware does not disturb the payload. All the necessary lines and status are kept to make sure that it is transparent for the payload.

4.3.8.3 Firmware Redundancy

Kontron implementation includes redundant firmware images. Thoses images allow a 'failsafe' firmware upgrade procedure, by supporting automatic rollback when the new firmware activation fails.

4.3.8.4 Commands definitions

This section defines the command used for the firmware upgrade procedure. The are specified within [HPM.1]

The table below shows the list of IPMI commands used during the upgrade procedure.

Table 4-19:List of IPMI commands used during the upgrade procedure

Firmware Upgrader Commands	HPM.1 Table	NetFn	CMD	Supported by Kontron
Get target upgrade capabilities	3-3	PICMG	2Eh	Yes
Get component properties	3-5	PICMG	2Fh	Yes
Backup components	3-8	PICMG	30h	No
Prepare components	3-9	PICMG	31h	Yes
Upload firmware block	3-10	PICMG	32h	Yes
Finish firmware upload	3-11	PICMG	33h	Yes
Get upgrade status	3-2	PICMG	34h	Yes
Activate firmware	3-12	PICMG	35h	Yes
Query self-test results	3-13	PICMG	36h	Yes
Query Rollback status	3-14	PICMG	37h	Yes
Manual Firmware Rollback	3-15	PICMG	38h	Yes

Kontron implementation supports all the commands defined in this table except the optional Backup components command. We do not support this command because of the firmware image redundancy and automatic rollback feature. In that case, the Backup command becomes useless.

Here is a general definition of each command. Complete commands definitions can be found in [HPM.1] document.

4.3.8.4.1 Get target upgrade capabilities command

This command is used to retrieve the IPMC upgrade capabilities, such as the current implemented components by the IPMC, automatic rollback support, IPMB accessibility, self-test support, etc. This is usually the first command called by the Upgrade Agent during the upgrade procedure.

4.3.8.4.2 Get component properties command

This command is used to retrieve the properties of a specific component, such as the Current version of the Active Copy, a description string of the component, the Rollback firmware version (Backup Copy), etc.

4.3.8.4.3 Backup components command

Minimal IPMC not supporting permanent redundant firmware images may use this command to backup the Active Copy before the new firmware upload. This command is not used by Kontron implementation since we are supporting the automatic rollback feature.

4.3.8.4.4 Prepare components command

This command is used to tell the IPMC to prepare to receive a new firmware image.

4.3.8.4.5 Upload firmware block command

This command is used to send the new firmware data to the IPMC. This command must be repeated until the entire firmware image is sent. The maximum number of byte sent per transaction is limited by the protocol requirements (such as the maximum message size defined for IPMB packets).

4.3.8.4.6 Finish firmware upload command

This command is used to inform the IPMC that all the bytes have been sent. The IPMC then verify the image integrity and set the appropriate memory space state to 'New'.

4.3.8.4.7 Get upgrade status command

This command is used to get the status of the last executed firmware command. Some command are identified as long duration command and the Get upgrade status command is used to know when the command is completed. Refer to [HPM.1] section 3.1 for more information on long duration command handling.

4.3.8.4.8 Activate firmware command

This command is used to activate the firmware stored in the memory space labeled as 'New'. If the activation fails, an automatic rollback is performed.

4.3.8.4.9 Query self-test results command

This command is used to retrieve the self-test results.

4.3.8.4.10 Query Rollback status command

This command is used to retrieve the Rollback status. It tells the Upgrade Agent if a rollback is in progress or occurred.

4.3.8.4.11 Manual firmware Rollback command

This command is used to initiate a manual rollback of the firmware. The Backup Copy (Previous Good) is restored as the Active Copy (Last Known Good) and become the running firmware on the IPMC.

4.3.9 Power Control

4.3.9.1 Payload Graceful Shutdown

The x86 implementation relies on ACPI for Payload Graceful Shutdown support.

The FPGA implements a virtual ACPI power button interface that is used by the IPMC to power down the payload. The IPMC also has access to a Hard Turn Off feature that allows it to turn off the power immediately.

The BIOS and OS uses the "Set ACPI Power State" API to inform the IPMC of the current/upcoming ACPI power state, the OS and System Manager can query the ACPI state using the "Get ACPI Power State" API.

The supported ACPI states are: Legacy Off, Legacy On, SoftOff/S5, SoftOff/S5 Override and Working/S0. In case none of these states are detected, the IPMC reports "unknown".

When a Payload reset is detected the ACPI state is automatically set to Legacy On.

4.3.10 Standard IPMI Watchdog

The hardware management layer implements a standardized 'Watchdog Timer' that can be used for a number of system timeout functions by system management software or BIOS.

The watchdog provides a configurable timeout from 100 millisecond to 6553, 5 seconds with 100 millisecond granularity and allows a pre-timeout interrupt from 0 to 255 seconds. Setting a timeout value of '0' allows the selected timeout action to occur immediately. This provides a standardized means for System Management Software on the IPMB to perform emergency recovery actions. This timeout can be set using the standard IPMI command "Set Watchdog Timer" defined in section 21.6 of IPMI v1.5 specification.

The IPMC implement the standard "IPMI Watchdog 2" sensor. This sensor type (23h) is available for error reporting (See sensor list), each time a pretimeout or a timeout occurs, an event is sent to the ShMC SEL.

The pre-timeout actions supported are: none and messaging interrupt (same IRQ as KCS interface) while the timeout action includes: none, reset, power down and power cycle.

4.3.10.1 Standard IPMI Watchdog Phase

The complete startup and possibly execution process of CPU (base on the operating system support) is guarded using external watchdog timers implemented by the hardware management subsystem under the IPMC. There are 4 distinctive watchdog timers that run during different phases of the system startup and operation.

The watchdog timer trigers a specific action when expired. The action is dependent on previous reset types (either warm or cold) and on watchdog type.

Table 4-20:Watchdogs

WD Name	When started	Description	Typical trigger period	Strobed	Action when triggered/bite	Stopped
FRB2	Watchdog started automatically on reset of CPU by IPMC.	Guards boot bloc initialization and early BIOS execution. Standard IPMI watchdog is used with "timer use" field automatically set to "FRB2" (fault resilient booting level 2) after a reset.	15 secs.	Never	Reset, Send IPMI watchdog event.	After Post WD is started
Post	Watchdog started by BIOS during BIOS boot bloc initialization.	Guards BIOS execution. Standard IPMI watchdog is used with "timer use" field set to "BIOS POST" by the BIOS.	150 seconds typical, transitory set to 300 seconds under long task such as memory check	Never	Send IPMI WD event, Send IPMI POST event.	After OS WD is started
OS Load	Watchdog started by BIOS before execution is passed to OS.	Guards BIOS preparation for OS loading, OS initialization and execution. Enable by default but configurable by BIOS setup menu. Standard IPMI watchdog is used with "timer use" field set to "OS Load" by the BIOS.	150 seconds	Never	Send IPMI Watchdog event.	After SMS/OS WD is started or manually shutdown from OS
SMS/OS	Watchdog started after successful OS initialization and startup of applications.	Guards CPU application execution. Standard IPMI watchdog is used with "timer use" field set to "SMS OS Watchdog" by an OS component.	1 second (this is OS specific)	Periodically by OS watchdog daemon	Power down or Power Cycle, Send IPMI Watchdog event.	On any CPU reset

The trigger periods defined in that table are typical trigger periods. The BIOS implements a user selectable trigger period in the CMOS setup menu.

4.3.10.2 IPMC boot image Watchdog

Include in the standard IPMI watchdog, the IPMC is monitoring the boot process automatically. In case of boot failure (BIOS hang), the IPMC is automatically cold resetting the payload after 15 seconds.

4.3.11 External Drivers, Applications & Utilities

Kontron doesn't develop any utility, drivers or applications. Kontron is part of the IPMITool project (in Linux). Kontron contributes to this utility to provide functionality and compatibility to our customers. Since IPMC is fully compliant to the IPMI 1.5 and 2.0 specifications, the user can use any third party driver, applications and utilities available on the market.

4.3.11.1 Host Interface (KCS) Driver

Kontron implements a KCS interface to communicate with the IPMC from the payload. On the payload side, a KCS driver is required to interface with the IPMC host interface.

4.3.11.1.1 Linux

In Linux, the OpenIPMI package is suggested and can be used to interface with the KCS interface. Development and most of the testing have been done using this package.

More information about OpenIPMI can be found using the following link:

http://ipmitool.sourceforge.net/.

4.3.11.2 Applications

4.3.11.2.1 Linux

Under Linux, IPMITool is the proposed applications to communicates with the IPMC. IPMITool is a utility for managing and configuring devices that support the Intelligent Platform Management Interface (IPMI) version 1.5 and version 2.0 specifications.

IPMITool is compatible with many interfaces and driver including OpenIPMI (Host KCS Interface), IPMI-Over-LAN (IOL) 1.5 and IPMI-Over-LAN 2.0. It is also possible to bridge commands from any interface to the IPMB bus to access another IPMC controller on the chassis.

IPMITool also offer a Serial-Over-LAN(SOL) Terminal to remotely access to the target serial port. This feature is very useful to access the BIOS or log into the target. For more information regarding SOL, see the IPMI-Over-LAN(IOL) section.

IPMITool is most often used for the development and testing. More information, sources and binary of IPMITool can be found at: http://ipmitool.sourceforge.net/.

Chapter 5

Software Setup

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5. Software Setup

5.1 AMI BIOS Setup Program

All relevant information for operating the board and connected peripherals is stored in the CMOS memory. A battery-backed up memory holds this information when the board is powered off, the BIOS Setup program is required to make changes to the setup.

5.1.1 Accessing the BIOS Setup Utility

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the CP6014 SBC. It uses the AMI Setup program, a setup utility in flash memory that is accessed by pressing the <Del> or <F4> on a remote keyboard at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

To run the AMI Setup program incorporated in the ROM BIOS:

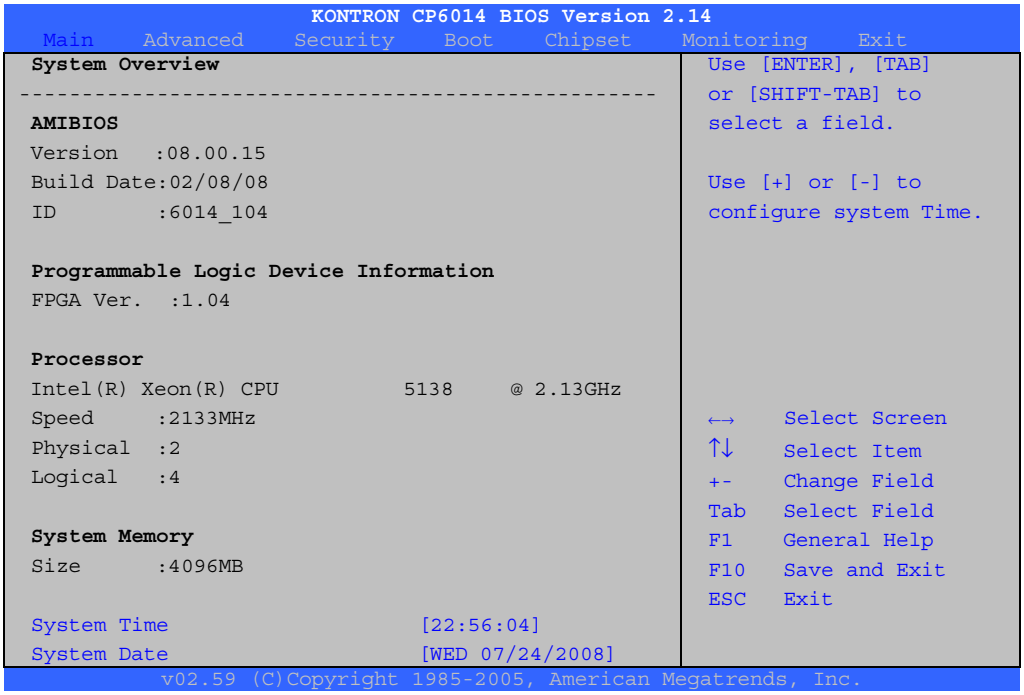
- Turn on or reboot the system.
- When you get the following messages, hit <Del> or <F4> on a remote keyboard key to enter SETUP.

```
AMIBIOS(C)2006 American Megatrends, Inc.
KONTRON CP6014 BIOS Version 2.14
CPU : Intel(R) Xeon(R) CPU            5138  @ 2.13GHz
 Speed : 2.13 GHz    Physical : 2    Logical : 4

Press DEL to run Setup (F4 on Remote Keyboard)
Press F12 if you want to boot from the network
Press F11 for BBS POPUP  (F3 on Remote Keyboard)
Initializing USB Controllers .. Done.
CORE:DDR Frequencies: BUSCLK=266 MHz, DDR=533 MHz.
2048MB OK
USB Device(s): 1 Keyboard, 1 Storage Device
Auto-Detecting Sec Slave...IDE Hard Disk
Sec Slave  : ST9120822SB  3.BSB
             Ultra DMA Mode-5, S.M.A.R.T. Capable and Status OK
Auto-detecting USB Mass Storage Devices ..
Device #01 : Generic STORAGE DEVICE
01 USB mass storage devices found and configured.
```

The main menu of the AMI BIOS CMOS Setup Utility appears on the screen.

Figure 5-1:BIOS Setup Menu Display



Setup Default values provide optimum performance settings for all devices and system features.

Note:
The CMOS setup option described in this section is based on BIOS Version 2.14 The options and default settings may change in a new BIOS release.

CAUTION
These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

Note:
All options in Bold are the default settings.

5.1.2 Menu Bar

The Menu Bar at the top of the window lists these selections:

Table 5-1:BIOS Setup Menu Bar

Menu Selection	Description
Main	Use this menu for basic system configuration.
Advanced	Use this menu to set the Advanced Features available on your system.
Security	Use this menu to configure Security features.
Boot	Use this menu to determine the booting device order.
Chipset	Use this menu to configure Chipset features.
Monitoring	Use this menu to configure Monitoring features.
Exit	Use this menu to choose Exits option.

Use the left and right arrows keys to make a selection.

5.1.2.1 Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates.

Table 5-2:BIOS Setup Legend Bar

Key	Function
<F1>	General Help windows
<Esc>	Exit this menu.
--> arrow keys	Select a different menu.
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to top or bottom of window.
<->	Select the Previous Value for the field.
<+>	Select the Next Value for the field.
<F2> and <F3>	Change colors used in Setup.
<F7>	Disacard the changes for all menus.
<F9>	Load the Optimal Default Configuration values for all menus.
<F10>	Save and exit.
<Enter>	Execute Command, display possible value for this field or Select the sub-menu.

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-and-minus value keys to select a value for that field. To save the values displayed in all menus, use the save commands in the Exit menu.

To display a submenu, use the arrow keys to move the cursor to the submenu you want. Then press <Enter>.

5.1.2.2 Field Help Window

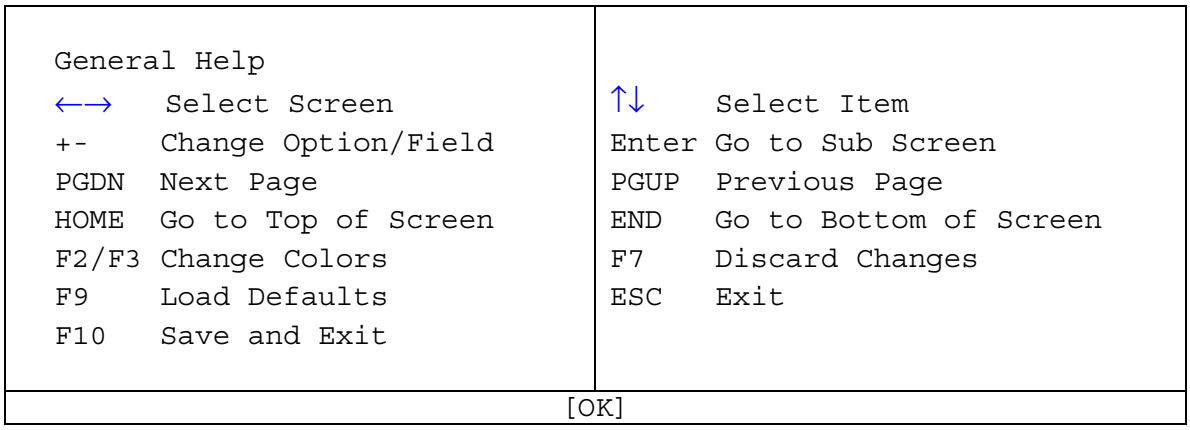
The help window on the right side of each menu displays the help text for the selected field.

It updates as you move the cursor to each field.

5.1.2.3 General Help Windows

Pressing <F1>on any menu brings up the General Help window that describes the legend keys and their alternates:

Figure 5-2:BIOS Setup General Help Windows



5.1.3 Main Menu

Feature	Options	Description	Setup Help
Version	X.YY	Displays the BIOS core version.	N/A, display only.
Build Date	YYMMDD	Displays the BIOS build date in the format YYMMDD.	N/A, display only.
ID	BIOS ID code	Displays the BIOS identification code. The first 5 characters uniquely identify the board. The last 3 digits correspond to BIOS version in the format X.YZ.	N/A, display only.
FPGA Ver.	X.YY	Displays the FPGA version.	N/A, display only.
	CPU Brand string	Reads and display the 48 bytes CPU Brand string from the CPU MSR.	N/A, display only.
Speed	X Ghz	Displays the current processor core(s) speed.	N/A, display only.
Physical	x	Displays the number of physical processors.	N/A, display only.
Logical	x	Displays the number of logical processors.	N/A, display only.
Size	X MB	Displays system memory size.	N/A, display only.
System Time	HH:MM:SS	Set the system time.	Use [ENTER], [TAB] or [SHIFT-TAB] to select a field. Use [+] or [-] to configure system Time.
System Date	MM/DD/YYYY	Set the system date.	Use [ENTER], [TAB] or [SHIFT-TAB] to select a field. Use [+] or [-] to configure system Date.

5.1.4 Advanced Menu

Feature	Options	Description	Setup Help
CPU Configuration	N/A	Press Enter to go to sub screen "CPU Configuration".	Configure CPU.
Drive Configuration	N/A	Press Enter to go to sub screen "Drive Configuration"	Configure the Drive device(s).
USB Configuration	N/A	Press Enter to go to sub screen "USB Configuration".	Configure the USB support.
ACPI Configuration	N/A	Press Enter to go to sub screen "ACPI Configuration".	Section for Advanced ACPI Configuration.
Event Log Configuration	N/A	Press Enter to go to sub screen "Event Log Configuration".	Mark as read, Clear or View Event Log statistics.
MPS Configuration	N/A	Press Enter to go to sub screen "MPS Configuration".	Configure the Multi-Processor Table.
On-board Devices Configuration	N/A	Press Enter to go to sub screen "On-board Devices Configuration".	Use this section to Enable/Disable special on-board devices and expansions ROMs.
Remote Access Configuration	N/A	Press Enter to go to sub screen "Remote Access Configuration".	Configure Remote Access.

5.1.4.1 CPU Configuration sub-menu

Feature	Options	Description	Setup Help
Module Version	CPU module version.	Displays the BIOS current CPU module version.	N/A, display only.
Manufacturer	Intel	Displays the processor manufacturer name.	N/A, display only.
	CPU Brand string	Reads and display the 48 bytes CPU Brand string from the CPU MSR.	N/A, display only.
Frequency	X Ghz	Displays the current processor core(s) speed.	N/A, display only.
FSB Speed	X Ghz	Displays the current processor Front Side bus speed to the chipset.	N/A, display only.
Cache L1	X KB	Displays amount of Level 1 processor cache per processor.	N/A, display only.
Cache L2	X KB/MB	Displays amount of Level 2 processor cache per processor.	N/A, display only.
Ratio Status	Unlocked (Min:xx, Max:xx)	If processor ratio is not locked, displays the minimum and maximum ratios allowed. Option is hidden if processor ratio is locked.	N/A, display only.
Ratio Actual Value	x	Displays current processor FSB multiplier value (FSB time ratio = processor core speed).	N/A, display only.
Ratio CMOS Setting	x	Selects the processor FSB ratio value (FSB x ratio = processor core speed).	Sets the ratio between CPU Core Clock and the FSB Frequency. NOTE: If an invalid ratio has been entered to this field, BIOS will restore it to previous state.
Hardware Prefetcher	Disabled **Enabled**	The hardware prefetcher looks at streams of data. The hardware prefetcher assumes that if a line A and A+1 were requested, then line A+2 also will be requested. The data is prefetched into L2 from external memory. Disabling of the hardware prefetcher may impact processor performance. Default should be enabled. Optionally for DP/MP servers, the default may be set based on performance results observed during platform validation and testing with standard workloads.	This should be enabled in order to enable or disable the Hardware Prefetcher Disable Feature.
Adjacent Cache Line Prefetch	Disabled **Enabled**	When enabled the Adjacent Cache Line Prefetcher fetches both cache lines that comprise a cache line pair (128 bytes) when it determines required data is not currently in its cache. When the Adjacent Cache Line Prefetcher is disabled, the processor will only fetch the cache line (64 bytes) that contains the data currently required by the processor. Note: Single processor platforms should enable it. It is recommended that server platforms disable it. Optionally for DP/MP servers, the default may be set based on performance results observed during platform validation and testing with standard workloads.	This should be enabled in order to enable or disable the Adjacent Cache Line Prefetch Disable Feature.
Max CPUID Value Limit	**Disabled** Enabled		Disabled for WindowsXP

Feature	Options	Description	Setup Help
Intel(R) Virtualization Tech	Disabled **Enabled**		When enabled, a VMM can utilize the additional HW Caps. provided by Intel(R) Virtualization Tech. Note: A full reset is requried to change the setting.
Execute-Disable Bit Capability	Disabled **Enabled**	Execute Disable Bit allows the processor to classify areas in memory by where application code can execute and where it cannot preventing certain classes of malicious buffer overflow attacks when combined with a supporting operating system.	When disabled, force the XD feature flag to always return 0.
PECI	Disabled **Enabled**	CPU have Platform Environmental Control Interface (PECI) support. Enable PECI when the CPU supports it.	When enabled, enables PECI interface.
Intel(R) SpeedStep(tm) tech	Disabled **Enabled**	Enables Intel(R) SpeedStep(tm) technology for usage by OS.	Disable: Disable GV3 Enable: Enable GV3

5.1.4.2 *Drive Configuration sub-menu*

Feature	Options	Description	Setup Help
SATA#1 Configuration	Disabled Compatible **Enhanced**		Disabled: Disables the integrated IDE controller. Compatible: Enables up to two IDE channels for OS requiring legacy IDE operation. Enhanced (or Native): Enables all SATA and PATA resources.
SATA Port 0 (PM)	N/A	Press Enter to go to sub screen "SATA Port 0 (PM)"	While entering setup, BIOS auto detects the presence of IDE devices. this displays the status of auto detection of IDE devices.
SATA Port 2 (PS)	N/A	Press Enter to go to sub screen "SATA Port 2 (PS)"	While entering setup, BIOS auto detects the presence of IDE devices. this displays the status of auto detection of IDE devices.
SATA Port 3 (SS)	N/A	Press Enter to go to sub screen "SATA Port 3 (SS)"	While entering setup, BIOS auto detects the presence of IDE devices. this displays the status of auto detection of IDE devices.

5.1.4.2.1 SATA Port 0 (PM)

Feature	Options	Description	Setup Help
Device	“variable”		N/A, display only.
Vendor	“variable”		N/A, display only.
Size	“variable”		N/A, display only.
Ultra DMA	“variable”		N/A, display only.
S.M.A.R.T.	“variable”		N/A, display only.
Type	Not Installed **Auto**		Select the type of device connected to the system.

5.1.4.2.2 SATA Port 2 (PS)

Feature	Options	Description	Setup Help
Device	“variable”		N/A, display only.
Vendor	“variable”		N/A, display only.
Size	“variable”		N/A, display only.
Ultra DMA	“variable”		N/A, display only.
S.M.A.R.T.	“variable”		N/A, display only.
Type	Not Installed **Auto**		Select the type of device connected to the system.

5.1.4.2.3 SATA Port 3 (SS)

Feature	Options	Description	Setup Help
Device	“variable”		N/A, display only.
Vendor	“variable”		N/A, display only.
Size	“variable”		N/A, display only.
Ultra DMA	“variable”		N/A, display only.
S.M.A.R.T.	“variable”		N/A, display only.
Type	Not Installed **Auto**		Select the type of device connected to the system.

5.1.4.3 USB Configuration sub-menu

Feature	Options	Description	Setup Help
Module Version -	USB module version.	Displays the BIOS current USB module version.	N/A, display only.
USB Devices Enabled	List USB device(s) detected.	This feature appears when the BIOS POST has detected USB device(s).	N/A, display only.
USB 2.0 Controller Mode	FullSpeed **HiSpeed**	Configures the USB 2.0 Controller in HiSpeed (480 Mbps) or FullSpeed (12 Mbps).	Configures the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps).
BIOS EHCI Hand-Off	Disabled **Enabled**	A workaround for OSes without EHCI hand-off support can be enabled/disabled. The EHCI ownership change should be claimed by an EHCI driver.	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.
USB Mass Storage Device Configuration	N/A	Press Enter to go to sub screen "USB Mass Storage Device Configuration".	Configure the USB Mass Storage Class Devices.

5.1.4.3.1 USB Mass Storage Device Configuration sub-menu

Feature	Options	Description	Setup Help
Device #1	USB device description	Displays the 1st USB mass storage device description.	N/A, display only.
Emulation Type	Auto Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).
Device #2	USB device description	Displays the 2nd USB mass storage device description.	N/A, display only.
Emulation Type	Auto Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).
Device #3	USB device description	Displays the 3rd USB mass storage device description.	N/A, display only.
Emulation Type	Auto Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).
Device #4	USB device description	Displays the 4th USB mass storage device description.	N/A, display only.

Feature	Options	Description	Setup Help
Emulation Type	Auto Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).
Device #5	USB device description	Displays the 5th USB mass storage device description.	N/A, display only.
Emulation Type	Auto Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).
Device #6	USB device description	Displays the 6th USB mass storage device description.	N/A, display only.
Emulation Type	Auto Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

5.1.4.4 ACPI Configuration sub-menu

Feature	Options	Description	Setup Help
Advanced ACPI Configuration	N/A	Press Enter to go to sub screen "Advanced ACPI Configuration".	Advanced ACPI Configuration settings. Use this section to configure additional ACPI options.
Chipset ACPI Configuration	N/A	Press Enter to go to sub screen "Chipset ACPI Configuration".	Chipset ACPI related Configuration settings.

5.1.4.4.1 Advanced ACPI Configuration sub-menu

Feature	Options	Description	Setup Help
ACPI Version Features	ACPI v1.0 ACPI v2.0 **ACPI v3.0**	Version 1.0 only supports RSDP pointers to 32-bit Fixed System Description Tables. Version 2.0 enables RSDP pointers to 64-bit Fixed System Description Tables. Version 3.0 improves processor, PCI Express and SATA support.	Enable RSDP pointers to 64-bit Fixed System Description Tables. Different ACPI version has some addition.
ACPI APIC support	Disabled **Enabled**	Support for ACPI APIC table pointer to Root System Description Table. RSDT pointer list can be enabled/disabled.	Include ACPI APIC table pointer to RSDT pointer list.
Headless mode	Disabled **Enabled**	Headless operation mode through ACPI can be enabled/disabled. When enabled, the Serial Port Console Redirection "SPCR" table is generated to inform OS about the settings of the serial port console set in BIOS.	Enable / Disable Headless operation mode through ACPI.

5.1.4.4.2 Chipset ACPI Configuration sub-menu

Feature	Options	Description	Setup Help
APIC ACPI SCI IRQ	**Disabled** Enabled	IRQ9 if APIC is not used for SCI. IRQ20 is only available for SCI if APIC is enabled.	Enable/Disable APIC ACPI SCI IRQ.

5.1.4.5 Event Log Configuration sub-menu

Feature	Options	Description	Setup Help
View Event Log	Enter	View all unread events in the Event Log.	View all unread events on the Event Log.
Mark all events as read	Enter	Mark all unread events as read in the Event Log.	Mark all unread events as read.
Clear Event Log	Enter	Discard all events in the Event Log.	Discard all events in the Event Log.
ECC Event Logging	Disabled **Enabled**	ECC Event Logging can be enabled/disabled.	Enable or Disable ECC Event Logging

5.1.4.6 MPS Configuration sub-menu

Feature	Options	Description	Setup Help
MPS Revision	1.1 **1.4**	Configures the Multiprocessor Specification (MPS) revision level. Some operating systems might require revision 1.1 for compatibility reasons.	Configures the Multiprocessor Specification (MPS) revision level. Some operating systems will require revision 1.1 for compatibility reasons.

5.1.4.7 On-Board Devices Configurations Settings sub-menu

Feature	Options	Description	Setup Help
Ethernet LAN0 Expansion ROM	Disabled **Enabled**	The LAN0 interface PXE Expansion ROM can be enabled/disabled. If disabled, remote LAN boot via the LAN0 interface is not available to boot the system.	Enabled: Initializes cPCI-J3 LAN0 PXE expansion ROM. Disabled: cPCI-J3 LAN0 PXE expansion ROM not used. If disabled, remote LAN0 boot via cPCI J3 is not available to boot the system.
Ethernet LAN1 Expansion ROM	Disabled **Enabled**	The LAN1 interface PXE Expansion ROM can be enabled/disabled. If disabled, remote LAN boot via the LAN1 interface is not available to boot the system.	Enabled: Initializes cPCI-J3 LAN1 PXE expansion ROM. Disabled: cPCI-J3 LAN1 PXE expansion ROM not used. If disabled, remote LAN1 boot via cPCI J3 is not available to boot the system.
Front plate LAN Expansion ROM	**Enabled** Disabled	The front plate GbE interface PXE Expansion ROM can be enabled/disabled. If disabled, remote LAN boot via the front plate GbE interface is not available to boot the system.	Enabled: Initializes front plate GbE PXE expansion ROM. Disabled: front plate GbE PXE expansion ROM not used. If disabled, remote boot via front plate GbE is not available to boot the system.
PMC Expansion ROM(s)	Disabled **Enabled**	Enables or disables PMC Expansion ROM(s), if any detected. If disabled, PMC Expansion ROM(s) code will not be executed during POST.	Enabled: Initializes PMC expansion ROM(s). Disabled: PMC expansion ROM(s) not used.
XMC Expansion ROM(s)	Disabled **Enabled**	Enables or disables XMC Expansion ROM(s), if any detected. If disabled, XMC Expansion ROM(s) code will not be executed during POST.	Enabled: Initializes XMC expansion ROM(s). Disabled: XMC expansion ROM(s) not used.
On-board Video Output	Front Panel **RTM**		Select where on-board video controller will be outputted.
Boot Graphic Adapter Priority	**Onboard VGA**		Select which graphics controller tu use as the primary boot device.

Note:
Front plate LAN Expansion ROM and On-board Video Output menus might not be available when the board is ordered with the Rear Access option.

5.1.4.8 Remote Access Configuration sub-menu

Feature	Options	Description	Setup Help
Remote Access	Disabled **Enabled**	Configures console redirection. Disabling remote access will hide all related features in this sub-menu.	Select Remote Access type.
Serial port number	**COM1** COM2	Configures serial port for console redirection. Also used for Headless operation mode through ACPI.	Select Serial Port for console redirection. Make sure the selected port is enabled.
Base Address, IRQ	IO, IRQ	Displays the hardware address of the COM port used for the console.	N/A, display only.
Serial Port Mode	**115200 8,n,1** 57600 8,n,1 38400 8,n,1 19200 8,n,1 09600 8,n,1	Configures the serial Baud rate for the serial ports. 8 data bits, no parity and 1 stop bit parameters are fixed.	Select Serial Port settings.
Flow Control	None **Hardware** Software	Configures flow control for console redirection for both serial ports.	Select Flow Control for console redirection.
Redirection After BIOS POST	Disabled Boot Loader **Always**	Selects how the serial redirection done by the BIOS will operate after the POST.	Disable: Turns off the redirection after POST Boot Loader: Redirection is active during POST and during Boot Loader. Always: Redirection is always active. (Some OSs may not work if set to Always)
Terminal Type	**ANSI** VT100 VTUTF8	Configures the type of console emulation used for both serial ports.	Select the target terminal type.
VT-UTF8 Combo Key Support	Disabled **Enabled**	VT-UTF8 adds escape sequences for F1 to F12 and most other control keys on a keyboard.	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.

5.1.5 Security menu

Feature	Options	Description	Setup Help
Supervisor Password	Installed **Not Installed**	Indicates the status of the Supervisor Password.	N/A, display only.
User Password	Installed **Not Installed**	Indicates the status of the User Password.	N/A, display only.
Change Supervisor Password	Enter	The supervisor password can be installed or changed.	Install or Change the password.
User Access Level	No Access View Only Limited Full Access	Controls the user access level to the BIOS Setup utility. Supervisor has full access to the BIOS Setup utility. No Access: Prevents user access to the setup utility. View Only: Allows read only user access to the setup utility i.e. none of the fields ca	LIMITED: allows only limited fields to be changed such as Date and Time. NO ACCESS: prevents User access to the Setup Utility. VIEW ONLY: allows access to the Setup Utility but the fields can not be changed. FULL: allows any field to be changed except the Supervisor password.
Change User Password	Enter	The user password can be installed or changed.	Install or Change the password.
Clear User Password	Enter	Immediately clears the User password.	Immediately clears the User password.
Password Check	Setup Always	Selects when the password is check during POST.	Setup: Check password while invoking setup. Always: Check password while invoking setup as well as on each boot.
Boot Sector Virus Protection	**Disabled** Enabled		Enable/Disable Boot Sector Virus Protection.

5.1.6 Boot menu

Feature	Options	Description	Setup Help
Boot Settings Configuration	N/A	Press Enter to go to sub screen "Boot Settings Configuration".	Configure Settings during System Boot.
Boot Device Priority	N/A	Press Enter to go to sub screen "Boot Device Priority".	Specifies the Boot Device Priority sequence.
Hard Disk Drives	N/A	Press Enter to go to sub screen "Hard Disk Drives".	Specifies the Boot Device Priority sequence from available Hard Drives.
Removable Drives	N/A	Press Enter to go to sub screen "Removable Drives".	Specifies the Boot Device Priority sequence from available Removable Drives.
CD/DVD Drives	N/A	Press Enter to go to sub screen "CD/DVD Drives".	Specifies the Boot Device Priority sequence from available CD/DVD Drives.
USB Drives	N/A	Press Enter to go to sub screen "USB Drives".	Specifies the Boot Device Priority sequence from available USB Drives.
Network Drives	N/A	Press Enter to go to sub screen "Network Drives".	Specifies the Boot Device Priority sequence from available Network Drives.
Other Drives	N/A	Press Enter to go to sub screen "Other Drives".	Specifies the Boot Device Priority sequence from available Other Drives.

5.1.6.1 Boot Settings Configuration sub-menu

Feature	Options	Description	Setup Help
Quick Boot	Disabled **Enabled**	Allows/denies skipping the memory tests.	Allows BIOS to skip certain tests while booting. The System Configuration Summary will be skipped. This will decrease the time needed to boot the system.
Retry Boot Sequence	**Enabled**		Enable this option to retry the boot sequence until a successful boot (infinite retries)
Save CMOS in FLASH	Disabled **Enabled**	The CMOS content can be saved to NVRAM in case the CMOS power is lost. POST will restore CMOS from NVRAM (if valid, else from build time default values) when CMOS checksum is bad.	Saving CMOS memory content into Flash Memory will prevent loosing CMOS options when battery fails.
Clear NVRAM	**No** Yes	BIOS stores information about PCI devices scanned and boot devices in NVRAM. Its content may no longer be valid and this may result in unexpected behaviors (this sometimes happens when there are many changes with devices connected to the system).	Clear NVRAM during System Boot.

5.1.6.1.1 Boot Device Priority sub-menu

Feature	Options	Description	Setup Help
1st Boot	Type: Boot device	Specifies the priority of the available boot sources. The list includes USB CD ROM, USB Hard Drive, Hard Drive and PXE. Other supported devices might be dynamically added to the list.	Specifies the boot sequence from the available devices. A device enclosed in parenthesis has been disabled in the corresponding type menu.
Nth Boot	Type: Boot device	Specifies the priority of the available boot sources. The list includes USB CD ROM, USB Hard Drive, Hard Drive and PXE. Other supported devices might be dynamically added to the list.	Specifies the boot sequence from the available devices. A device enclosed in parenthesis has been disabled in the corresponding type menu.

5.1.6.2 Hard Disk Drives sub-menu

Feature	Options	Description	Setup Help
1st HDD	Hard Disk Drive description	Specifies the boot priority of the available Hard Disk devices.	Specifies the boot sequence from the available devices.
Nth HDD	Hard Disk Drive description	Specifies the boot priority of the available Hard Disk devices.	Specifies the boot sequence from the available devices.

5.1.6.3 Removable Drives sub-menu

Feature	Options	Description	Setup Help
1st RM	Removable drive description	Specifies the boot priority of the available Removable devices.	Specifies the boot sequence from the available devices.
Nth RM	Removable drive description	Specifies the boot priority of the available Removable devices.	Specifies the boot sequence from the available devices.

5.1.6.4 CD/DVD Drives sub-menu

Feature	Options	Description	Setup Help
1st C/D	CD or DVD drive description	Specifies the boot priority of the available CD or DVD devices.	Specifies the boot sequence from the available devices.
Nth C/D	CD or DVD drive description	Specifies the boot priority of the available CD or DVD devices.	Specifies the boot sequence from the available devices.

5.1.6.5 USB Drives sub-menu

Feature	Options	Description	Setup Help
1st USB	USB drive description	Specifies the boot priority of the available USB disk devices.	Specifies the boot sequence from the available devices.
Nth USB	USB drive description	Specifies the boot priority of the available USB disk devices.	Specifies the boot sequence from the available devices.

5.1.6.6 Network Drives sub-menu

Feature	Options	Description	Setup Help
1st PXE	Network drive description	Specifies the boot priority of the available Network disk devices.	Specifies the boot sequence from the available devices.
Nth PXE	Network drive description	Specifies the boot priority of the available Network disk devices.	Specifies the boot sequence from the available devices.

5.1.6.7 Other Drives sub-menu

Feature	Options	Description	Setup Help
1st BEV	"Other" drive description	Specifies the boot priority of any other available devices (other than Hard Disk, Removable, CD/DVD, USB disk or Network).	Specifies the boot sequence from the available devices.
Nth BEV	"Other" drive description	Specifies the boot priority of any other available devices (other than Hard Disk, Removable, CD/DVD, USB disk or Network).	Specifies the boot sequence from the available devices.

5.1.7 Chipset menu

Feature	Options	Description	Setup Help
Spread Spectrum Clocking Mode	**Enabled** Disabled	Allows BIOS to set Clock Spread Spectrum for EMI (electromagnetic interference) control.	Allows BIOS to Set Clock Spread Spectrum for EMI Control.
Northbridge Configuration	N/A	Press Enter to go to sub screen "Northbridge Configuration".	Configure North Bridge features.
Southbridge Configuration	N/A	Press Enter to go to sub screen "Southbridge Configuration".	Configure South Bridge features.

5.1.7.1 Northbridge Configuration sub-menu

Feature	Options	Description	Setup Help
Crystal Beach / DMA	Disabled **Enabled**	DMA Controller can be enabled/disabled.	Crystal Beach / DMA configuration.
MCH Channel Mode	Channel Sequencing **Channel Interleave** Single Channel 0	The system address space must be interleaved between channels to distribute memory traffic and improve system performance.	Sequencing: allocates address channel 0 then 1. Interleaving: interleaves channel across channels. Single Channel: forces single ch-0.
Patrol Scrubbing	Disabled **Enabled**	The scrub unit starts at DIMM Rank 0/Address 0 upon reset. Every 16k core cycles the unit will scrub one cache line and then increment the address one cache line provided that back pressure or other internal dependencies (queuing, conflicts etc) do not prolong the issuing of these transactions to DDR. Using this method, the memory behind the MCH Chipset can be completely scrubbed every day at least once (estimate).	ECC patrol scrub enable/ disable.
Demand Scrubbing	Disabled **Enabled**	Correctable read data will be corrected to the requestor and scrubbed in memory. This adds an extra cycle of latency to accomplish the correction.	ECC demand scrub enable/disable.
Dynamic Calibration	Disabled **Enabled**	When this setting is enabled, the board will start faster only if no memory change has been detected. This allows quicker boot when memory has been calibrated. Note: the fist boot with uncalibrated memory will takes 15 more seconds.	This feature allows the memory interface to calibrate quickly by using the stored calibration data from a previous power on. If enabled, CMOS must be cleared if memory configuration changes
Read Completion Coalescing	Disabled Enabled **Auto**	PCI Express read completion returns 64 bytes or less if disabled, 128 bytes completion combining if enabled. When set to Auto, 128 bytes completion is set unless device read completion was already set.	Read returns of > 64B.

5.1.7.2 Southbridge Configuration sub-menu

Feature	Options	Description	Setup Help
USB 2.0 Controller	**Enabled** Disabled	This can be used to force UHCI instead of EHCI mode of operation. The speed of the USB device(s) will be reduced, but it may help to boot the system.	Disabled will turn off the USB 2.0 controller. USB "Full Speed"is still available.
Restore on AC Power Loss	Power Off **Power On** Last State		Power Off: Keep power off until reinsertion Last State: Restore previous power state Power On: Restore power to the board.

5.1.8 Monitoring menu

Feature	Options	Description	Setup Help
IPMI Configuration	N/A	Press Enter to go to sub screen "IPMI Configuration".	IPMI configuration including server monitoring and event log.
Watchdog Configuration	N/A	Press Enter to go to sub screen "Watchdog Configuration".	Configure Watchdog
FPGA IRQ	**Disabled** IRQ5 IRQ7		Select the FPGA IRQ number for enabled events.
Display & Clear Reset History	Disabled **Enabled**		When Enabled, displays in the System Configuration Summary the type of Reset detected by the FPGA. The History bits in FPGA will also be cleared.

5.1.8.1 IPMI Configuration sub-menu

Feature	Options	Description	Setup Help
Status of IPMC	Working or Not Working	Indicate if the BIOS was able to communicate with the IPMC.	N/A, display only.
View IPMC System Event Log	N/A	Press Enter to go to sub screen "View IPMC System Event Log".	View all events in the IPMC Event Log. It will take a max. of 15 seconds to read all IPMC SEL records.
Clear IPMC System Event Log	N/A	Press Enter to go to sub screen "Clear IPMC System Event Log".	Clear all events in IPMC System Event Log.
Set LAN Configuration	N/A	Press Enter to go to sub screen "Set LAN Configuration".	InPut for Set LAN Configuration command. See IPMI 1.5 Spec, table 19.1 NOTE: - Each question in this group may take considerable amount of time. (direct access to IPMC)
IPMI Device and Firmware Information	N/A	Press Enter to go to sub screen "IPMI Device and Firmware Information".	View IPMI Device and Firmware Information
System Management	N/A	Press Enter to go to sub screen "System Management".	Display FRU board and product information, Display IPMC device and FW information.
KCS-SMS IRQ	Disabled IRQ 10 **IRQ 11**	Selects the SMS IRQ number.	Select Management Controller IRQ for the System Management Software (SMS).

Feature	Options	Description	Setup Help
Dual Port IPMB Redundancy	Disabled **Enabled**		Disabled: IPMB0 (Intelligent Platform Management Bus 0) and IPMB1 operate as separate channels Enabled: IPMB1 is hidden behind IPMB0 and used as a redundancy channel
Management Controller Config.	Baseboard **Satellite**	If the chassis is not populated with a shelf-manager, then the system integrator must elect a BMC within the pool of IPMC present in the chassis. In BMC mode, the blade only covers the IPMC BMC functionalities (SDRR, SEL, etc.) and does not replace a shelf-manager. The system integrator must add software on top of the IPMC to fulfill the requirements of the chassis.	Satellite - the Board is a Satellite Management Controller, under the control of an external central Management Controller.
OS Load Watchdog Timer Action	No Action **Hard Reset** Power Down Power Cycle	The OS Load Watchdog usage requires OS support of this IPMI watchdog.	Allows the IPMC to reset or power down the system if the operating system crashes or hangs.
IPMC Watchdog Time Out	**0** 15 30 45 60 90 120 150 300 600	Selects the Watchdog Time Out delay in seconds.	Amount of time for IPMC to wait before assuming the system has crashed and needs to be reset.
BIOS POST Action	No Action **Hard Reset** Power Down Power Cycle		Select which action to take when the BIOS POST IPMI HW watchdog expires.

5.1.8.1.1 View IPMC System Event Log sub-menu

Feature	Options	Description	Setup Help
Total Number of Entries	“variable”		N/A, display only.
SEL Entry Number	“variable”		Use +/- to traverse the event log.
SEL Record ID	“variable”		N/A, display only.
SEL Record Type	“variable”		N/A, display only.
Event Timestamp	“variable”		N/A, display only.
Generator ID	“variable”		N/A, display only.
Event Message Format Ver	“variable”		N/A, display only.
Event Sensor Type	“variable”		N/A, display only.
Event Sensor Number	“variable”		N/A, display only.
Event Dir Type	“variable”		N/A, display only.
Event Data	“variable”		N/A, display only.

5.1.8.1.1.1Set LAN Configuration sub-menu

Feature	Options	Description	Setup Help
Channel Number		Each interface has a channel number that is used when configuring the channel and for routing messages between channels. The channel number assignments are described in IPMI Specification 1.5, table 6-1.	Enter Channel Number for SET LAN Config Command. Proper value below 16.
Channel Number Status	Valid or Invalid	Display Valid if IPMC support LAN Channel.	N/A, display only.
IP Address	N/A	Press Enter to go to sub screen "IP Address".	Enter for IP Address Configuration.
MAC Address	N/A	Press Enter to go to sub screen "MAC Address".	Enter for MAC Address Configuration.
Subnet Mask	N/A	Press Enter to go to sub screen "Subnet Mask".	Enter for Subnet Mask Configuration.
Gateway Address	N/A	Press Enter to go to sub screen "Gateway Address".	Enter for Gateway IP Address Configuration.
Active LAN Channel Number	**Disabled** 02 03 Both	Each interface has a channel number that is used when configuring the channel and for routing messages between channels. The channel number assignments are described in IPMI Specification 1.5, table 6-1.	Enter Active LAN Channel Number for Set LAN Configuration Command. This refers to IPMI communication channel.
IPMI Communication Channel 2 = Fabric ‘A’ links	N/A		N/A, display only.
IPMI Communication Channel 3 = Fabric ‘B’ links	N/A		N/A, display only.

5.1.8.1.1.1.1IP Address sub-menu

Feature	Options	Description	Setup Help
Channel Number		Each interface has a channel number that is used when configuring the channel and for routing messages between channels. The channel number assignments are described in IPMI Specification 1.5, table 6-1.	Enter Channel Number for SET LAN Config Command. Proper value below 16.
Channel Number Status	**Valid** or Invalid	Display Valid if IPMC support LAN Channel.	N/A, display only.
IP Address	Enter	This allows setting an IP Address for LAN configuration.	Enter for IP Address in decimal in the form of XXX.XXX.XXX.XXX (XXX less than 256 and in decimal only)
Current IP Address	xxx.xxx.xxx.xxx	Display the current LAN configuration stored in IPMI NVRAM for IPMI LAN.	N/A, display only.

5.1.8.1.1.1.2MAC Address sub-menu

Feature	Options	Description	Setup Help
Channel Number		Each interface has a channel number that is used when configuring the channel and for routing messages between channels. The channel number assignments are described in IPMI Specification 1.5, table 6-1.	Enter Channel Number for SET LAN Config Command. Proper value below 16.
Channel Number Status	**Valid** or Invalid	Display Valid if IPMC support LAN Channel.	N/A, display only.
Current MAC Address	xx.xx.xx.xx.xx.xx	Display the current MAC Address stored in IPMI NVRAM for IPMI LAN.	N/A, display only.

5.1.8.1.1.1.3Subnet Mask sub-menu

Feature	Options	Description	Setup Help
Channel Number		Each interface has a channel number that is used when configuring the channel and for routing messages between channels. The channel number assignments are described in IPMI Specification 1.5, table 6-1.	Enter Channel Number for SET LAN Config Command. Proper value below 16.
Channel Number Status	**Valid** or Invalid	Display Valid if IPMC support LAN Channel.	N/A, display only.
Subnet Mask	Enter	This allows setting of a Subnet Mask for LAN configuration.	Enter for Subnet Mask in decimal in the form of XXX.XXX.XXX.XXX (XXX less than 256 and in decimal only)
Current Subnet Mask	xxx.xxx.xxx.xxx	Display the current Subnet Mask configuration stored in IPMI NVRAM for IPMI LAN.	N/A, display only.

5.1.8.1.1.1.4Gateway Address sub-menu

Feature	Options	Description	Setup Help
Channel Number		Each interface has a channel number that is used when configuring the channel and for routing messages between channels. The channel number assignments are described in IPMI Specification 1.5, table 6-1.	Enter Channel Number for SET LAN Config Command. Proper value below 16.
Channel Number Status	**Valid** or Invalid	Display Valid if IPMC support LAN Channel.	N/A, display only.
Gateway Address	Enter	This allows setting an Gateway IP Address for LAN configuration.	Enter for Gateway IP Address in decimal in the form of XXX.XXX.XXX.XXX (XXX less than 256 and in decimal only)
Current Gateway Address	xxx.xxx.xxx.xxx	Display the current Gateway configuration stored in IPMI NVRAM for IPMI LAN.	N/A, display only.

5.1.8.1.1.2IPMI Device and Firmware Information sub-menu

Feature	Options	Description	Setup Help
Product ID	Product ID code (2 bytes)	Displays CPU blade product ID from IPMI "Get Device ID Command", byte 11:12. Least significant byte first.	N/A, display only.
IPMI Version	1.5 or 2.0	Displays IPMI Specification version.	N/A, display only.
Device ID	Varies	Displays IPMI device ID. OEM defined, IPMI Device ID has been assigned like this: Renesas H8S2148 = 1 Kontron PMM = 2 Renesas H8S2145 = 3 Renesas H8S2166 = 4 Renesas H8S2138 = 5 Renesas H8S2168 = 6	N/A, display only.
Device Revision	Varies	Displays IPMI device revision. OEM defined, specify the version of the IPMI Device controller.	N/A, display only.
Firmware Revision	Varies	Displays IPMI firmware version.	N/A, display only.
SDR Revision	Varies	Displays SDR (Sensor Data Record) revision. This field correpond to the implementation specific auxiliary information from IPMI "Get Device ID Command", byte 13. The SDR revision is displayed in decimal notation.	N/A, display only.
Maintenance Revision	Varies	Displays Aux byte 2 but more verbose about the version	N/A, display only.
Slot Address	XX		N/A, display only.

Feature	Options	Description	Setup Help
Aux Revision Info byte 0	Varies	Displays implementation specific auxiliary information from IPMI "Get Device ID Command", byte 13. The byte is displayed as a 2-digit hexadecimal number.	N/A, display only.
Aux Revision Info byte 1	Varies	Displays implementation specific auxiliary information from IPMI "Get Device ID Command", byte 14. The byte is displayed as a 2-digit hexadecimal number.	N/A, display only.
Aux Revision Info byte 2	Varies	Displays implementation specific auxiliary information from IPMI "Get Device ID Command", byte 15. The byte is displayed as a 2-digit hexadecimal number.	N/A, display only.
Aux Revision Info byte 3	Varies	Displays implementation specific auxiliary information from IPMI "Get Device ID Command", byte 16. The byte is displayed as a 2-digit hexadecimal number.	N/A, display only.

5.1.8.1.1.3System Management sub-menu

Feature	Options	Description	Setup Help
Board Product Name	CP6014	Displays the CPU blade product name.	N/A, display only.
Board Serial Number	Varies	Displays the CPU blade serial number.	N/A, display only.
Board Part Number	T6014xxxx	Displays the CPU blade part/model number. The "xxxx" correspond to the Product Part Number Scheme.	N/A, display only.
Product Name	CP6014	Displays the CPU blade product name.	N/A, display only.
Product Part/Model	T6014xxxx	Displays the CPU blade part/model number. The "xxxx" correspond to the Product Part Number Scheme.	N/A, display only.
Product Version Number	Manufacturer PCB version	Displays the CPU blade PCB revision number.	N/A, display only.
Product Serial Number	Varies	Displays the CPU blade serial number.	N/A, display only.

5.1.8.2 Watchdog Configuration sub-menu

Feature	Options	Description	Setup Help
FPGA Watchdog Timer after POST	**Disabled** Enabled		This option enables the FPGA watchdog after the card has done the POST to monitor the OS loading phase. Requires a driver to disable or trig the FPGA Watchdog to prevent reset.
Watchdog Duration	16 Seconds 67 Seconds 268 Seconds		Use this option to set the timeout of the watchdog timing circuitry.

5.1.9 Exit menu

Feature	Options	Description	Setup Help
Save Changes and Exit	Enter	Saves modified settings into non-volatile memory and reboots the system.	Exit system setup after saving the changes. F10 key can be used for this operation.
Discard Changes and Exit	Enter	Discards modifications to settings and reverts to the state when Setup was entered, then complete remaining POST.	Exit system setup without saving any changes. ESC key can be used for this operation.
Discard Changes	Enter	Discards modifications to settings and reverts to the state when Setup was entered.	Discards changes done so far to any of the setup questions. F7 key can be used for this operation.
Load Optimal Defaults	Enter	Loads the factory default settings.	Load Optimal Default values for all the setup questions. F9 key can be used for this operation.
Load Failsafe Defaults	Enter	Loads the factory failsafe settings. These settings could be used when the board is not operating correctly.	Load Failsafe Default values for all the setup questions. F8 key can be used for this operation.
Exit & Update BIOS	Enter		Force BIOS recovery mode on next system reset.

5.2 Boot Utilities

AMI Boot Utilities are: Boot Menu POP-UP

Boot Menu POP-UP is a boot screen that displays a selection of boot devices from which you can boot your operating system.

5.2.1 Pressing <F2>

Pressing < F2 > during POST enters Setup.

5.2.2 Pressing <F11> (or <F3> from a Console Redirection terminal)

Pressing <F11> (or <F3> from a Console Redirection terminal) displays the Boot Menu POP-UP with these options:

1 Load the operating system from a boot device of your choice.

2 Exit the Boot Menu POP-UP (with <ESC>) and load the operating system from the boot devices in the order specified in Setup.

5.2.3 BOOT Menu POP-UP

The BOOT Menu POP-UP expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, CDROM, Flash Disk, SCSI or LAN. You can select your boot device in Setup, or you can choose a different device each time you boot during POST by selecting your boot device in the Boot device <F11> (or <F3> from a Console Redirection terminal).

5.3 Console Redirection (VT100 Mode)

The VT100 operating mode allows remote setup of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

5.3.1 Requirements

The terminal should emulate a VT100 or an ANSI terminal. Terminal emulation programs such as Telix©, HyperTherminal(Windows), minicom(Linux) or ProComm©(Windows) can also be used.

5.3.2 ANSI and VT100 Keystroke Mapping

Table 5-3:ANSI and VT100 Keystroke Mapping

Up	<ESC>[A
Down	<ESC>[B
Right	<ESC>[C
Left	<ESC>[D
Home	<ESC>[H
End	<ESC>[K
F1	<ESC>OP
F2	<ESC>OQ
F3	<ESC>OR
F4	<ESC>OT

5.3.3 VT-UTF8 Keystroke Mapping

The following "escape sequences" are defined in the "Conventions for Keys Not in VT100 Terminal Definition and ASCII Character Set" section of "Standardizing Out-of-Band Management Console Output and Terminal Emulation (VT-UTF8 and VT100+)",available for download at microsoft.com.

Table 5-4:VT-UTF8 Keystroke Mapping

F1 Key	<ESC>1
F2 Key	<ESC>2
F3 Key	<ESC>3
F4 Key	<ESC>4
F5 Key	<ESC>5
F6 Key	<ESC>6
F7 Key	<ESC>7
F8 Key	<ESC>8
F9 Key	<ESC>9
F10 Key	<ESC>0
F11 Key	<ESC>!
F12 Key	<ESC>@
Alt Modifier	<ESC>^A
Control Modifier	<ESC>^C
Home Key	<ESC>h
End Key	<ESC>k
Insert Key	<ESC>+
Delete Key	<ESC>-
Page Up Key	<ESC>?
Page Down Key	<ESC>/

These "escape sequences" are supported by VT-UTF8 compliant terminal connections, such as Windows Server 2003 Emergency Management Services (EMS).

AMIBIOS8 Serial Redirection supports these key sequences under two configurations:

- "Terminal Type" setup question is set to "VT-UTF8"
- "Terminal Type" setup question is set to "VT100" or "ANSI" and "VTUTF8 Combo Key Support" setup question is set to "Enabled"

5.4 Installing Drivers

5.4.1 Linux

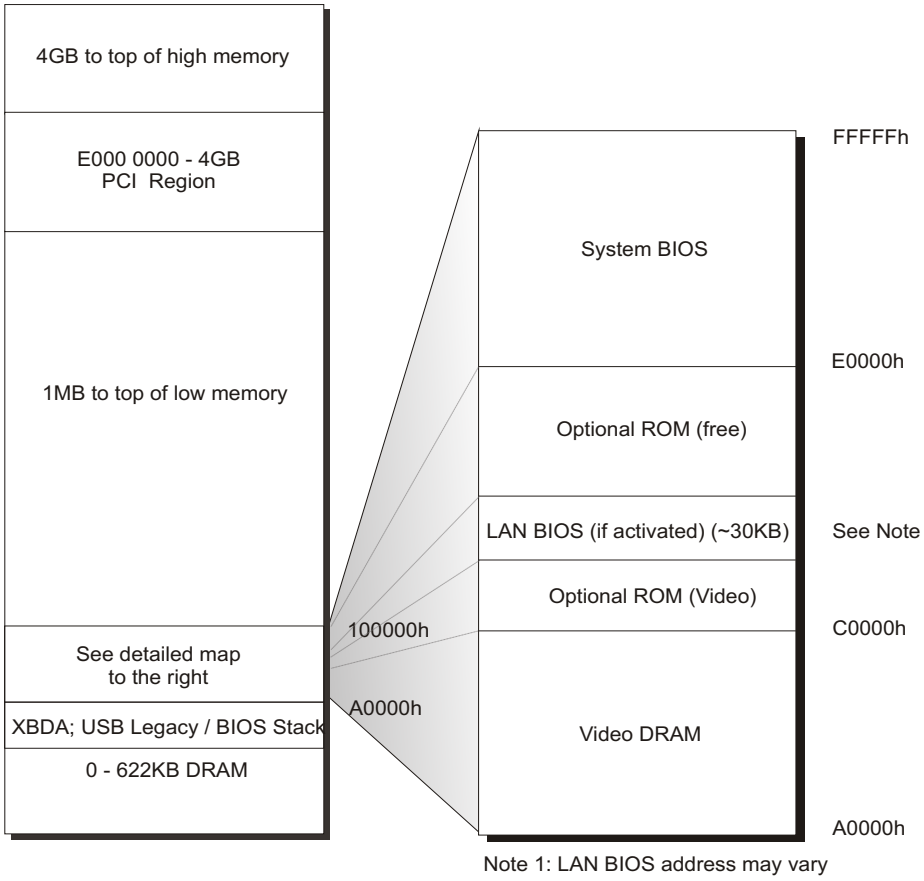
WindRiver PNE Linux 1.5 BSP and RedHat Enterprise Linux 5.1 include all required drivers to fully support all on-board devices.

5.4.2 Windows

Windows 2003 requires to install Chipset, Video and Ethernet drivers. They are available on the CD provided with this board or from our web site at www.kontron.com.

A. Memory & I/O Maps

A.1 Memory Mapping



Address	Function
00000-9B7FF	0-622 KB DRAM
9B800-9FFFF	622KB - 640 KB XBDA; USB Legacy / BIOS Stack
A0000-BFFFF	Video DRAM
C0000-DFFFF	Optional ROM (PMC / XMC / CPCI Slots) LAN BIOS around 30KB if activated, address may vary Optional ROM (video) External BIOS 18KB-64KB , address may vary
E0000-FFFFF	System BIOS
100000-PCI Memory	DRAM available “low”
1 0000 0000 - top of memory	DRAM available “High”

A.2 Kontron I/O Mapping

Address	Optional Address	Function
000-01F		DMA Controller 1
020-03F		Interrupt Controller 1
040-05F		Timer
060-06F		Keyboard
070-07F		Real-time clock
080-09F		DMA Page Register
0A0-0BF		Interrupt Controller 2
0C0-0DF		DMA Controller 2
0F0-0F1, 0F8-0FF		Math Coprocessor
2F8-2FF		UART2 port
378-37A		LPT port for Xilinx JTAG programmer
3F8-3FF		UART1 port
A00-A1F		Kontron FPGA resources
CA2-CA3		KCS interface

A.3 PCI IDSEL and Device Numbers

Bus#	Dev#	Funct.#	V. ID	D. ID	Description	PCI Description
00	00	0	8086	65C0	Intel 5100 DMI	Link to ICH9
00	02	0	8086	65E2	Intel 5100 PCI Express port 2	
00	03	0	8086	65E3	Intel 5100 PCI Express port 3	Bridge -> PMC
00	04	0	8086	65E4	Intel 5100 PCI Express port 4	-> Video
00	05	0	8086	65E5	Intel 5100 PCI Express port 5	-> LAN A & B
00	06	0	8086	65E6	Intel 5100 PCI Express port 6	-> XMC
00	07	0	8086	65E7	Intel 5100 PCI Express port 7	Bridge -> CPCI
00	08	0	8086	65FF	Intel 5100 DMA Engine	
00	10	0	8086	65F0	Intel 5100 Proc bus/INT/sys addr	
00	10	1	8086	65F0	Intel 5100 Mem map/ctrl/err	
00	10	2	8086	65F0	Intel 5100 RAS register	
00	11	0	8086	65F1	Intel 5100 reserved	
00	13	0	8086	65F3	Intel 5100 Miscellaneous	
00	15	0	8086	65F5	Intel 5100 Channel 0 Mem ctrl reg	
00	16	0	8086	65F6	Intel 5100 Channel 1 Mem ctrl reg	
00	19	0	8086	10BD	Intel ICH9 Integrated LAN	LAN front plate
00	1D	0	8086	2934	Intel ICH9 USB UHCI controller 1	
00	1D	1	8086	2935	Intel ICH9 USB UHCI controller 2	
00	1D	7	8086	293A	Intel ICH9 USB EHCI controller 1	
00	1E	0	8086	244E	Intel ICH9 DMI-to-PCI Bridge	Not used
00	1F	0	8086	2916	Intel ICH9 LPC	
00	1F	2	8086	2920	Intel ICH9 SATA or Intel ICH9 SATA RAID	
00	1F	3	8086	2930	Intel ICH9 SMBus	
02	00	0	8086	105E	Intel 82571EB	LAN A
02	00	1	8086	105E	Intel 82571EB	LAN B
04	00	0	1002	94CB	ATI RADEON E2400	Video
05	00	0	12D8	E130	Pericom Bridge (PCI, PCI-X)	-> CPCI slots
06	1F-19	--	--	--	CPCI bus (up to 7 slots)	
07+x	00	0	12D8	E130	Pericom Bridge (PCI, PCI-X)	-> PMC
08+x	16	--	--	--	PMC card	PMC

x = number of PCI bridges present in the CPCI slot cards.

B. Kontron Extension Registers

B.1 FPGA/CPLD Registers Definition

Unused bits are reserved. To insure compatibility with other product and upgrades to this product, do not modify unused bits. Bits marked NU are not used on this board. Writing to such bit does nothing and reading is undefined, either 0 or 1 may be returned.

Legend:

Symbol	Signification
U	Unchanged (stay unchanged after reset)
X	Not Defined (bit not used on this board)
NU	Not Used
NA	Not Applicable
RSV	Reserved

B.1.1 CPU Addressing Space

B.1.1.1 80h/81h: Postcode register

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
80/81h	Read	postcodes							
	Write	postcodes							
	Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
D7	postcode	Postcodes are captured in this register as they are written. Be careful that postcodes are not always 16-bit and the high byte in register 81h could be unrelated to the content of register 80h. Also, the legacy floppy disk controller (if any) MUST BE DISABLED. The LPC bridge in this design does a full decode and cycle acknowledge on I/O 81h and this will conflict with any other resource that decodes this address.
D6		
D5		
D4		
D3		
D2		
D1		
D0		

B.1.1.2 A00h: Customer & FPGA major version

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A00h	Read	Customer			Major version				
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	Customer (2)	Customer identification. 000: generic Kontron board 001: customer #1 (for customer specific registers)
D6	Customer (1)	
D5	Customer (0)	
D4	Maj. Vers. (4)	FPGA major version. For the production test software to verify that the latest code is programmed. See also CPU-04h for minor version.
D3	Maj. Vers. (3)	
D2	Maj. Vers. (2)	
D1	Maj. Vers. (1)	
D0	Maj. Vers. (0)	

B.1.1.3 A01h: Debug LED & Manufacturing flag

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A01h	Read	Mfgflag	NU	NU	NU	NU	NU	NU	NU
	Write	Mfgflag	NU	NU	NU	NU	NU	NU	NU
	Reset	0	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	Mfg flag	A memory element used by the BIOS and test software in manufacturing. Note that this bit is cleared on a power-up but is not affected by a reset.
D6	NU	NA
D5	NU	NA
D4	NU	NA
D3	NU	NA
D2	NU	NA
D1	NU	NA
D0	NU	NA

B.1.1.4 A02h: IPMI firmware upgrade

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A02h	Read	NU	NU	NU	NU	NU	uart	mode	reset
	Write	NU	NU	NU	NU	NU	uart	mode	reset
	Reset	NA	NA	NA	NA	NA	0	1	0/1

Bit	Name	Description
D7	NU	NA
D6	NU	NA
D5	NU	NA
D4	NU	NA
D3	NU	NA
D2	uart	1: Set this bit to connect UART1 to the IPMC for programming. 0: Deassert to disconnect UART1 from the IPMC.
D1	mode	IPMC mode pin. See details below.
D0	reset	0: at power-up, normal boot. 1: at power-up, upgrade boot, when T2604 is present with its factory jumper on or if baseboard factory jumper is on (IPMC in reset). If IPMI override jumper is on, it also boots in upgrade mode. This bit is not affected by any other reset. This is the highest priority reset source.

B.1.1.5 A03h: BIOS to IPMC mailbox

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A03h	Read	MI7	MI6	MI5	MI4	MI3	MI2	MI1	MI0
	Write	MI7	MI6	MI5	MI4	MI3	MI2	MI1	MI0
	Reset*	0	0	0	0	0	0	0	0

* Blade insertion only. No reset after that.

Bit	Name	Description
D7	MI[7:0]	Message from BIOS to IPMC. The state written here is copied to a register in the IPMC address space. Readback by the BIOS is a local readback. The IPMC can clear any of those bits by writing a 1 in the corresponding IPMC register.
D6		
D5		
D4		
D3		
D2		
D1		
D0		

B.1.1.6 A04h: Development features

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A04h	Read	Minor version				Test	IPMIOvr	WDDis	NU
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	Minor version[3]	Minor version that does not impact the IPMC; for tracking only.
D6	Minor version[2]	
D5	Minor version[1]	
D4	Minor version[0]	
D3	Test	1: indicates that the FPGA build is a test version that should never be sent to production.
D2	IPMI Over.	1: IPMI override jumper is in. IPMC is kept in reset.
D1	WD Over.	1: all watchdogs are disabled. Debug mode operation.
D0	NU	NA

B.1.1.7 A06h: FPGA PROM and PCB version

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A06h	Read	PROM	VBATok	mezPCB1	mezPCB0	clrCMOS	PCB2	PCB1	PCB0
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	PROM	Indicates which PROM is currently selected for the FPGA (based on selection jumper). 0: jumper present : factory PROM used 1: jumper absent : user PROM used
D6	VBATok	State of the RTC battery. 0: RTC battery voltage is below 2V. 1: RTC battery voltage is correct (above 2V).
D5	mezPCB1	Mezzanine PCB version (FPGA inputs tied to VCC/GND to indicate version).
D4	mezPCB0	
D3	clrCMOS	Sate of the clear CMOS jumper. 0: jumper absent : normal operation 1: jumper present : BIOS must clear CMOS setup stored in flash.
D2	PCB2	PCB version (FPGA inputs tied to VCC/GND to indicate version).
D1	PCB1	
D0	PCB0	

B.1.1.8 A07h: BOM Version

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A07h	Read	mezBOM1	mezBOM0	NU	NU	NU	BOM2	BOM1	BOM0
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	mezBOM1	Mezzanine BOM options(FPGA input connected to GND/VCC thru a RA/RB resistor).
D6	mezBOM0	
D5	NU	NA
D4	NU	NA
D3	NU	NA
D2	BOM2	BOM option 2 (FPGA input connected to GND/VCC thru a RA/RB resistor).
D1	BOM1	BOM option 1 (FPGA input connected to GND/VCC thru a RA/RB resistor).
D0	BOM0	BOM option 0 (FPGA input connected to GND/VCC thru a RA/RB resistor).

B.1.1.9 A08h: T2604 mezzanine flash, BIOS EEPROM and SPI control

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A08h	Read	EEWP	NU	DLC5EN	SOL	RJ45PR	FWHID	factory mode	HIDE
	Write	EEWP	NU	DLC5EN	URECFG	NU	NU	NU	HIDE
	Reset	1*	NA	0*	0*	NA	NA	NA	0*

*not cleared by a reset; power-up only

Bit	Name	Description
D7	EEWP	CMOS EEPROM Write Protect 0: unprotected 1: write protected An equivalent bit exists in IPMC address space (28h). Both must assert this bit for the EEPROM to be write protected; at least one must de-assert this bit to unprotect the EEPROM.
D6	NU	NA
D5	DLC5EN	Enable the operation of the DLC5 pod. 0: DLC5 POD disabled. When not enabled, the SPI output is 3-state, JTAG outputs are in benign state and parallel port is not functional. This is the power up default. It leaves the possibility to hook an external DLC5 pod directly to the SPI for direct-SPI programming using Xilinx tool. Discretes are required on the board to provide a benign state on the SPI interface. The POD, using this bit, should be enabled prior to use and disabled immediately afterward.

Bit	Name	Description
D4	SOL/URECFG	User re-configures FPGA / SOL activated Read 1: Serial-Over-LAN is activated. Write 1: when '1' is written, an FPGA re-configuration is initiated. It works only if the FPGA FACTORY PROM jumper is absent. When the jumper is present, the operator must extract, remove the jumper and re-insert the board in the chassis (complete power cycle). If the jumper is absent and reconfiguration is initiated, the code following the I/O write instruction is never executed. If the jumper is present, nothing special happens.
D3	RJ45PR	Serial port 0 cable presence. 1: A cable is present either in front plate connector or rear IO serial port 0 connector.
D2	FWHID	Firmware hub identifier. Inidicates the presence of the T2604 BIOS mezzanine at ICH's last reset. 0: BIOS from onboard SPI FLASH 1: BIOS from the T2604 *always '0' when bit HIDE='1'
D1	factorymode	Board usage mode, normal or factory. 0: normal use 1: BIOS must use alternate setup for factory. This bit reflects the presence of the jumper on the T2604.
D0	HIDE	Hide T2604 FLASH. 0: BIOS uses T2604 FLASH if the T2604 is connected. 1: BIOS uses onboard FLASH, even if the T2604 is connected (typically used the first time the onboard FLASH is programmed).

B.1.1.10 A0Ah: Reset History

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A0Ah	Read	NU	CRIP	NU	NU	lastRst			
	Write	NU	CRIP	NU	NU	NU	NU	NU	NU
	Reset	NA	1*	NA	NA	NA	NA	NA	NA

*'1' at power up; otherwise, it depends on the last reset (warm = '0', cold = '1')

Bit	Name	Description
D7	NU	NA
D6	CRIP	Cold Reset In Progress ** this bit can be written only by BIOS ** 0: can initiate warm or cold reset 1: cold reset is in progress; any warm reset request while this bit is set is automatically modified into a cold reset
D5	NU	NA
D4	NU	NA

Bit	Name	Description
D3	lastRst[3] lastRst[2] lastRst[1] lastRst[0]	This value indicates the last reset that happened. In case of multiple back-to-back reset, only the last one is reported. Interpretation is as follows: 0000: Reserved 0001: Power up 0010: Custom watchdog cold 0011: Reserved 0100: Reserved 0101: Reserved 0110: Software initiated cold (ICH's CF9h write) 0111: Reserved 1000: IPMI initiated cold 1001: Reserved 1010: Reset push button cold 1011: Reserved 1100: Reserved 1101: Reserved 1110: DEBUG T2604 hide cold 1111: Reserved
D2		
D1		
D0		

B.1.1.11 A0Bh: FPGA DNA

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A0Bh	Read	NU	NU	NU	NU	data	clk	NU	NU
	Write	NU	NU	NU	NU	mode	clk	NU	NU
	Reset	NA	NA	NA	NA	0	0	NA	NA

Bit	Name	Description
D7	NU	NA
D6	NU	NA
D5	NU	NA
D4	NU	NA
D3	data/mode	Write 0: Shift data from FPGA DNA port 1: load FPGA DNA port shift register with serial number Read Data from FPGA DNA port shift register (see figure)
D2	clk	Clock signal for the FPGA DNA port (see figure)
D1	NU	NA
D0	NU	NA

B.1.1.12 A10h: Custom watchdog control

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A10h	Read	jmpwden	swopen	pmcpr#	xmcpr#	wden	wdtimeo2	wdtimeo1	wdtimeo0
	Write	NU	NU	NU	NU	wden	wdtimeo2	wdtimeo1	wdtimeo0
	Reset	NA	NA	NA	NA	0	1	1	1

Bit	Name	Description
D7	jmpwden	Watchdog disable jumper state. 0: All watchdogs are disabled (for test purposes). 1: All watchdogs are enabled.
D6	swopen	cPCI handle switch open indicator 0: switch closed 1: switch opened
D5	pmcpr#	PMC presence indicator 0: PMC present 1: PMC not present
D4	xmcpr#	XMC presence indicator 0: XMC present 1: XMC not present
D3	wden	Custom watchdog enable 0: disabled 1: enabled Note: This bit can be changed only when WDENLOCK bit (A0D, d6) is not set.
D2 D1 D0	wdtimeo[2:0]	Custom watchdog timeout selection. 000: 0.016s 001: 0.065s 010: 0.262s 011: 1.048s 100: 4.194s 101: 16.78s 110: 67.11s 111: 268.4s

B.1.1.13 A11h: Bridges speed, video output and LED2 source

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A11h	Read	LED2 sel			LED2 Type	CPUsmisn	NU	brgDis	video rear
	Write	LED2 sel			NU	NU	NU	NU	video rear
	Reset	0*	0*	0*	NA	NA	NA	NA	1*

Bit	Name	Description
D7 D6 D5	LED2sel	LED2 source selection. 000: Reserved 100: ICH SATA activity 101:Reserved 11x: reserved
D4	LED2Type	LED2 Type (mirror of IPMI-07 D5) 0: HDD activity, based on bits D7-D5 1 : IPMI override; manual control using IPMI-07 register
D3	CPUsmism	CPUs FSB mismatch 0: If 2 CPUs are used, both use same FSB frequency. Always '0' if only one CPU is installed. 1: If 2 CPUs are used, they use different FSB frequency, so stop boot sequence and advise the user.
D2	NU	NA
D1	brgDis	Baseboard bridge disable (reflects real bridge state) 0: Baseboard bridge is enabled 1: Baseboard bridge is disabled * Baseboard bridge can only be enabled when board is inserted in a system slot of a CPCI backplane, without the "bridge disable jumper". Otherwise, baseboard bridge is disabled.
D0	videorear	Video output switch selection. 0: Video outputs to front panel connector. 1: Video outputs to rear IO connector. (default)

B.1.1.14 A12h: SerIRQ source status and enable

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A12h	Read	NU	wdenlock	swintsts	wdintsts	enumintsts	swinten	wdinten	enuminten
	Write	NU	wdenlock	swintsts	wdintsts	NU	swinten	wdinten	enuminten
	Reset	NA	1	0	0	NA	0	0	0

Bit	Name	Description
D7	NU	NA
D6	wdenlock	Custom watchdog enable lock. 0: Can change wden bit. 1: wden bit is locked; can't change its state.
D5	swintsts	cPCI handle switch event status. Read 0: No state change on cPCI handle or event cleared. 1: cPCI handle switch state changed. Write 0: No effect on bit. 1: Clear event.
D4	wdintsts	Custom watchdog event status. Read 0: No custom watchdog timeout or event cleared. 1: Custom watchdog timeout has occurred. Write 0: No effect on bit. 1: Clear event.
D3	enumintsts	ENUM cPCI signal status. Read 0: cPCI ENUM signal not asserted 1: cPCI ENUM signal asserted. Write No effect on bit. Must clear the ENUM condition in the PCI-PCIe bridge to clear this bit.
D2	swinten	cPCI handle switch interrupt enable. 0: Disable interrupt on switch event (swsts = '1'). 1: Enable interrupt on switch event (swsts = '1').
D1	wdinten	Custom watchdog interrupt enable. 0: Custom watchdog interrupt disabled. 1: Custom watchdog interrupt enabled.
D0	enuminten	cPCI ENUM interrupt enable. 0: Disable interrupt on ENUM assertion. 1: Enable interrupt on ENUM assertion.

B.1.1.15 A13h: Serial IRQ and NMI

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A13h	Read	mezBrgRst	bbBrgRst	SERIRQen	IRQnum	SWNMIen	SWNMI	WDNMIen	WDNMI
	Write	mezBrgRst	bbBrgRst	SERIRQen	IRQnum	SWNMIen	NU	WDNMIen	NU
	Reset	NA	NA	0	0	0	0	0	0

Bit	Name	Description
D7	mezBrgRst	Mezzanine's PCIe-PCI bridge reset read 0: normal operation 1: bridge is kept in reset write 0: no effect 1: BIOS asks for mezzanine's bridge to be resetted * BIOS can set this bit to '1'; FPGA put it back to '0' when reset is over.
D6	bbBrgRst	Baseboard's PCIe-PCI bridge reset read 0: normal operation 1: bridge is kept in reset write 0: no effect 1: BIOS asks for baseboard's bridge to be resetted * BIOS can set this bit to '1'; FPGA put it back to '0' when reset is over.
D5	SERIRQen	Serial IRQ interrupt enable (applies to IRQ5/IRQ7 only) 0: disabled 1: enabled
D4	IRQnum	Serial IRQ interrupt number 0: IRQ5 (default) 1: IRQ7
D3	SWNMIen	cPCI handle switch NMI generation enable 0: disabled 1: enabled
D2	SWNMI	cPCI handle switch NMI request 0: No NMI request. Cleared by disabling SWNMIEN. 1: cPCI handle switch opened, so NMI requested.
D1	WDNMIen	Custom watchdog NMI generation enable 0: disabled 1: enabled
D0	WDNMI	Custom watchdog NMI request 0: No NMI request. Cleared by triggering the watchdog. 1: Custom watchdog timeout, so NMI requested.

IRQ#	Entry point	Usage
3	Serial IRQ	ICH serial port 1
4	Serial IRQ	ICH serial port 0
5	Serial IRQ	FPGA IRQ (see A12h and A13h)
6	Serial IRQ	Available
7	Serial IRQ	FPGA IRQ (see A12h and A13h)
8	ICH	ICH internally generated.
9	Serial IRQ	Available
10	Serial IRQ	Available
11	Serial IRQ	Available
12	Serial IRQ	Available
13	FERR#	ICH hardwired to FERR#
14	Serial IRQ	Available
15	Serial IRQ	Available
16	IOCHCK#	FPGA NMI request (see A13h)
17	PCI INTA#	ICH PIRQA#
18	PCI INTB#	ICH PIRQB#
19	PCI INTC#	ICH PIRQC#
20	PCI INTD#	ICH PIRQD#

B.1.1.16 A14h: SMBus arbitration

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
A14h	Read	CPCI ID4	CPCI ID3	CPCI ID2	CPCI ID1	RSV	smbSPD Gnt	smb mchck Gnt	SMBEEP Gnt
	Write	NU	NU	NU	NU	NU	smbSPD Req	smb mchck Req	SMBEEP Req
	Reset	NA	NA	NA	NA	NA	0	0	0

Bit	Name	Description
D7	CPCI_ID4	CPCI rear module identifier (same as IPMC-31h) [4:3] 00 : TBD 01 : TBD 10 : TBD 11 : Kontron RTM pinout version 1.x
D6	CPCI_ID3	
D5	CPCI_ID2	CPCI RTM type (same as IPMC-31h) 0: RTM is of a valid type (new RTM) 1: RTM is not of a valid type (T1071 or T1072) -- non-early powers are not enabled so this state should never be seen * Valid only when CPCI_ID1 = '0'

Bit	Name	Description
D4	CPCI_ID1	CPCI RTM presence (same as IPMC-31h) 0: RTM is present 1: No RTM is present
D2	smbSPDGnt/Req	SMBus arbitration between the BIOS and the IPMI. This dual purpose bit is mirrored in register IPMC-37h. Read 0: SPD SMBus not granted to BIOS; IPMC has control. 1: SPD SMBus granted to BIOS by the IPMC. Write 0: BIOS doesn't ask for SPD SMBus control. 1: BIOS asks for SPD SMBus control. See Note 1 for operation details.
D1	smbmchckGnt/Req	SMBus arbitration between the BIOS and the IPMI. This dual purpose bit is mirrored in register IPMC-37h. Read 0: MCH/CK505 SMBus not granted to BIOS; IPMC has control. 1: MCH/CK505 SMBus granted to BIOS by the IPMC. Write 0: BIOS doesn't ask for MCH/CK505 SMBus control. 1: BIOS asks for MCH/CK505 SMBus control. See Note 2 for operation details.
D0	smbEEPGnt/Req	"SMBus arbitration between the BIOS and the IPMI. This dual purpose bit is mirrored in register IPMC-37h. Read 0: CMOS EEPROM SMBus not granted to BIOS; IPMC has control. 1: CMOS EEPROM SMBus granted to BIOS by the IPMC. Write 0: BIOS doesn't ask for CMOS EEPROM SMBus control. 1: BIOS asks for CMOS EEPROM SMBus control. See Note 3 for operation details.

Note:1

BIOS should take control of SMBus only when necessary; IPMC has control by default. If the IPMC is in reset, smbSPDGnt = '1' to avoid locking of the SMBus segments.
The BIOS proceeds as follows:
1) Sets bit smbSPDReq in the early boot, prior to using SMBus controller for SPD accesses (dedicated SMBus segment between DIMMs and MCH).
2) Waits for bit smbSPDGnt = '1'.
3) Clears GPIO-30 to physically connect the SMBus controller to the SPD SMBus.
4) Uses the SMBus controller as long as needed.
5) Waits for completion of the current SMBus transaction (on wires).
6) Sets GPIO-30 to release SMBus segment and give it back to the IPMC.
7) Clears smbSPDReq to tell the IPMC that it now has the bus.

The IPMC proceeds as follows:
1) When bit smbSPDReq = '1', waits for completion of any SMBus transaction (on wires).
2) Sets bit smbSPDGnt to tell BIOS that it can now take the SMBus segment.
3) When bit smbSPDReq = '0', clears smbSPDGnt immediately.
SMBus segment is now controlled by the IPMC.

Note:2

BIOS should take control of SMBus only when necessary; IPMC has control by default. If the IPMC is in reset, smbmchckGnt = '1' to avoid locking of the SMBus segment.
The BIOS proceeds as follows:
1) Sets bit smbmchckReq when non early power is available, prior to using SMBus controller for MCH/CK505/DB403/ITP accesses.
2) Waits for bit smbmckckGnt = '1'.
3) Clears GPIO-31 to physically connect the SMBus controller to the MCH/CK505/DB403/ITP SMBus.
4) Uses the SMBus controller as long as needed.
5) Waits for completion of the current SMBus transaction (on wires).
6) Sets GPIO-31 to release SMBus segment and give it back to the IPMC.
7) Clears smbmchckReq to tell the IPMC that it now has the bus.

The IPMC proceeds as follows:
1) When bit smbmchckReq = '1', waits for completion of any SMBus transaction (on wires).
2) Sets bit smbmchckGnt to tell BIOS that it can now take the SMBus segment.
3) When bit smbmchckReq = '0', clears smbmchckGnt immediately.
SMBus segment is now controlled by the IPMC.

Note:3

BIOS should take control of SMBus only when necessary; IPMC has control by default. If the IPMC is in reset, smbEEPGnt = '1' to avoid locking of the SMBus segments.
The BIOS proceeds as follows:
1) Sets bit smbEEPReq in the early boot, prior to using SMBus controller for CMOS EEPROM accesses.
2) Waits for bit smbEPPGnt = '1'.
3) Clears GPIO-29 to physically connect the SMBus controller to the CMOS EEPROM SMBus.
4) Uses the SMBus controller as long as needed.
5) Waits for completion of the current SMBus transaction (on wires).
6) Sets GPIO-29 to release SMBus segment and give it back to the IPMC.
7) Clears smbEEPReq to tell the IPMC that it now has the bus. The IPMC proceeds as follows:
1) When bit smbEEPReq = '1', waits for completion of any SMBus transaction (on wires).
2) Sets bit smbEEPGnt to tell BIOS that it can now take the SMBus segment.
3) When bit smbEEPReq = '0', clears smbEEPGnt immediately.
SMBus segment is now controlled by the IPMC.

B.1.1.17 2F8h: UART2 - Receiver/Transmitter buffers register - BASE+00h, DLAB = '0'

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2F8h	Read	RxData							
	Write	TxData							
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	RxData[7:0] / TxData[7:0]	Write TxData[7:0]: data bits to be transmitted. Bit 0 is the lsb and is transmitted first. Read RxData[7:0]: data bits received. Bit 0 is the lsb and is received first.
D6		
D5		
D4		
D3		
D2		
D1		
D0		

B.1.1.18 2F8h: UART2 - Divisor Lacth (LSB) register - BASE+00h, DLAB = '1'

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2F8h	Read	Divisor value (LSB)							
	Write	Divisor value (LSB)							
	Reset	0	0	0	0	0	0	0	1

Bit	Name	Description
D7	Divisor value[7:0] (LSB)	Baud rate generator divisor value LSB (see table under register 2F9h definition).
D6		
D5		
D4		
D3		
D2		
D1		
D0		

B.1.1.19 2F9h: UART2 - Divisor Latch (MSB) register - BASE+01h, DLAB = '1'

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2F9h	Read	Divisor value (MSB)							
	Write	Divisor value (MSB)							
	Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
D7	Divisor value[7:0] (MSB)	Baud rate generator divisor value MSB (see table below).
D6		
D5		
D4		
D3		
D2		
D1		
D0		

Baud rate	Divisor latch (MSB)(decimal)	Divisor latch (LSB)(decimal)
9600	0	12
19200	0	6
38400	0	3
56000	0	2
115200	0	1

B.1.1.20 2F9h: UART2 - Interrupt Enable register - BASE+01h, DLAB = '0'

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2F9h	Read	0	0	0	0	EDSSI	ELSI	ETBEI	ERBFI
	Write	NU	NU	NU	NU	EDSSI	ELSI	ETBEI	ERBFI
	Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
D7	NU	NA
D6	NU	NA
D5	NU	NA
D4	NU	NA

Bit	Name	Description
D3	EDSSI	Modem status interrupt enable. 0: disabled 1: enabled
D2	ELSI	Receiver line status interrupt enable. 0: disabled 1: enabled
D1	ETBEI	Transmitter holding register empty interrupt enable. 0: disabled 1: enabled
D0	ERBFI	Received data available interrupt enable (timeout in FIFO mode). 0: disabled 1: enabled

B.1.1.21 2FAh: UART2 - Interrupt Identification / FIFO control register - BASE+02h, DLAB = x

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2FAh	Read	mode		0	0	IIR			
	Write	trig		NU	NU	RDYmode	ClrTx	ClrRx	FIFOEN
	Reset	0	0	0	0	0	0	0	1

Bit	Name	Description
D7	mode / trig	Read 00: non-FIFO mode 01: not valid 10: not valid 11: FIFO mode Write Sets trigger level (in bytes) for the RCVR FIFO interrupt (trig[7:6]). 00: 01 01: 04 10: 08 11: 14
D6		
D5	NU	NA
D4	NU	NA
D3	IIR[3] / RDYmode	Read Interrupt identification bit 3; see table below for description. Write 0: no mode change on RXRDY# and TXRDY# pins. 1: change from mode 0 to mode 1 on RXRDY# and TXRDY# pins.

Bit	Name	Description
D2	IIR[2] / ClrTx	Read Interrupt identification bit 2; see table below for description. Write 0: normal operation of TX FIFO. 1: clears TX FIFO and resets its counter logic. The shift register is not cleared.
D1	IIR[1] / ClrRx	Read Interrupt identification bit 1; see table below for description. Write 0: normal operation of Rx FIFO. 1: clears RX FIFO and resets its counter logic. The shift register is not cleared.
D0	IIR[0] / FIFOEn	Read Interrupt identification bit 0; see table below for description. Write 0: 16450 mode (no FIFO) 1: 16550 mode (enables RX and TX FIFOs; FIFOs are resetted on mode change; must set this bit prior to set other FCR bits).

IIR Value (3:0)	Priority level*	Interrupt type	Interrupt source	Interrupt reset control
0001	-	None	None	-
0110	0	Receiver Line Status	Overrun error, parity error, framing error or break interrupt	Reading the Line Status register
0100	1	Received Data Available	Receiver Data Available	Reading the Receiver Buffer register or the FIFO drops below the trigger level
1100	1	Character Timeout Indication	No character has been read from the RCVR FIFO during the last 4 char. times and there is at least 1 char. in it during this time	Reading the Receiver Buffer register
0010	2	Transmitter Holding Register Empty	Transmitter Holding register empty	Reading the IIR or writing into the Transmitter Holding register
0000	3	Modem Status	Clear To Send, Data Set Ready, Ring Indicator or Data Carrier Detect	Reading the Modem Status register

* 0 is the highest priority

B.1.1.22 2FBh: UART2 - Line Control register - BASE+03h, DLAB = x

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2FBh	Read	DLAB	SB	SP	EPS	PEN	STB	WLS	
	Write	DLAB	SB	SP	EPS	PEN	STB	WLS	
	Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
D7	DLAB	Divisor latch access bit. 0: disabled; normal addressing mode. 1: enabled; enables access to divisor latch registers during read or write operation to addresses BASE+0h and BASE +1h.
D6	SB	Set break. 0: disabled 1: set break; SOUT is forced to '0'. This does not have any effects on transmitter logic. The break is disabled by setting the bit to '0'.
D5	SP	Stick parity. 0: disabled 1: enabled
D4	EPS	Even parity select. 0: odd parity 1: even parity * when SP = '1', if EPS = '1' and PEN = '1', parity is always '1'. * when SP = '1', if EPS = '0' and PEN = '1', parity is always '0'.
D3	PEN	Parity enable. 0: disabled 1: enabled; parity is added in transmission and checked in reception.
D2	STB	Number of STOP bits. 0: 1 STOP bit 1: 1½ STOP bit when WLS = ""00"" 2 STOP bits when other cases (WLS /= ""00"")
D1	WLS[1:0]	Word length select (WLS[1:0]). 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits
D0		

B.1.1.23 2FCh: UART2 - Modem Control register - BASE+04h, DLAB = x

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2FCh	Read	NU	NU	NU	Loop	Out2	Out1	RTS	DTR
	Write	NU	NU	NU	Loop	Out2	Out1	RTS	DTR
	Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
D7	NU	NA
D6	NU	NA
D5	NU	NA
D4	Loop	Loop enable. 0: disabled 1: enabled
D3	Out2	Output2 (OUT2n) control. 0: OUT2n = '1' 1: OUT2n = '0'
D2	Out1	Output1 (OUT1n) control. 0: OUT1n = '1' 1: OUT1n = '0'
D1	RTS	Request to send (RTSn) control. 0: RTSn = '1' 1: RTSn = '0'
D0	DTR	Data Terminal Ready (DTRn) control. 0: DTRn = '1' 1: DTRn = '0'

B.1.1.24 2FDh: UART2 - Line Status register - BASE+05h, DLAB = x

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2FDh	Read	FIER	TEMT	THRE	BI	FE	PE	OE	DR
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	0	1	1	0	0	0	0	0

Bit	Name	Description
D7	FIER	FIFO data error. 0: In 16450 mode or CPU read the LSR and no subsequent errors occurred in the FIFO. 1: At least one parity error, framing error or break indication in the FIFO.
D6	TEMT	Transmitter Empty indicator. 0: Either THR or TSR contains a data byte. 1: Transmitter Shift Register and Transmitter Holding registers are empty. / XMIT FIFO and Shift Register are empty.
D5	THRE	Transmitter Holding register empty indicator. 0: Byte written to the Transmitter Holding Register. / At least one byte is written to the XMIT FIFO. 1: The UART is ready to transmit a new data byte. It causes an interrupt to the CPU when bit ETBEI = '1' (Interrupt Enable register, bit 1). Data from the Transmitter Holding Register is transferred into the Transmitter Shift Register (TSR). / XMIT FIFO is empty.
D4	BI	Break interrupt indicator. 0: Normal data byte or Line Status register read. 1: Data byte received is at '0' longer than a full word transmission time (start bit + data bits + parity + stop bits). / Data byte at the top of the FIFO has the error. When it occurs, only one zero character is loaded into the FIFO.
D3	FE	Framing Error indicator. 0: Valid STOP bit or Line Status register read. 1: Data byte received did not have a valid STOP bit. The UART will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this start bit twice, and then starts receiving data again. / Data byte at the top of the FIFO has a framing error.
D2	PE	Parity Error indicator. 0: No parity error or Line Status register read. 1: The Received data byte had a parity error. / Data byte at the top of the FIFO has a parity error.
D1	OE	Overrun Error indicator. 0: No error; line status register read. 1: New byte was received before CPU read; previous data byte lost. / FIFO is full and next character in the shift register has been overwritten by a new character, but not transferred to FIFO.
D0	DR	Data Ready indicator. 0: Data read from the receive buffer or FIFO. 1: Data byte received and stored in the receive buffer or FIFO

B.1.1.25 2FEh: UART2 - Modem Status register - BASE+06h, DLAB = x

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2FEh	Read	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
D7	DCD	Data Carrier Detect. Complement of DCDn. When MCR bit 4 = '1' (loop), this bit is equivalent to OUT2n in the MCR.
D6	RI	Ring Indicator. Complement of RIn. When MCR bit 4 = '1' (loop), this bit is equivalent to OUT1n in the MCR.
D5	DSR	Data Set Ready. Complement of DSR. When MCR bit 4 = '1' (loop), this bit is equivalent to RTSn in the MCR.
D4	CTS	Clear To Send. Complement of CTSn. When MCR bit 4 = '1' (loop), this bit is equivalent to DTR in the MCR.
D3	DDCD	Delta Data Carrier Detect indicator. 0: No change on DCD input. 1: DCD input has changed state. NOTE: whenever bit 0, 1, 2 or 3 is set to '1', a Modem Status Interrupt is generated.
D2	TERI	Trailing Edge of Ring Indicator detector. 0: No rising edge on RI input. 1: RI input has changed from '0' to '1'.
D1	DDSR	Delta Data Set Ready indicator. 0: No change on DSRn input. 1: DSRn input has changed state since the last time it was read.
D0	DCTS	Delta Clear To Send indicator. 0: No change on CTSn input. 1: CTSn has changed state since the last time it was read.

B.1.1.26 2FFh: UART2 - Scratch register - BASE+07h, DLAB = x

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2FFh	Read	SCR							
	Write	SCR							
	Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
D7	SCR[7:0]	Read/Write scratch pad. No effects on UART operation.
D6		
D5		
D4		
D3		
D2		
D1		
D0		

B.1.1.27 378h: LPT Data register

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
378h	Read	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
	Write	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
	Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
D7	LD[7:0]	LPT data write and readback.
D6		
D5		
D4		
D3		
D2		
D1		
D0		

B.1.1.28 379h: LPT Status register

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
379h	Read	BUSY#	ACK#	PE	SLCT1	ERR	IRQ#	NU	NU
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	BUSY#	Printer busy.
D6	ACK#	Printer acknowledge. Always return 1 (no ack).
D5	PE	Paper empty.
D4	SLCT1	Select in.
D3	ERR	Error.
D2	IRQ#	Interrupt status. Always return 1 (no interrupt).
D1	NU	NA
D0	NU	NA

B.1.1.29 37Ah: LPT Control register

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
37Ah	Read	NU	NU	NU	NU	SLCT0#	INIT	ALF#	STRB#
	Write	NU	NU	NU	NU	SLCT0#	INIT	ALF#	STRB#
	Reset	NA	NA	NA	NA	1	1	1	1

Bit	Name	Description
D7	NU	NA
D6	NU	NA
D5	NU	NA
D4	NU	NA
D3	SLCT0#	Printer Select Output.
D2	INIT	Reset printer. 0: reset. 1: normal use.
D1	ALF#	Auto line feed.
D0	STRB#	Strobe.

B.1.2 IPMI Addressing Space

B.1.2.1 00h: Board control

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
00h	Read	FPGArdy	BoardON	TurnX	PwrBtn	NU	NU	UART	BRST
	Write	HTO	NU	NU	PwrBtn*	NU	NU	UART	BRST
	Power up	0	NA	NA	0	NA	NA	0	0

*can only write '1', cleared upon reset sequence completion

Bit	Name	Description
D7	HTO / FPGArdy	Read FPGA ready 1: FPGA is powered and clocked; ready to start power up sequence. Write Hard turn off. 1: Turn off power supplies immediately.
D6	BoardON	Power status of the board. 1: board ON.
D5	TurnX	0: Normal operation. 1: Turn ON or turn OFF in progress.
D4	PwrBtn	ATX-like power button. 1: fake power button press; bit clears upon reset sequence completion. This bit should only be set when TurnX = '0'. See below for power up/down processes.
D3	NU	NA
D2	NU	NA
D1	UART	UART override. 1: IPMC's serial port is routed to the front plate serial port (development tool only). 0: Normal operation.
D0	BRST	Board Reset. 0: No board reset requested. 1: Board reset requested. This bit shall be set for a minimum of 16ms to reset the board. The type of reset (cold/warm) depends on the state of bit warm in IPMC-2Dh.

B.1.2.2 01h: Board status

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
01h	Read	CPU0	CPU1	1.05V	VTT	1.1V	1.2V	1.5V	1.8V
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	CPU0	VCORE for CPU0 is within specifications.
D6	CPU1	VCORE for CPU1 is within specifications.
D5	1.05V	1.05V rail is within specifications.
D4	VTT	VTT rail is within specifications.
D3	1.1V	1.1V rail is within specifications.
D2	1.2V	1.2V rail is within specifications.
D1	1.5V	1.5V rail is within specifications.
D0	1.8V	1.8V rail is within specifications.

B.1.2.3 02h: Post codes (LSB)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
02h	Read	post (LSB)							
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	post(LSB)[7:0]	Last post LSB written by the BIOS.
D6		
D5		
D4		
D3		
D2		
D1		
D0		

B.1.2.4 03h: Post codes (MSB)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
03h	Read	post (MSB)							
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	post(MSB)[15:8]	Last post MSB written by the BIOS.
D6		
D5		
D4		
D3		
D2		
D1		
D0		

B.1.2.5 07h: LEDs control

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
07h	Read	NU	NU	L2TYPE	L1TYPE	L0TYPE	LED2	LED1	LED0
	Write	NU	NU	L2TYPE	L1TYPE	L0TYPE	LED2	LED1	LED0
	Reset	NA	NA	0	0	0	0	0	0

Bit	Name	Description
D7	NU	NA
D6	NU	NA
D5	L2TYPE	LED2 type 0: HDD activity (default) 1: User defined
D4	L1TYPE	LED1 type 0: Healthy green LED (default) 1: User defined
D3	L0TYPE	LED0 type 0: Hotswap blue LED (default) 1: User defined
D2	LED2	HDD activity/User green LED 1: blinks on HDD activity (when L2TYPE = '0')/ user defined usage (when L2TYPE = '1')

Bit	Name	Description
D1	LED1	Healthy green LED 1: light up LED to indicate all powers are healthy (when L1TYPE = '0')/ user defined usage (when L1TYPE = '1')
D0	LED0	Standard hotswap Blue LED 1: light up LED when board is fully hotswapped (when L0TYPE = '0')/ user defined usage (when L0TYPE = '1')

B.1.2.6 09h: Intel 82571EB link and activity

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
09h	Read	linkb 1000#	linkb 100#	linkb#	actb#	linka 1000#	linka 100#	linka#	acta#
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	linkb1000#	1Gbps Link detection on Intel 82571EB LAN port B. 0: 1Gbps link detected. 1: No link or link speed lower than 1Gbps.
D6	linkb100#	100Mbps Link detection on Intel 82571EB LAN port B. 0: 100Mbps link detected. 1: No link or link speed lower than 100Mbps.
D5	linkb#	Link detection on Intel 82571EB LAN port B. 0: Link detected. 1: No link.
D4	actb#	Activity detection on Intel 82571EB LAN port B. 0: Activity detected (blink). 1: No activity.
D3	linka1000#	1Gbps Link detection on Intel 82571EB LAN port A. 0: 1Gbps link detected. 1: No link or link speed lower than 1Gbps.
D2	linka100#	100Mbps Link detection on Intel 82571EB LAN port B. 0: 100Mbps link detected. 1: No link or link speed lower than 100Mbps.
D1	linka#	Link detection on Intel 82571EB LAN port A. 0: Link detected. 1: No link.
D0	acta#	Activity detection on Intel 82571EB LAN port A. 0: Activity detected (blink). 1: No activity.

B.1.2.7 0Ah: Mezzanine misc and XMC status

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0Ah	Read	NU	NU	NU	XMCpr#	XMCrst0#	RSV	VGA tcrit#	mez therm int#
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	NU	NA
D6	NU	NA
D5	NU	NA
D4	XMCpr#	XMC presence. 0: An XMC is connected to the baseboard.
D3	XMCrst0#	XMC reset out. 0: XMC is in reset; IPMI could decide to generate a board reset if required by customer.
D1	VGAtcrit#	VGA controller critical temperature alarm. 0: Critical temperature alarm activated from internal thermal sensor reading. 1: Internal thermal sensor temperature is not critical.
D0	mezthermint#	Mezzanine thermal sensor alarm. 0: One of the readings is out of range; alarm is activated. 1: All readings within specified range.

B.1.2.8 19h/1Bh: CPU0/1 status

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
19h/1Bh	Read	BSEL2	BSEL1	BSEL0	NU	HOT	TTRIP	IERR	PR
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	BSEL2	CPU's BCLK selection signals. Interprete as follows (BSEL[2:0]): 000: 266.666MHz 001: Reserved 010: Reserved 011: Reserved 100: 333.333MHz 101: Reserved 110: Reserved 111: Reserved
D6	BSEL1	
D5	BSEL0	
D4	NU	NA

Bit	Name	Description
D3	HOT	Prochot. 1: CPU has reached its maximum safe operating temperature; TCC is activated.
D2	TTRIP	Thermal trip. 1: Thermal trip has occurred, so VCORE switcher is turned off. 0: normal operation; VCORE switcher can be turned on. This bit retains its value when the board is turned off but it is cleared at power up time. Prior to the first power up, this bit is cleared. The IPMC can restart the CPU using the PWRBTN bit; this automatically clears the bit. Note that bits IERR and HOT are set following a therm trip since the CPU is unpowered. The FPGA performs the following action when a thermal trip occurs: 1) Memorizes the condition. 2) Turns off VCORE, VTT and VCCA on the faulty CPU. 3) Forces a virtual turn off.
D1	IERR	CPU internal error. 1: internal error has occurred (IPMI will take action if needed/wanted)
D0	PR	CPU present. 1: CPU is present (always '1' for CPU0)

B.1.2.9 1Ah: CPU0 & CPU1 MS ID

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
1Ah	Read	NU	NU	NU	CFGERR	MSID1_1	MSID1_0	MSID0_1	MSID0_0
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	NU	NA
D6	NU	NA
D5	NU	NA
D4	CFGERR	Configuration error. 1: mismatch of CPU0 and CPU1 FSB frequency (BSEL[2:0]) (IPMI will take action upon CFGERR assertion to reset/power down the board). 0: both CPUs use the same FSB frequency.
D3	MSID1_1	Market Segment identifier for CPU1 (MSID[1:0]). 00: Wolfdale-DP Processor. 01: Woodcrest Processor. 10: Clovertown Processor. 11: Harpertown Processor.
D2	MSID1_0	

Bit	Name	Description
D1	MSID0_1	Market Segment identifier for CPU0 (MSID[1:0]). 00: Wolfdale-DP Processor. 01: Woodcrest Processor. 10: Clovertown Processor. 11: Harpertown Processor.
D0	MSID0_0	

B.1.2.10 1Ch: Hot swap controllers status

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
1Ch	Read	HSpwrgdmez	HSpwrgd	HSFLTmez	NU	3VOCmez	HSFLT	5VOC	3VOC
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	HSpwrgdmez	Mezzanine hot swap controller power good. 1: power is stable.
D6	HSpwrgd	Baseboard hot swap controller power good. 1: power is stable.
D5	HSFLTmez	Mezzanine hot swap controller fault. 1: fault occurred. Action is taken by the IPMI.
D4	NU	NA
D3	3VOCmez	Mezzanine 3.3V over current. 1: Over current fault on mezzanine's 3.3V rail.
D2	HSFLT	Baseboad hot swap controller fault. 1: fault occurred. Action is taken by the IPMI.
D1	5VOC	Baseboard 5V over current. 1: Over current fault on baseboard's 5V rail.
D0	3VOC	Baseboard 3.3V over current. 1: Over current fault on baseboard's 3.3V rail.

B.1.2.11 Power Fail Source Debug

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
26h	Read	NU	NU	NU	NU	NU	NU	NU	NU
	Write	CPU0	CPU1	1.05V	VTT	1.1V	1.2V	1.5V	1.8V
	Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
D7	CPU0	1: Remove CPU0 power enable to generate a fault.
D6	CPU1	1: Remove CPU1 power enable to generate a fault.
D5	1.05V	1: Remove 1.05V power enable to generate a fault.
D4	VTT	1: Remove VTT power enable to generate a fault.
D3	1.1V	1: Remove 1.1V power enable to generate a fault.
D2	1.2V	1: Remove 1.2V power enable to generate a fault.
D1	1.5V	1: Remove 1.5V power enable to generate a fault.
D0	1.8V	1: Remove 1.8V power enable to generate a fault.

B.1.2.12 27h: Power fail source

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
27h	Read	CPU0	CPU1	1.05V	VTT	1.1V	1.2V	1.5V	1.8V
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
D7	CPU0	0: VCore for CPU0 failed and caused last reset.
D6	CPU1	0: VCore for CPU1 failed and caused last reset.
D5	1.05V	0: 1.05V failed and caused last reset.
D4	VTT	0: VTT failed and caused last reset.
D3	1.1V	0: 1.1V failed and caused last reset.
D2	1.2V	0: 1.2V failed and caused last reset.
D1	1.5V	0: 1.5V failed and caused last reset.
D0	1.8V	0: 1.8V failed and caused last reset.

B.1.2.13 28h: BIOS EEPROM write protect

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
28h	Read	EEWP	factory Mode	0	0	0	FWH ID	0	0
	Write	EEWP	NU	NU	NU	NU	NU	NU	NU
	Reset	1	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	EEWP	BIOS Setup EEPROM Write Protect. 0: EEPROM is not write protected (even if BIOS bit is set to WP). 1: EEPROM is write protected (default state). Both, BIOS (CPU-08h) and IPMI must set this bit for the EEPROM to be write protected.
D6	factoryMode	Board usage mode, normal or factory. 0: normal use 1: BIOS must use alternate setup for factory. This bit reflects the presence of the jumper on the T2604. Same bit as in CPU-08h register.
D5	NU	NA
D4	NU	NA
D3	NU	NA
D2	FWHID	Firmware hub identifier. Inidicates the presence of the T2604 BIOS mezzanine at ICH's last reset. 0: BIOS from onboard SPI FLASH 1: BIOS from the T2604 *always '0' when bit HIDE='1' Same bit as in CPU-08h register.
D1	NU	NA
D0	NU	NA

B.1.2.14 29h: Reset events

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
29h	Read	0	PwrGd	PFRev	0	Rstev	RIP	PBev	PB
	Write	NU	NU	Clr	NU	Clr	NU	Clr	NU
	Reset	NA	x	1	NA	x	0	x	0

Bit	Name	Description
D7	NU	NA
D6	PwrGd	ICH power good. 0: ICH power is not granted. 1: ICH has power (ICH_PGOOD = '1').
D5	PFRev	Power Fail Reset event. 0: No power fail or IPMI has written '1' into this bit. 1: Power fail occurred. This bit is used to capture a short pulse on the power source. Since power supplies are not valid during a normal power up, this bit will always be set following a normal power up. It is not possible to clear this bit when the power supplies are not stable. Make sure PwrGd is active before clearing this bit.
D4	NU	NA
D3	Rstev	Reset event. 0: No reset occurred or IPMI has written a '1' into this bit. 1: A cold or warm reset occurred.
D2	RIP	Reset In Progress. 0: No reset in progress. 1: A cold or warm reset is in progress. This bit returns automatically to '0' at the end of the reset sequence and Rstev will turn to '1' (if not already '1') at this time.
D1	PBev	Push button reset event. 0: No reset occurred or IPMI has written a '1' into this bit. 1: Reset push button has been pressed.
D0	PB	Push button reset state. 0: Push button currently released. 1: Push button currently pressed.

B.1.2.15 2Dh: Misc

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2Dh	Read	SSC	SOL	NU	SW_O	RS232pr	NU	NU	videorear
	Write	SSC	SOL	NU	NU	NU	NU	NU	NU
	Reset	1	0	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	SSC	Spread Spectrum Clocking enable. 0: No spread spectrum on PCIe clocks. 1: Spread spectrum is activated on all PCIe clocks (default state).
D6	SOL	Serial-Over-Lan enable. 0: No SOL operation. 1: SOL is activated. See serial port mux table for details.
D5	NU	NA
D4	SW_O	cPCI handle switch open indicator 0: switch closed 1: switch opened
D3	RS232pr	RS232 cable detect. 0: No RS232 cable connected into COM1 connector. SOL can be activated (default). 1: RS232 cable connected into COM1 connector (either front plate or Rear IO connector).
D2	NU	NA
D1	NU	NA
D0	videorear	Video output selection. 0: Video output to front panel. 1: Video output to rear IO.

B.1.2.16 2Fh: BOM straps

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2Fh	Read	mezBOM1	mezBOM0	NU	NU	NU	BOM2	BOM1	BOM0
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	mezBOM1	Mezzanine BOM option 1.... TBD!
D6	mezBOM0	Mezzanine BOM option 0.... TBD!
D5	NU	NA
D4	NU	NA
D3	NU	NA
D2	BOM2	BOM option 2.... TBD! (same as CPU-07h)
D1	BOM1	BOM option 1.... TBD! (same as CPU-07h)
D0	BOM0	BOM option 0.... TBD! (same as CPU-07h)

B.1.2.17 30h: cPCI status and control 0

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
30h	Read	cpci pr#	NU	NU	NU	fully seated#	sysen#	bdsel mez#	bdsel#
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	cpcipr#	cPCI backplane presence. 0: Board inserted in a cPCI backplane. 1: Board inserted in a cTCA backplane.
D6	NU	NU
D5	NU	NU
D4	NU	NU
D3	fullyseated#	Fully seated (input signal from cPCI J1-J2 early signals). 0: Early powers and signals stable.
D2	sysen#	System enable (input signal from cPCI J1-J2). 0: Board inserted in system slot; acts as master on cPCI. 1: Board inserted in peripheral slot; acts as ""drone"" (disconnected from cPCI backplane).

Bit	Name	Description
D1	bdselmez#	Board select on mezzanine (input signal from cPCI J1-J2 mez). 0: Always '0' in system slot when board hot swapped; board select in peripheral slots.
D0	bdsel#	Board select on baseboard (input signal from cPCI J1-J2). 0: Always '0' in system slot when board hot swapped; board select in peripheral slots.

B.1.2.18 31h: cPCI related

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
31h	Read	RSV	mez pr#	healthy bp#	cPCI ID[4]	cPCI ID[3]	cPCI ID[2]	cPCI ID[1]	cPCI ID[0]
	Write	RSV	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D6	mezpr#	Mezzanine presence. 0: A mezzanine is present.
D5	healthybp#	Healthy backplane. (copy of output signal)
D4	cPCIID[4:0]	Rear IO Identifier (input signal from cPCI J3). [0] = '0' (hardwired) TBD...
D3		
D2		
D1		
D0		

B.1.2.19 35h: IPMC to BIOS mailbox

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
35h	Read	MI7	MI6	MI5	MI4	MI3	MI2	MI1	MI0
	Write	MI7 CLR	MI6 CLR	MI5 CLR	MI4 CLR	MI3 CLR	MI2 CLR	MI1 CLR	MI0 CLR
	Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
D7	MI7 / MI7CLR	Message from BIOS to IPMC. The state written here is copied from CPU-03h register. The IPMC can clear a given bit by writing a '1' in it. Writing a '0' has no effect. Those are software defined bits. This register is used to send simple messages to the IPMC prior to DRAM initialization. See CPU-03h register description for details.
D6	MI6 / MI6CLR	
D5	MI5 / MI5CLR	
D4	MI4 / MI4CLR	
D3	MI3 / MI3CLR	
D2	MI2 / MI2CLR	
D1	MI1 / MI1CLR	
D0	MI0 / MI0CLR	

B.1.2.20 36h: Reset History

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
36h	Read	WDEN	NU	NU	NU	lastRst			
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	WDEN	Watchdog disable jumper state. 0: All watchdogs are disabled (for test purposes). 1: All watchdogs are enabled.
D6	NU	NA
D5	NU	NA
D4	NU	NA

Bit	Name	Description
D3	lastRst[3]	This value indicates the last reset that happened. In case of multiple back-to-back reset, only the last one is reported. Interpretation is as follows: 0000: Reserved 0001: Power up 0010: Custom watchdog cold 0011: Reserved 0100: Reserved 0101: Reserved 0110: Software initiated cold (ICH's CF9h write) 0111: Reserved 1000: IPMI initiated cold 1001: Reserved 1010: Reset push button cold 1011: Reserved 1100: Reserved 1101: CPU Debugger cold 1110: Reserved 1111: Reserved
D2	lastRst[2]	
D1	lastRst[1]	
D0	lastRst[0]	

B.1.2.21 37h: SMBus arbitration

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
37h	Read	NU	NU	NU	NU	NU	smb SPD Req	smb mchck Req	smb EEP Req
	Write	NU	NU	NU	NU	NU	smb SPD Gnt	smb mchck Gnt	smb EEP Gnt
	Reset	NA	NA	NA	NA	NA	1*	1*	1*

*smbxyzGnt = '1' when IPMC is in reset (external reset source)

Bit	Name	Description
D7	NU	NA
D6	NU	NA
D5	NU	NA
D4	NU	NA
D3	NU	NA
D2	smbSPDGnt/Req	SMBus arbitration between the BIOS and the IPMI. This dual purpose bit is a mirror of register CPU-14h. Read 0: SPD SMBus not requested by BIOS; IPMC has control. 1: SPD SMBus requested by BIOS. Write 0: IPMC doesn't grant SPD SMBus control to BIOS. 1: IPMC grants SPD SMBus control to BIOS or is in reset.
D1	smbmchckGnt/Req	"SMBus arbitration between the BIOS and the IPMI. This dual purpose bit is a mirror of register CPU-14h. Read 0: MCH/CK505 SMBus not requested by BIOS; IPMC has control. 1: MCH/CK505 SMBus requested by BIOS. Write 0: IPMC doesn't grant MCH/CK505 SMBus control to BIOS. 1: IPMC grants MCH/CK505 SMBus control to BIOS or is in reset.
D0	smbEEPGnt/Req	SMBus arbitration between the BIOS and the IPMI. This dual purpose bit is a mirror of register CPU-14h. Read 0: CMOS EEPROM SMBus not requested by BIOS; IPMC has control. 1: CMOS EEPROM SMBus requested by BIOS. Write 0: IPMC doesn't grant CMOS EEPROM SMBus control to BIOS. 1: IPMC grants CMOS EEPROM SMBus control to BIOS or is in reset.

Note:
When IPMC is in reset, those bits are automatically set to avoid locking of SMBus segments (mostly for factory use). When the IPMC leaves reset state, it MUST UPDATE the value of smbxyzGnt with corresponding smbxyzReq before using the corresponding SMBus segment.

B.1.2.22 50h: FML0 - Control register (devices 0 & 1)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
50h	Read	IntEn	Wake FML	NU	Clr	rxSts AlEn	rxSts En	Start Rd FIFO	Start Wr FIFO
	Write	IntEn	Wake FML	NU	Clr	rxSts AlEn	rxSts En	Start Rd FIFO	Start Wr FIFO
	Reset	0	0	NA	0	0	0	0	0

Bit	Name	Description
D7	IntEn	Interrupt enable. 1: Enable interrupts on packet reception and on transmit errors. Note: Both interrupts are reported by the same interrupt signal to the IPMC. Interrupt line is held active until the RxFIFO is empty (for RX interrupt) or until the transmission is done without error using retries (for TX interrupt).
D6	WakeFML	Wake FML. 1: Send a start/stop condition on FML master data line to wake slave FML interface (when interface is not responding). This bit self clears when the start/stop condition is done.
D5	NU	NA
D4	Clr	Clear FIFOs. 1: Clear TX and RX FIFOs. 0: Normal FIFOs operation. This bit self clears when the FIFOs are cleared. It can take a certain time; clear occurs when no FML transaction is in progress.
D3	rxStsAlEn	RX status alone enable. 1: enable reception of “periodic” LAN status (periodic packet sent by the i82571EB without request from the FPGA); status information is stored in RX FIFO. 0: disable reception of “periodic” LAN status; information is dropped by the FPGA so IPMC is not aware of this reception.
D2	rxStsEn	RX status enable. 1: enable reception of LAN status received following a data packet; status information is added to data packet into the RX FIFO. 0: disable reception of LAN status received following a data packet; information is dropped by the FPGA so RX FIFO contains only data.
D1	StartRdFIFO	Start read RX FIFO. 1: Start reading RX FIFO request. If RxFIFOEmpty bit is set, no transfer is possible. This bit is self cleared when RX FIFO reading is in progress.
D0	StartWrFIFO	Start write TX FIFO. 1: Start writing data into the TX FIFO; keep this bit high until all data is written into FIFO. Note: If no transaction is in progress on the FML link and the tx FIFO contains at least one packet, the FML host (FPGA) will immediately generate a start condition, send the slave address specified in the address register, and start the transfer. If TxFIFOEmpty flag or the InProg flag is set, no transfer is possible.

B.1.2.23 51h: FML1 - Status register (devices 0 & 1)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
51h	Read	wait for RxD	TxErr	Tx FIFO Alm Full	TxFIFO Full	TxFIFO Emp	RxFIFO Full	Rx FIFO Emp	In Prog
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
D7	waitForRxD	Wait for Rx Data. 1: rxFIFO data is available 0: rxFIFO data is not available
D6	TxErr	Transmit error. 1: NACK received during TX FIFO transfer (TX interrupt status bit). 0: no error detected during TX FIFO transfer. Note: on TxErr, the FPGA retries to send the byte in error. Retries are interleaved with reception transactions if data is available on the FML link. NOT IMPLEMENTED YET.
D5	TxFIFOAlmFull	Transmit FIFO almost full. 1: FIFO space left for a maximum of two packets (2*240bytes) 0: FIFO space left for more than two packets
D4	TxFIFOFull	Transmit FIFO full. 1: TX FIFO is full. TX Data received from BAD interface is dropped.
D3	TxFIFOEmp	Transmit FIFO empty. 1: TX FIFO is empty.
D2	RxFIFOFull	Receive FIFO full. 1: RX FIFO is full. Data received on FML bus is dropped.
D1	RxFIFOEmp	Receive FIFO empty. 1: RX FIFO is empty (RX interrupt status bit).
D0	InProg	Transfer in progress. 1: Data transfer in progress on FML interface.

B.1.2.24 52h: FML2 - Data port FIFOs (devices 0 & 1)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
52h	Read	Rx FIFO							
	Write	Tx FIFO							
	Reset	0	0	0	0	0	0	0	0

Bit	Name	Description
D7	RxFIFO[7:0] / Tx FIFO[7:0]	Read Next data byte available to read from Rx FIFO (from slave). Write Next data byte to write into TX FIFO (to slave).
D6		
D5		
D4		
D3		
D2		
D1		
D0		

B.1.2.25 53h: FML3 - Slave address (for reception, devices 0 & 1)

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
53h	Read	slvAdd							rd/wr#
	Write	slvAdd							rd/wr#
	Reset	0	0	0	0	0	0	0	1

Bit	Name	Description
D7	slvAdd[7:0]	Read / Write Slave address for read requests to device 0; device 1 address is slvAdd with bit D2 inverted.
D6		
D5		
D4		
D3		
D2		
D1		
D0		

B.1.2.26 FPGA DNA

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
FCh	Read	DNA byte							
	Write	NU	NU	NU	NU	NU	DNAsel2	DNAsel1	DNAsel0
	Reset	NA	NA	NA	NA	NA		0	0

Bit	Name	Description
D7	DNA byte[7]	Read only bit [7] of the selected DNA byte
D6	DNA byte[6]	Read only bit [6] of the selected DNA byte
D5	DNA byte[5]	Read only bit [5] of the selected DNA byte
D4	DNA byte[4]	Read only bit [4] of the selected DNA byte
D3	DNA byte[3]	Read only bit [3] of the selected DNA byte
D2	DNAsel2/ DNA byte[2]	Write bit [2] for DNA byte selection Read bit [2] of the selected DNA byte
D1	DNAsel1/ DNA byte[1]	Write bit [1] for DNA byte selection Read bit [1] of the selected DNA byte
D0	DNAsel0/ DNA byte[0]	Write bit [0] for DNA byte selection Read bit [0] of the selected DNA byte

B.1.2.27 FDh: Baseboard and mezzanine PCB revision

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
FDh	Read	NU	NU	NU	mez PCB1	mez PCB0	PCB2	PCB1	PCB0
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	NU	NA
D6	NU	NA
D5	NU	NA
D4	mezPCB[1:0]	Mezzanine PCB revision. Hardwired on PCB.
D3		
D2	PCB[2:0]	Baseboard PCB revision. Hardwired on PCB.
D1		
D0		

B.1.2.28 FEh: FPGA minor/test version

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
FEh	Read	NU	NU	NU	test	minor 3	minor 2	minor 1	minor 0
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	NU	NA
D6	NU	NA
D5	NU	NA
D4	test	Test version. 0: Version available for release. 1: Version not to be released to clients; for TEST ONLY.
D3	minor[3:0]	FPGA minor version. This is for reporting only. The IPMC must not do anything with this. FPGA modifications that affect the software have a new major version number. The minor version is for hardware only modification tracking.
D2		
D1		
D0		

B.1.2.29 FFh: Customer identification and FPGA major version

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
FFh	Read	cust 2	cust 1	cust 0	major 4	major 3	major 2	major 1	major 0
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	NA	NA	NA	NA	NA	NA	NA	NA

Bit	Name	Description
D7	cust[2:0]	Customer identification. 000: generic Kontron board. Others: reserved for customer specific configurations.
D6		
D5		
D4	major[4:0]	Programmable FPGA version.
D3		
D2		
D1		
D0		

C. Connector Pinouts

C.1 Connectors Summary

C.1.1 Baseboard

Connector	Description
J1-J3 & J5	CompactPCI
J12	Serial Port COM1 (Faceplate)
J13	USB (Faceplate)
J14	VGA Video (Faceplate)
J15	Ethernet LAN1 (Faceplate)

C.1.2 Mezzanine

Connector	Description
J1	CompactPCI
J11-J13	64-bit PCIX Mezzanine
J15	XMC

C.2 Serial Port COM1 (J12)

Signal	Pin		Pin	Signal
DCD#	1		6	DSR#
RXD	2		7	RTS#
TXD	3		8	CTS#
DTR#	4		9	RI#
GND	5			

C.3 VGA Video(J14)

Signal	Pin		Pin	Signal
RED	1		9	N.C.
GREEN	2		10	GND
BLUE	3		11	N.C.
N.C.	4		12	SDATA
GND	5		13	HSYNC
GND	6		14	VSYNC
GND	7		15	SCLK
GND	8			

C.4 Ethernet(J15)

Signal	Pin		Pin	Signal
DA+	1		5	DC-
DA-	2		6	DB-
DB+	3		7	DD+
DC+	4		8	DD-

C.5 USB Port (J13)

Signal	Pin
VCC	1
DATA-	2
DATA+	3
GND	4

C.6 CPCI Bus (J1)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E
1	5V	-12V	RSV	+12V	5V
2	RSV	5V	RSV	RSV	RSV
3	INTA#	INTB#	INTC#	5V	INTD#
4	IPMB_PWR	HEALTHY#	VI/O	INTP	INTS
5	RSV	RSV	PCI_RST#	GND	GNT0#
6	REQ0#	PCI_PRESENT#	3V3	CLK0	AD31
7	AD30	AD29	AD28	GND	AD27
8	AD26	GND	VI/O	AD25	AD24
9	C/BE3#	IDSEL (N.C.)	AD23	GND	AD22
10	AD21	GND	3V3	AD20	AD19
11	AD18	AD17	AD16	GND	C/BE2#
12	KEY AREA				
13					
14					
15	3V3	FRAME#	IRDY#	BD_SEL#	TRDY#
16	DEVSEL#	PCIXCAP	VI/O	STOP#	LOCK#
17	3V3	IPMB_SCL	IPMB0_SDA	GND	PERR#
18	SERR#	GND	3V3	PAR	C/BE1#
19	3V3	AD15	AD14	GND	AD13
20	AD12	GND	VI/O	AD11	AD10
21	3V3	AD9	AD8	M66EN	C/BE0#
22	AD7	GND	3V3	AD6	AD5
23	3V3	AD4	AD3	5V	AD2
24	AD1	VCCE	VI/O	AD0	ACK64#
25	5V	REQ64#	ENUM#	3V3	5V

Active Low

Long pins : 3D, 4C,5D, 6C, 7D, 9D, 10D, 17D, 19D, 22C, 23D, 24C

Short pins : 9B, 15D

C.7 CPCI Bus (J2)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E
1	CLK1	GND	REQ1#	GNT1#	REQ2#
2	CLK2	S_CLK3	SYSEN#	GNT2#	REQ3#
3	CLK4	GND	GNT3#	REQ4#	GNT4#
4	V I/O	RSV	C/BE7#	GND	C/BE6#
5	C/BE5#	64_EN#	V I/O	C/BE4#	PAR64
6	AD63	AD62	AD61	GND	AD60
7	AD59	GND	V I/O	AD58	AD57
8	AD56	AD55	AD54	GND	AD53
9	AD52	GND	V I/O	AD51	AD50
10	AD49	AD48	AD47	GND	AD46
11	AD45	GND	V I/O	AD44	AD43
12	AD42	AD41	AD40	GND	AD39
13	AD38	GND	V I/O	AD37	AD36
14	AD35	AD34	AD33	GND	AD32
15	RSV	GND	FAL#	REQ5#	GNT5#
16	RSV	RSV	DEG#	GND	RSV
17	RSV	GND	PRST#	REQ6#	GNT6#
18	RSV	RSV	RSV	GND	RSV
19	GND	GND	SMB_SDA	SMB_SCL	SMB_ALERT#
20	CLK5	GND	RSV	GND	RSV
21	CLK6	GND	ST2	ST1	ST0
22	GA4	GA3	GA2	GA1	GA0

Active Low

C.8 CPCI I/O (J3)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E
1	SP0:RTS	SP0:RXD	SP0:DSR	SP0:DCD	ID1
2	SP0:RI	SP0:DTR	SP0:CTS	SP0:TXD	RSV
3	SP1:RTS	SP1:RXD	SP1:DSR	SP1:DCD	RSV
4	SP1:RI	SP1:DTR	SP1:CTS	SP1:TXD	RSV
5	VGA:BLUE	VGA:HSYNC	VGA:VSYNC	VGA:SCL	RSV
6	VGA:RED	VGA:GREEN	VGA:SDA	POST:CLK	POST:DATA
7	3V3	ID2	ID3	ID4	RSV
8	USB0:DATA-	USB0:DATA+	RSV	RSV	RSV
9	USB1:DATA-	USB1:DATA+	GND	RSV	RSV
10	USB1:VCC	USB0:VCC	GND	RSV	RSV
11	RSV	RSV	GND	RSV	RSV
12	RSV	RSV	GND	RSV	RSV
13	LPA:ACT#	LPB:ACT#	N.C.	RSV	RSV
14	LPA:LINK#	LPB:LINK#	LPAB:CT	RSV	RSV
15	LPB:DB+	LPB:DB-	GND	LAN1:DD+	LAN1:DD-
16	LPB:DA+	LPB:DA-	GND	LAN1:DC+	LAN1:DC-
17	LPA:DB+	LPA:DB-	GND	LAN2:DD+	LAN2:DD-
18	LPA:DA+	LPA:DA-	GND	LAN2:DC+	LAN2:DC-
19	5V	5V	3V3	+12V	-12V

Active Low

C.9 CPCI I/O (J5)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E
1	GND	GND	GND	GND	GND
2	HT0:TX+	HT0:TX-	GND	HT0:RX+	HT0:RX-
3	GND	GND	GND	GND	GND
4	RSV	RSV	GND	RSV	RSV
5	GND	GND	GND	GND	GND
6	HT2_TX+	HT2_TX-	GND	HT2_RX+	HT2_RX-
7	GND	GND	GND	GND	GND
8	RSV	RSV	GND	RSV	RSV
9	GND	GND	GND	GND	GND
10	RSV	RSV	GND	SMB:SDA	SMB:SCL
11	RSV	RSV	GND	RSV	RSV
12	RSV	RSV	GND	RSV	RSV
13	RSV	RSV	GND	RSV	RSV
14	RSV	RSV	GND	RSV	RSV
15	RSV	RSV	GND	RSV	RSV
16	RSV	RSV	GND	RSV	RSV
17	RSV	RSV	GND	RSV	RSV
18	RSV	RSV	GND	RSV	RSV
19	RSV	RSV	GND	RSV	RSV
20	RSV	RSV	GND	RSV	RSV
21	RSV	RSV	GND	RSV	RSV
22	RSV	RSV	GND	RSV	RSV

Active Low

C.10 Mezzanine CPCI Power Connector (J1)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E
1	5V	-12V	RSV	+12V	5V
2	RSV	5V	RSV	RSV	RSV
3	RSV	RSV	RSV	5V	RSV
4	RSV	HEALTHY#	VI/O	RSV	RSV
5	RSV	RSV	RSV	GND	RSV
6	RSV	RSV	3V3	RSV	RSV
7	RSV	RSV	RSV	GND	RSV
8	RSV	GND	VI/O	RSV	RSV
9	RSV	RSV	RSV	GND	RSV
10	RSV	GND	3V3	RSV	RSV
11	RSV	RSV	RSV	GND	RSV
12	KEY AREA				
13					
14					
15	3V3	RSV	RSV	BD_SEL#	RSV
16	RSV	GND	VI/O	RSV	RSV
17	3V3	RSV	RSV	GND	RSV
18	RSV	GND	3V3	RSV	RSV
19	3V3	RSV	RSV	GND	RSV
20	RSV	GND	VI/O	RSV	RSV
21	3V3	RSV	RSV	RSV	RSV
22	RSV	GND	3V3	RSV	RSV
23	3V3	RSV	RSV	5V	RSV
24	RSV	5V	VI/O	RSV	RSV
25	5V	RSV	RSV	3V3	5V

Active Low

Long pins : 3D, 4C,5D, 6C, 7D, 9D, 10D, 17D, 19D, 22C, 23D, 24C

Short pins : 9B, 15D

C.11 PMC (J11)

Signal	Pin		Pin	Signal
TCK	1		2	-12V
GND	3		4	INTA#
INTB#	5		6	INTC#
BUSMODE1#	7		8	5V
INTD#	9		10	PMC-RSV
GND	11		12	PMC-RSV
CLK	13		14	GND
GND	15		16	GNT#
REQ#	17		18	5V
VIO	19		20	AD31
AD28	21		22	AD27
AD25	23		24	GND
GND	25		26	C/BE#3
AD22	27		28	AD21
AD19	29		30	5V
VIO	31		32	AD17
FRAME#	33		34	GND
GND	35		36	IRDY#
DEVSEL#	37		38	5V
PCIXCAP	39		40	LOCK#
PMC-RSV	41		42	PMC-RSV
PAR	43		44	GND
VIO	45		46	AD15
AD12	47		48	AD11
AD9	49		50	5V
GND	51		52	C/BE0#
AD6	53		54	AD5
AD4	55		56	GND
VIO	57		58	AD3
AD2	59		60	AD1
AD0	61		62	5V
GND	63		64	REQ64#

Active Low Signal

C.12 PMC (J12)

Signal	Pin		Pin	Signal
+12V	1		2	TRST#
TMS	3		4	TDO
TDI	5		6	GND
GND	7		8	PCI-RSV
PMC-RSV	9		10	PCI-RSV
BUSMODE2#	11		12	3V3
RST#	13		14	BUSMODE3#
3V3	15		16	BUSMODE4#
PME#	17		18	GND
AD30	19		20	AD29
GND	21		22	AD26
AD24	23		24	3V3
IDSEL	25		26	AD23
3V3	27		28	AD20
AD18	29		30	GND
AD16	31		32	C/BE2#
GND	33		34	PMC-RSV
TRDY#	35		36	3V3
GND	37		38	STOP#
PERR#	39		40	GND
3V3	41		42	SERR#
C/BE1#	43		44	GND
AD14	45		46	AD13
M66EN	47		48	AD10
AD8	49		50	3V3
AD7	51		52	PMC-RSV
3V3	53		54	PMC-RSV
PMC-RSV	55		56	GND
PMC-RSV	57		58	PMC-RSV
GND	59		60	PMC-RSV
ACK64#	61		62	3V3
GND	63		64	PMC-RSV

Active Low Signal

C.13 PMC (J13)

Signal	Pin		Pin	Signal
PMC-RSV	1		2	GND
GND	3		4	C/BE7#
C/BE6#	5		6	C/BE5#
C/BE4#	7		8	GND
VIO	9		10	PAR64
AD63	11		12	AD62
AD61	13		14	GND
GND	15		16	AD60
AD59	17		18	AD58
AD57	19		20	GND
VIO	21		22	AD56
AD55	23		24	AD54
AD53	25		26	GND
GND	27		28	AD52
AD51	29		30	AD50
AD49	31		32	GND
GND	33		34	AD48
AD47	35		36	AD46
AD45	37		38	GND
VIO	39		40	AD44
AD43	41		42	AD42
AD41	43		44	GND
GND	45		46	AD40
AD39	47		48	AD38
AD37	49		50	GND
GND	51		52	AD36
AD35	53		54	AD34
AD33	55		56	GND
VIO	57		58	AD32
PMC-RSV	59		60	PMC-RSV
PMC-RSV	61		62	GND
GND	63		64	PMC-RSV

Active Low Signal

C.14 XMC (J15)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	PER0_0_P	PER0_0_N	3V3	PER0_1_P	PER0_1_N	5V
2	GND	GND	TRST#	GND	GND	MRST1#
3	PER0_2_P	PER0_2_N	3V3	PER0_3_P	PER0_3_N	5V
4	GND	GND	TCK	GND	GND	MRTS0#
5	N.C.	N.C.	3V3	N.C.	N.C.	5V
6	GND	GND	TMS	GND	GND	12V
7	N.C.	N.C.	3V3	N.C.	N.C.	5V
8	GND	GND	TDI	GND	GND	12V
9	N.C.	N.C.	N.C.	N.C.	N.C.	5V
10	GND	GND	TDO	GND	GND	GA0
11	PET0_0_P	PET0_0_N	MBIST#	PET0_1_P	PET0_1_N	5V
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PET0_2_P	PET0_2_N	3V3_AUX	PET0_3_P	PET0_3_N	5V
14	GND	GND	GA2	GND	GND	MSDA
15	N.C.	N.C.	N.C.	N.C.	N.C.	5V
16	GND	GND	MVMRO	GND	GND	MSCL
17	N.C.	N.C.	GND	N.C.	N.C.	N.C.
18	GND	GND	N.C.	GND	GND	N.C.
19	REFCLK0+	REFCLK0-	N.C.	WAKE#	ROOT0#	N.C.

Active Low Signal

D. BIOS Setup Error Codes

D.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS:

Checkpoint	Description
Before D1	Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waiking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable CACHE before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See Bootblock Recovery Code Checkpoints section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See POST Code Checkpoints section of document for more information.

D.2 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O (if present). Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from media.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

D.3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
24	Uncompress and initialize any platform specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
39	Initializes DMAC-1 & DMAC-2.

Checkpoint	Description
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, ... etc.) successfully installed in the system and update the BDA, EBDA...etc.
50	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7A	Initializes remaining option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A8	Prepare CPU for OS boot including final MTRR values.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitializes the ADM module.
AB	Prepare BBS for Int 19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Passes control to OS Loader (typically INT19h).
61-70	OEM POST Error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.
DD-DE	OEM PCI init debug POST code during DIMM init, See DIM Code Checkpoints section of document for more information.

D.4 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system busses. The following table describes the main checkpoints where the DIM module is accessed:

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 CONFIGURES all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.
DD-DE	OEM PCI init debug POST code during DIMM init. DEh during BUS number assignment and DDh during ressource allocation, Hight byte is the BUS number.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.

1 = func#1, static devices initialization on the BUS concerned.

2 = func#2, output device initialization on the BUS concerned.

3 = func#3, input device initialization on the BUS concerned.

4 = func#4, IPL device initialization on the BUS concerned.

5 = func#5, general device initialization on the BUS concerned.

6 = func#6, error reporting for the BUS concerned.

7 = func#7, add-on ROM initialization for all BUSes.

8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).

1 = On-board System devices.

2 = ISA devices.

3 = EISA devices.

4 = ISA PnP devices.

5 = PCI devices.

D.5 Memory Initialization ERROR Code

Checkpoint	Description
E0h	Memory Error - Expander type.
E1h	Memory Error - No memory installed.
E2h	Memory Error - Invalid Ratio
E3h	Memory Error - Protocol Error
E4h	Memory Error - SMB Command Error
E5h	Memory Error - Memory population order.
E6h	Memory Error - Chipset Reset
E7h	Memory Error - CL Cycles Not Supported
E8h	Memory Error - DDR Initialisation
E9h	Memory Error - Skew Calibration
EAh	Memory Error - DDR Calibration
EBh	Memory Error - Memory Test
ECh	Memory Error - Clock SMB Command
EEh	Memory Error - Calibration Not Restored

D.6 Memory Reference Code

Checkpoint	Description
A0h	Status - Chipset Initialisation
A1h	Status - Reset State
A2h	Status - Detect DDR Module
A3h	Status - DDR Clock Initialisation
A4h	Status - Reset DDR Controller
A5h	Status - Check DIMM popolation for host compatibility
A6h	Status - Check DIMM popolation for matched ramks
A7h	Status - Determine common DRAM timing parameters
A8h	Status - Execute DRAM Initialisation sequence
A9h	Status - Initialize DRAM configuration and timings
AAh	Status - Calibrate Skewing registers
AFh	Status - Calibrate DRAM Interface
B0h	Status - Execute Membist scrub DRAM
B1h	Status - Qualify enabled ranks
B2h	Status - Initialize SCNB memory configuration
B3h	Status - Initialize SCNB memory mapping
B4h	Status - Initialize global open loop throttling
B5h	Status - Enable SCNB periodic auto-refresh control
B6h	Status - Indicate that MRC is complete

E. Software Update

E.1 IPMC Firmware Update Procedure

It is important to use compatible BIOS, IPMC, FPGA and U-BOOT (switch) versions. Since all these software and hardware solution are exchanging information, they must be in synch. Please always follow Kontron documentation for all your upgrade.

The current version of the IPMC firmware can be retrieved from the BIOS Setup IPMI Menu or using IPMITOOL, through HPM.1 functionalities.

The upgrade of the firmware is also done using HPM.1 functionalities of IPMITOOL. The upgrade can be done through any IPMI interface and is designed to be without payload impact.

The IPMC Firmware update procedure is detailed in a ReadMe file included with the IPMC Firmware package.

E.2 Updating CP6014 BIOS

The AMI Linux upgrade utility is used to upgrade the BIOS.

Please note that you'll have to reboot in order to take advantage of the new BIOS.

It is important to use compatible BIOS, IPMC and FPGA versions. Since all these software and hardware solution are exchanging information, they must be in synch. Please always follow Kontron documentation for all your upgrade.

The recommended upgrade sequence must be: FPGA, IPMC, BIOS.

To read the actual version of FPGA and IPMC use the IPMITOOL tool. The BIOS version is written at every boot during BIOS POST, you can also get it by entering BIOS Setup Menu. The BIOS Setup does also provide the IPMC firmware version, via the IPMI Menu.

Type the following:

afulnx2 /i<BIOS_BIN_File_Name> /pbnc <enter>

(no space between /i and the filename)

/pbnc is for

b - Program Boot Block

n - Program NVRAM

c - Destroy System CMOS

After the upgrade process is completed, reboot by typing

Ctrl-alt-del keys

During BIOS POST, enter BIOS Setup Menu by typing

Del key

In BIOS Setup Menu, make sure to select BIOS Optimal Default Settings by typing F9 key

E.3 BIOS Recovery Procedure

BIOS recovery procedure with a USB stick:

1 Format a USB stick in FAT16.

2 Copy the BIOS file "AMIBOOT.ROM" on your USB stick.

3 Install the CLEAR_CMOS jumper (JP1 pin 1-2) on the CP6014. Refer to the Quick Reference sheet for the jumper location.

4 Insert the USB stick into any USB connector.

5 Start the system.

6 Wait approximately three minutes and the system will restart automatically and be up to run again (ensure to let enough time to recovery).

Note:
During the recovery process, there will be no video. But if you are connected on the console redirection, messages will appear.

For the latest BIOS version, consult www.kontron.com

F. Getting Help

If, at any time, you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, contact our Technical Support at:

North America	EMEA
Tel.: (450) 437-5682	Tel.: +49 (0) 8341 803 333
Fax: (450) 437-8053	Fax: +49 (0) 8341 803 339

If you have any questions about Kontron, our products, or services, visit our Web site at: www.kontron.com

You also can contact us by E-mail at:

North America: support@ca.kontron.com

EMEA: support-kom@kontron.com

Or at the following address:

North America	EMEA
Kontron Canada, Inc.	Kontron Modular Computers GmbH
4555, Ambroise-Lafortune	Sudetenstrasse 7
Boisbriand, Québec	87600 Kaufbeuren
J7H 0A4 Canada	Germany

F.1 Returning Defective Merchandise

Before returning any merchandise please do one of the following:

- Call

    1 Call our Technical Support department in North America at (450) 437-5682 and in EMEA at +49 (0) 8341 803 333. Make sure you have the following on hand: our Invoice #, your Purchase Order #, and the Serial Number of the defective unit.

    2 Provide the serial number found on the back of the unit and explain the nature of your problem to a service technician.

    3 The technician will instruct you on the return procedure if the problem cannot be solved over the telephone.

    4 Make sure you receive an RMA # from our Technical Support before returning any merchandise.

- E-mail

    1 Send us an e-mail at: RMA@ca.kontron.com in North America and at: orderprocessing@kontron-modular.com in EMEA. In the e-mail, you must include your name, your company name, your address, your city, your postal/zip code, your phone number, and your e-mail. You must also include the serial number of the defective product and a description of the problem.

F.2 When Returning a Unit

- In the box, you must include the name and telephone number of a contact person, in case further explanations are required. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.
- Ensure that the unit is properly packed. Pack it in a rigid cardboard box.
- Clearly write or mark the RMA number on the outside of the package you are returning.
- Ship prepaid. We take care of insuring incoming units.

North America	EMEA
Kontron Canada, Inc.	Kontron Modular Computers GmbH
4555, Ambroise-Lafortune	Sudetenstrasse 7
Boisbriand, Québec	87600 Kaufbeuren
J7H 0A4 Canada	Germany

G. Glossary

Acronyms	Descriptions
6U	CompactPCI board size (3U = 100 mm by 160 mm, 6U = 233.35 mm by 160 mm). Refers to height.
8HP	Horizontal Pitch (1 HP = .2 inches, a CompactPCI board is 4HP, Dual width CompactPCI board is 8HP). Refers to width.
ACPI	Advanced Configuration & Power Interface
AER	Advanced Error Reporting. PCI Express device capability for more robust error reporting and is implemented with a specific PCI Express capability structure. See the PCI Express Base Specification.
ANSI	American National Standards Institute
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
ARMD	ATAPI Removable Media Device
ASCII	American Standard Code for Information Interchange. ASCII codes represent text in computers, communications equipment, and other devices that work with text.
ATA	Advanced Technology Attachment
ATAPI	Advanced Technology Attachment Packet Interface
BBS	BIOS Boot Specification
BDA	BIOS Data Area
BEV	Bootstrap Entry Vector
BIOS	Basic Input/Output System
BMC	Base Management Controller
BOM	Bill Of Material
BT	Block Transfer. An optional IPMI system management interface.
CB	Certification Body
CFM	Cubic Foot per Minute
CMOS	Complementary Metal Oxide Semiconductor. Also refers to the small amount of battery (or capacitor) powered CMOS memory to hold the date, time, and system setup parameters.
CPCI	Compact PCI
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit. This sometimes refers to a whole blade, not just a processor component.
CPUID	CPU IDentification. Code that uniquely identify a processor type.
CTCA	Compact Telecom Computing Architecture
CTS	Clear To Send
DC	Direct Current
DDR2	(Same as DDR-II). DDR2 SDRAM or Double-Data-Rate two (2) Synchronous Dynamic Random Access Memory.
DDR-II	(Same as DDR2). DDR2 SDRAM or Double-Data-Rate two (2) Synchronous Dynamic Random Access Memory.
DIMM	Dual In-line Memory Module
DMA	Direct Memory Access
DMI	Desktop Management Interface
DRAM	Dynamic Random Access Memory
DTC	Data Transfer Controller

Acronyms	Descriptions
DTR	Data Terminal Ready
DVD	Digital Video Disk
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface. Specification for Universal Serial Bus specification, revision 2.0.
EISA	Extended Industry Standard Architecture. Superset of ISA, 32-bit bus architecture.
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FAT	File Allocation Table. Usually followed by a number, ex.: FAT32, which defines the number of bits used to address clusters on a disk.
FCC	Federal Communications Commission
FIFO	First In First Out
FML	Fast Management Link
FPGA	Field-Programmable Gate Array
FRU	Field Replaceable Unit. Any entity that can be replaced by a user in the field. Not all FRUs are hot swappable.
FSB	Front Side Bus
FTP	File Transfer Protocol
FW	FirmWare
FWH	FirmWare Hub. Boot flash connected to the LPC bus containing BIOS FW.
Gb	Gigabit
GB	(Same as GByte) GigaByte.
GByte	(Same as GB) GigaByte.
GbE	Gigabit Ethernet
GHz	GigaHertz
GND	GrouND
HDD	Hard Disc Drive
HPM	PICMG Hardware Platform Management specification family
HPM.1	Hardware Platform Management IPM Controller Firmware Upgrade Specification
HW	HardWare
I2C	Inter Integrated Circuit bus
IC	Integrated Circuit
ICH	I/O Controller Hub
ID	IDentification
IDE	Integrated Drive Electronics
IEC	International Electrotechnical Commission
IMCH	Integrated Memory Controller Hub
IEEE	Institute of Electrical and Electronics Engineers
IERR	Internal ERRor. A signal from the Intel Architecture processors indicating an internal error condition.
INT	INTerrupt
IO	(Same as I/O). Input Output

Acronyms	Descriptions
IOH	I/O Hub
IOL	IPMI-Over-LAN
IP	Internet Protocol
IPM	Intelligent Platform Management
IPMB	Intelligent Platform Management Bus
IPMB-0	Intelligent Platform Management Bus Channel 0, the logical aggregation of IPMB-A and IPMB-B.
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
IRQ	Interrupt ReQuest
JTAG	Joint Test Action Group
KB	KiloByte
KHz	KiloHertz
LAN	Local Area Network
LED	Light-Emitting Diode
MAC	Media Access Controller address of a computer networking device.
MB	MegaByte
MCH	Memory Controller Hub
MHz	MegaHertz
Microcode	Intel-supplied data block used to correct specific errata in the processor.
MMC	Module Management Controller. MMCs are linked to the IPMC.
MP	MultiProcessor
MPS	MultiProcessor Specification
MTBF	Mean Time Between Failures
NC	Not Connected
NEBS	Network Equipment-Building System
NMI	Non-Maskable Interrupt
NVRAM	Non-Volatile Random Access Memory
OEM	Original Equipment Manufacturer
OS	Operating System
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCI-32	Peripheral Component Interconnect 32 bits
PCI®	Peripheral Component Interconnect
PCIe	(Same as PCI-E). PCI-Express. Next generation I/O standard
PCI-E	(Same as PCIe). PCI-Express. Next generation I/O standard.
PCI-X	PCI + minor changes to the protocol and faster data rate.
PICMG	PCI Industrial Computer Manufacturers Group
PICMG®	PCI Industrial Computer Manufacturers Group
PMC	PCI Mezzanine Card
PNE	Platform for Network Equipment. A Carrier Grade Linux (4.0) platform.
POST	Power-On Self-Test
PROM	Programmable Read-Only Memory

Acronyms	Descriptions
PXE	Preboot eXecution Environment
RAID	Redundant Array of Independent Disks / Redundant Array of Inexpensive Disks.
RAM	Random Access Memory
RHEL	Red Hat Enterprise Linux
RoHS	Restriction of the Use of Certain Hazardous Substances
ROM	Read Only Memory. Also refers to option ROM or expansion ROM code used during POST to provide services for specific controllers, such as boot capabilities.
RS-232	(Same as RS232). Recommended Standard 232.
RS232	(Same as RS-232). Recommended Standard 232.
RTC	Real Time Clock
RTM	Rear Transition Module
RTS	Request To Send
S.M.A.R.T.	Self-Monitoring, Analysis, and Reporting Technology for IDE.
SAS	Serial Attached SCSI
SATA	Serial ATA
SBC	Single Board Computer
SCSI	Small Computer System Interface
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic Random Access Memory
SEL	System Event Log
ShMC	Shelf Management Controller
SIMM	Single In-line Memory Module
SMART	Self-Monitoring, Analysis, and Reporting Technology, or S.M.A.R.T. A monitoring system for computer hard disks to detect and report on various indicators of reliability, in the hope of anticipating failures.
SMBUS	(Same as SMB/SMBus). System Management Bus.
SMBus	(Same as SMB/SMBUS). System Management Bus.
SMS	System Management Software
SMTP	Simple Mail Transfer Protocol
SNMP	Simple Network Management Protocol
SNTP	Simple Network Time Protocol
SOL	Serial Over LAN
SSE2	Streaming SIMD Extension 2. SIMD is "Single Instruction, Multiple Data".
SSE3	Streaming SIMD Extension 3. SIMD is "Single Instruction, Multiple Data".
SSH	Secure SHell. A network protocol that allows data to be exchanged over a secure channel between two computers.
TX	Transmit
TXD	Transmit
UA	Upgrade Agent
UART	Universal Asynchronous Receiver Transmitter
UL	Underwriters Laboratories inc
USB	Universal Serial Bus
VCC	Power supply

Acronyms	Descriptions
VCORE	Processor CORE power supply
VGA	Video Graphics Array
VLAN	Virtual Local Area Network
VTT	Power supply
WD	WatchDog
XMC	Switched Mezzanine Card