Errata 1

Manual: 28545

Manual Index: 01

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1. Reference: Page 2 - 27, Chapter 2.3.10.1, Table 2-22

The referenced information (table) is superceded by the following table.

Table 2-22: Rear I/O CompactPCI Bus Connector J2 Pinout

PIN	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	TDN1	RDN1	RDP1	GND
20	GND	CLK5	GND	TDP1	GND	VCC	GND
19	GND	GND	GND	FANSENSE2	RES	+3.3V	GND
18	GND	KDAT	UV2-	UV4+	RTC Bat	+3.3V	GND
17	GND	KCLK	ROUT (GND)	PRST#	REQ6#	GNT6#	GND
16	GND	PMDAT	UV2+	DEG#	GND	UV4-	GND
15	GND	PMCLK	GOUT (GND)	FAL#	REQ5#	GNT5#	GND
14	GND	2RIN	2DSR	2RTS	VSYNC (GND)	2CTS	GND
13	GND	2RXD	FANSENSE1 (GND)	BOUT (VIO)	2DTR	2DCD	GND
12	GND	1DSR	1RTS	1CTS	HSYNC (GND)	2TXD	GND
11	GND	1DTR	BOUT (GND)	IDE_PD[9]	1DCD	1RIN	GND
10	GND	IDE_PD[8]	IDE_RST#	1TXD	IDE_PD[10]	1RXD	GND
9	GND	IDE_PD[6]	IDE_PD[7]	IDE_PD[4]	IDE_PD[5]	IDE_PD[11]	GND
8	GND	IDE_PD[3]	IDE_PD[12]	IDE_PD[2]	IDE_PDIAG#/ CBLID#	IDE_PD[1]	GND
7	GND	IDE_PD[14]	IDE_PD[0]	IDE_PD[15]	IDE_PDRQ#	IDE_PIOW#	GND
6	GND	IDE_PIOR	IDE_PIORDY	IDE_PDACK#	IDE_PD [13]	IDE_PIRQ14	GND
5	GND	IDE_PA[1]	IDE_PDASP#	IDE_PA[0]	IDE_PA[2]	TH_GP/ SLP_S3	GND
4	GND	VIO	VCC	IDE_PCS0#	GND	IDE_PCS1#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

The following singals have been changed:

- B5: from GND to **IDE_PDASP#**
- D8: from GND to **IDE_PDIAG#/CBLID#**
- C4: from IDE_PCS1# to IDE_PCS0#
- E4: from IDE_PCS3# to IDE_PCS1#

2. Reference: Page 4 - 10, Chapter 4.5.5, Table 4-10

The referenced information (table) is superceded by the following table.

Table 4-10: I/O Status Register

REGISTER NAME		I/O Status Register						ACCESS	
ADDRESS		0x286						R	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		WST	Res.	Res.	Res.	CSLOT	CENUM	CFAIL	CDER
DEFAULT		1	0	0	0	0	1	1	1
BIT	NAME	VAL	DESCRIPTION						
0	CDER	0	Indicates power derating (CPCI DEG signal)						
		1	Power normal						
1	CFAIL	0	Indicates a power supply failure (CPCI FAIL signal)						
		1	Power normal						
2	CENUM	0	Indicates the insertion or removal of a hot swap system board (CPCI ENUM)						
		1	No hot swap event						
3	CSLOT	0	Indicates that the board is installed in a system slot						
		1	Indicates that the board is installed in a peripheral slot						
4		0	Reserved						
5		0	Reserved						
6		0	Reserved						
7	WST	0	Indicates that a Watchdog timeout has occurred						
		1	Indicates that no Watchdog timeout has occurred						

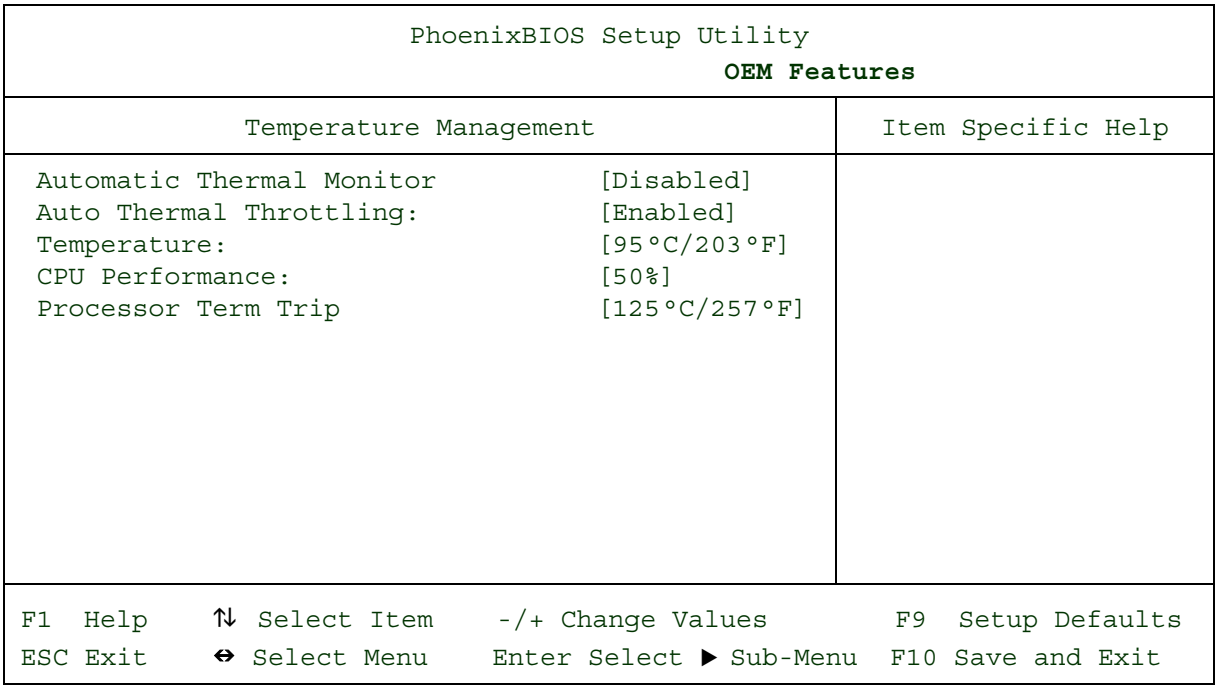
The following default settings have been changed:

- Bit position 0: from 0 to **1**
- Bit position 1: from 0 to **1**
- Bit position 2: from 0 to **1**

3. Reference: Page 5 - 29, Chapter 5.6.3, Figure 5-17

The referenced information (figure) is superceded by the following figure.

Figure 5-17: Temperature Management - Screen Display



4. Reference: Page 5 - 29, Chapter 5.6.3, Table 5-17

The referenced information (table) is superceded by the following table.

Table 5-17: Temperature Management Options

FEATURE	OPTIONS	DESCRIPTION
Automatic Thermal Monitor	Disabled Enabled	Thermal Monitor is enabled and when the die temperature is very near to the temperature limits of the processor, the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor.
Auto Thermal Throttling	Enabled Disabled	Reduces CPU speed to avoid overheating.
Temperature	95°C – 110°C	CPU clock throttling starts when select Temperature is reached.
CPU Performance	12.5% 25% 50% 75%	The CPU performance will be reduced to the selected value when reaching the temperature threshold.
Processor Term Trip	N/A	Shows the maximum processor temperature.

5. Reference: Page 6 - 4, Chapter 6.4, Text

The referenced information (text) is revised as follows.

The text:

The required behavior is described in the ATX (http://www.formfactors.org/FFDetail.asp?FFID=1&CatID=2) and the CompactPCI (PICMG, http://www.picmgeu.org/) specification.

is changed to read:

For information on the required behavior refer to the power supply specifications on the formfactors.org web site and to the CompactPCI (PICMG) specification on the picmgeu.org web site.

6. Reference: Page 7 - 3, Chapter 7.1.1, Text

The referenced information (text) is revised as follows.

The text:

3. Thermtrip:

   In the event of a catastrophic cooling failure, the processor will automatically shut down when the die temperature has reached approximately ~135 °C, this event is called Thermtrip.

is changed to read:

3. Thermtrip:

   In the event of a catastrophic cooling failure, the processor will automatically shut down when the die temperature has reached approximately ~125 °C, this event is called Thermtrip.

7. Reference: Page 7 - 4, Chapter 7.1.1.2, Text

The referenced information (text) is revised as follows.

The text:

The thermal control circuit does not automatically go inactive once the temperature goes below the selected thermal trip point. Explicit software action is necessary to switch back to normal mode.

is changed to read:

The thermal control circuit automatically goes inactive once the temperature goes approximately 5 °C below the selected thermal trip point.

8. Reference: Page 7 - 4, Chapter 7.1.1.3, Text

The referenced information (text) is revised as follows.

The text:

Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C.

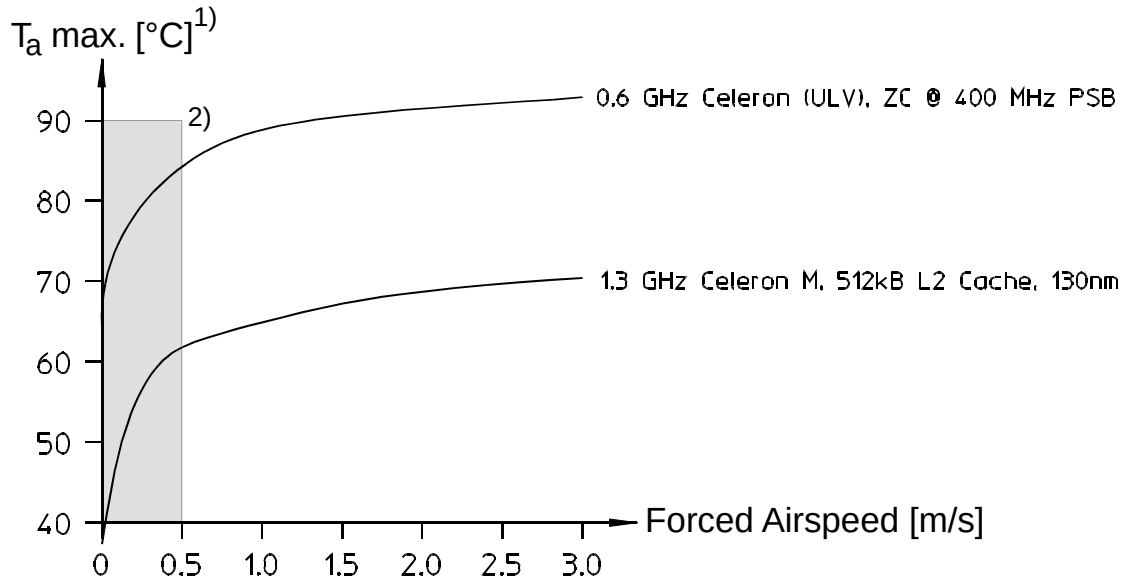
is changed to read:

Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 125°C.

9. Reference: Page 7 - 6, Chapter 7.1.2.2, Figure 7-1

The referenced information (figure) is superceded by the following figure.

Figure 7-1: Mobile Celeron M Temperature Vs. Airspeed Graph



10. Reference: Page B - 13, Chapter B.4.8, Table B-8

The referenced information (table) is superceded by the following table.

Table B-8: Rear I/O CompactPCI Bus Connector CON1 Pinout

PIN	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	TDN1	RDN1	RDP1	GND
20	GND	CLK5	GND	TDP1	GND	VCC	GND
19	GND	GND	GND	RES	RES	+3.3V	GND
18	GND	KDAT	UV2-	UV4+	RTC Bat	+3.3V	GND
17	GND	KCLK	ROUT (GND)	PRST#	REQ6#	GNT6#	GND
16	GND	PMDAT	UV2+	DEG#	GND	UV4-	GND
15	GND	PMCLK	GOUT (GND)	FAL#	REQ5#	GNT5#	GND
14	GND	2RIN	2DSR	2RTS	VSYNC (GND)	2CTS	GND
13	GND	2RXD	FANSENSE1 (GND)	BOUT (VIO)	2DTR	2DCD	GND
12	GND	1DSR	1RTS	1CTS	HSYNC (GND)	2TXD	GND
11	GND	1DTR	BOUT (GND)	IDE_PD[9]	1DCD	1RIN	GND
10	GND	IDE_PD[8]	IDE_RST#	1TXD	IDE_PD[10]	1RXD	GND
9	GND	IDE_PD[6]	IDE_PD[7]	IDE_PD[4]	IDE_PD[5]	IDE_PD[11]	GND
8	GND	IDE_PD[3]	IDE_PD[12]	IDE_PD[2]	IDE_PDIAG#/ CBLID#	IDE_PD[1]	GND
7	GND	IDE_PD[14]	IDE_PD[0]	IDE_PD[15]	IDE_PDRQ#	IDE_PIOW#	GND
6	GND	IDE_PIOR	IDE_PIORDY	IDE_PDACK#	IDE_PD [13]	IDE_PIRQ14	GND
5	GND	IDE_PA[1]	IDE_PDASP#	IDE_PA[0]	IDE_PA[2]	TH_GP/SLP_S3	GND
4	GND	VIO	VCC	IDE_PCS0#	GND	IDE_PCS1#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

The following singals have been changed:

- B5: from GND to **IDE_PDASP#**
- D8: from GND to **IDE_PDIAG#/CBLID#**
- C4: from IDE_PCS1# to IDE_PCS0#
- E4: from IDE_PCS3# to IDE_PCS1#