» User Guide «

CP6004-RA / CP6004-RC

Rugged 6U CompactPCI Processor Board based on the 3rd Generation Intel® Core™ i7 Processor with the Intel® QM77 Express Chipset

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Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

For Your Safety

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High Voltage Safety Instructions

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Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

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Special Handling and Unpacking Instructions

ESD Sensitive Device!

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Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

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General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Kontron grants the original purchaser of Kontron's products a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron.

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Chapter 1

Introduction

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1. Introduction

1.1 Board Overview

The CP6004-RA (Rugged Air-Cooled) / CP6004-RC (Rugged Conductive-Cooled) is a highly integrated 6U CompactPCI system controller board based on the 3rd generation Intel® Core™ i7 processor combined with the mobile Intel® QM77 Express Chipset.

The board supports the 3rd generation, Intel® Core™ i7-3612QE quad-core processor with 2.1 GHz and the Intel® Core™ i7-3555LE dual-core processor with 2.5 GHz. All processors are built on 22-nm technology and provided in a BGA package.

The CP6004-RA/-RC includes up to 16 GB dual-channel DDR3 soldered memory with Error Checking and Correction (ECC) running at 1600 MHz. Furthermore, up to 64 GB NAND flash memory (SSD) via a SATA Flash module can be integrated into the CP6004-RA/-RC.

The CP6004-RA has a front panel and comes with various interfaces such as up to five Gigabit Ethernet ports (three on front I/O and up to four on rear I/O in compliance with PICMG 2.16), four high-resolution graphics interfaces (DisplayPort, VGA, 2 x HDMI/DVI), two COM ports (RS-232 on front and rear I/O, RS-422/RS-232 on rear I/O), and five SATA interfaces with RAID 0/1/5/10 functionality, one for the SATA Flash module and four for rear I/O. In addition, six USB 2.0 ports, two on front I/O and four on rear I/O as well as four general purpose inputs (GPI) and four general purpose outputs (GPO) are available on the board. The CP6004-RA provides support for one standard PMC/XMC module either via one 64-bit/66 MHz PCI or 64-bit/133 MHz PCI-X PMC interface or via one XMC interface utilizing a x8 lane PCI Express 2.0 interconnection.

The CP6004-RC has no front panel and provides various interfaces such as four Gigabit Ethernet ports on rear I/O in compliance with PICMG 2.16, three high-resolution graphics interfaces (VGA, 2 x HDMI/DVI), two COM ports (RS-232 and RS-422/RS-232 on rear I/O), and five SATA interfaces with RAID 0/1/5/10 functionality, one for the SATA Flash module and four for rear I/O. In addition, four USB 2.0 ports on rear I/O as well as four general purpose inputs (GPI) and four general purpose outputs (GPO) are available on the board. The CP6004-RC provides support for one conduction-cooled PMC (CCPMC)/one conduction-cooled XMC either via one 64-bit/66 MHz PCI or 64-bit/133 MHz PCI-X PMC interface or via one XMC interface utilizing a x8 lane PCI Express 2.0 interconnection.

The CP6004-RA/-RC supports a configurable 64-bit/66 MHz PCI or PCI-X hot swap CompactPCI interface. When installed in the system slot, the interface is enabled, and when installed in a peripheral slot, the CP6004-RA/-RC is isolated from the CompactPCI bus. Safety and security features via a Trusted Platform Module (TPM) 1.2 are provided on request. Intelligent Platform Management Interface (IPMI) is supported as well.

The CP6004-RA/-RC has an extended operating temperature range and is ruggedized for high shock and vibration environments. The CP6004-RA provides a heat sink optimized for air cooling. The CP6004-RC provides a heat spreader extending across the whole board to enable the heat to be conducted from the board to the chassis. On the CP6004-RC two wedge locks are available for mounting the board in the chassis.

Designed for stability, the board fits into applications situated in industrial environments, including I/O intensive applications where only one slot is available for the CPU, making it a perfect core technology for long-life applications. Components with high temperature tolerance have been selected from embedded technology programs, and therefore offer long-term availability. The board is offered with various Board Support Packages including Windows, VxWorks and Linux operating systems. For further information concerning the operating systems available for the CP6004-RA/-RC, please contact Kontron.

1.2 CP6004-RA Board-Specific Information

The CP6004-RA is a rugged air-cooled CompactPCI single-board computer with front I/O. It is based on the 3rd generation Intel® Core™ i7 processor and specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

- Support for the following 3rd generation processors:
  - Intel® Core™ i7-3612QE (SV) quad-core processor, 2.1 GHz, 6 MB L3 cache
  - Intel® Core™ i7-3555LE (LV) dual-core processor, 2.5 GHz, 4 MB L3 cache
- Intel® QM77 Express Chipset
- Up to 16 GB, dual-channel, soldered DDR3 SDRAM memory with ECC running at 1600 MHz
- Integrated 3D high-performance graphics controller with up to four high-resolution graphics interfaces (VGA / DP / 2 x HDMI/DVI)
- 64-bit/66 MHz PCI or PCI-X CompactPCI interface (PICMG 2.0)
- One PMC slot with PCI functionality and rear I/O support; 64-bit/66 MHz PCI interface or 64-bit/133 MHz PCI-X interface
- One XMC slot utilizing a x8 lane PCI Express 2.0 interconnection
- Five Gigabit Ethernet interfaces:
  - Two Gigabit Ethernet interfaces switchable between front I/O and rear I/O
  - Two Gigabit Ethernet interfaces on rear I/O (PICMG 2.16)
  - One Gigabit Ethernet interface on front I/O
- Two Gigabit Ethernet (GbE) controllers:
  - One Intel® 82579LM Gigabit Ethernet controller connected to one GbE port on the front panel
  - One Intel® 82580EB Quad Gigabit Ethernet controller connected to two GbE ports on the front panel and two GbE ports on the rear I/O
- Five Serial ATA interfaces with SATA RAID 0/1/5/10 support:
  - One onboard SATA 6 Gb/s interface for the Serial ATA Flash module
  - Four SATA 3 Gb/s interfaces on the rear I/O
- Six USB ports:
  - Two USB 2.0 ports on the front panel
  - Four USB 2.0 ports on the rear I/O
- Two COM ports:
  - One RS-232 COM port either on the front panel or on the rear I/O (COMA)
  - One RS-422/RS-232 COM port on the rear I/O (COMB)
- TCG 1.2 compliant Trusted Platform Module (TPM), on request
- Two SPI boot flashes:
  - One standard SPI boot flash
  - One recovery SPI boot flash
- Four general purpose inputs (GPI) and four general purpose outputs (GPO) on rear I/O
- Watchdog timer
- Battery-backed real-time clock
- Three onboard DIP switches for board configuration
- Supports PICMG Packet Switching Backplane Specification 2.16
- IPMI support
- 4HP, 6U CompactPCI
- Passive heat sink solution for forced airflow cooling
- Rear I/O on J3, J4 and J5
- Hot swap capability: as system controller or as peripheral device
- AMI Aptio®, a uEFI-compliant platform firmware

1.3 CP6004-RC Board-Specific Information

The CP6004-RC is a rugged conductive-cooled CompactPCI single-board computer without front I/O. It is based on the 3rd generation Intel® Core™ i7 processor and specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

- Support for the following 3rd generation processors:
  - Intel® Core™ i7-3612QE (SV) quad-core processor, 2.1 GHz, 6 MB L3 cache
  - Intel® Core™ i7-3555LE (LV) dual-core processor, 2.5 GHz, 4 MB L3 cache
- Intel® QM77 Express Chipset
- Up to 16 GB, dual-channel, soldered DDR3 SDRAM memory with ECC running at 1600 MHz
- Integrated 3D high-performance graphics controller with up to three high-resolution graphics interfaces (VGA / 2 x HDMI/DVI)
- 64-bit/66 MHz PCI or PCI-X CompactPCI interface (PICMG 2.0)
- One conductive-cooled PMC slot with PCI functionality and rear I/O support; 64-bit/66 MHz PCI interface or 64-bit/133 MHz PCI-X interface
- One conductive-cooled XMC slot utilizing a x8 lane PCI Express 2.0 interconnection
- Four Gigabit Ethernet interfaces:
  - Two Gigabit Ethernet interfaces on rear I/O with disable option in uEFI BIOS
  - Two Gigabit Ethernet interfaces on rear I/O (PICMG 2.16)
- One Gigabit Ethernet controller:
  - One Intel® 82580EB Quad Gigabit Ethernet controller connected to the Gigabit Ethernet ports on the rear I/O
- Five Serial ATA interfaces with SATA RAID 0/1/5/10 support:
  - One onboard SATA 6 Gb/s interface for the Serial ATA Flash module
  - Four SATA 3 Gb/s interfaces on the rear I/O
- Four USB ports on the rear I/O
- Two COM ports:
  - One RS-232 COM port on the rear I/O (COMA)
  - One RS-422/RS-232 COM port on the rear I/O (COMB)
- TCG 1.2 compliant Trusted Platform Module (TPM), on request
- Two SPI boot flashes:
  - One standard SPI boot flash
  - One recovery SPI boot flash
- Four general purpose inputs (GPI) and four general purpose outputs (GPO) on rear I/O
- Watchdog timer
- Supports PICMG Packet Switching Backplane Specification 2.16
- IPMI support
- 4HP, 6U CompactPCI
- Passive heat sind solution for conductive-cooling
- Rear I/O on J3, J4 and J5
- AMI Aptio®, a uEFI-compliant platform firmware

1.4 System Expansion Capabilities

1.4.1 PMC/XMC Module (CP6004-RA)

The CP6004-RA has a 3.3V, rear I/O capable PMC mezzanine interface configurable for either 64-bit/66 MHz PCI or 64-bit/133 MHz PCI-X operation with support for PMC modules. For information on the PMC interface, refer to chapter 2.9.10, "PMC Interface".

The CP6004-RA has one XMC mezzanine interface for support of x1, x4 and x8 PCI Express 2.0 XMC modules. For information on the XMC interface, refer to chapter 2.9.11, "XMC Interface".

1.4.2 Conductive-Cooled PMC/XMC Module (CP6004-RC)

The CP6004-RC has a 3.3V, rear I/O capable PMC mezzanine interface configurable for either 64-bit/66 MHz PCI or 64-bit/133 MHz PCI-X operation with support for conductive-cooled PMC (CCPMC) modules. For information on the PMC interface, refer to chapter 2.9.10, "PMC Interface".

The CP6004-RC has one XMC mezzanine interface for support of x1, x4 and x8 PCI Express 2.0 conductive-cooled XMC modules. For information on the XMC interface, refer to chapter 2.9.11, "XMC Interface".

1.4.3 SATA Flash Module

The CP6004-RA/-RC provides support for up to 64 GB NAND flash memory in combination with an optional SATA Flash module, which is connected to the CP6004-RA/-RC via an on-board SATA extension connector. For further information concerning the SATA Flash module, please refer to Appendix A.

1.4.4 Rear I/O Module

The CP6004-RA/-RC provides support for one rear I/O module via the CompactPCI rear I/O connectors. For further information about the compatibility of rear I/O modules with the CP6004-RA/-RC, please refer to the CP6004-RA/-RC datasheet.

1.5 Version Comparison

Table 1-1: Version Comparison

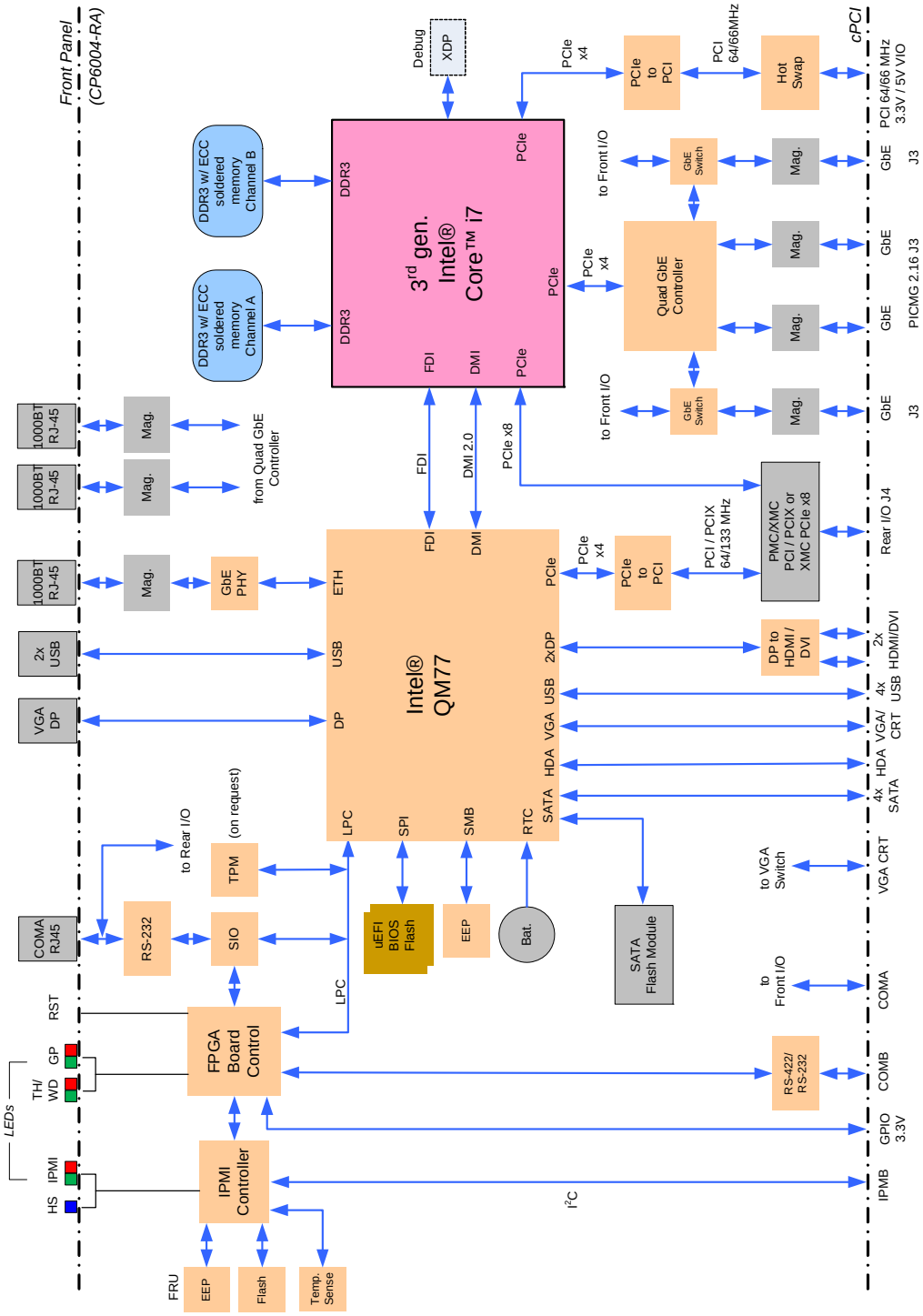
FEATURE	CP6004-RA	CP6004-RC
Heat sink	Air-cooled heat sink	Conductive-cooled heat sink
PMC/XMC	Standard PMC/XMC	Conductive-cooled PMC/XMC
Front Ethernet port	Up to 3 GbE ports	--
Rear Ethernet port	Up to four GbE ports	Up to four GbE ports
Front DisplayPort	1	--
Front COM port (RS-232)	1	--
Front LEDs	4	--
Cooling	Convection	Conduction

1.6 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

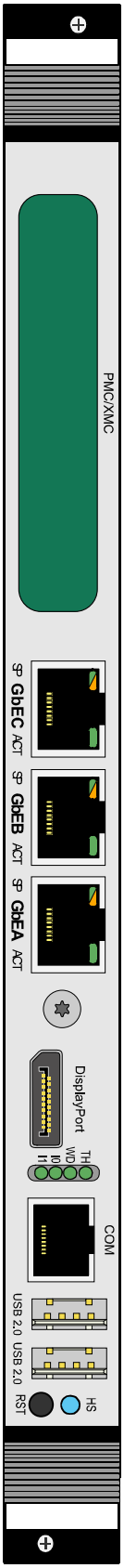
1.6.1 Functional Block Diagram

Figure 1-1: CP6004-RA/-RC Functional Block Diagram



1.6.2 Front Panel

Figure 1-2: CP6004-RA Front Panel



Legend:

IPMI LEDs

I0/I1 (red/green): Indicate the software status of the IPMI controller

Status LEDs

WD (green): Watchdog Status

TH (red/green): Temperature Status

HS (blue): Hot Swap Control

Integral Ethernet LEDs

ACT (green): Ethernet Link/Activity

SPEED (green/orange/off): Ethernet Speed

1.6.3 Board Layout

Figure 1-3: CP6004-RA Board Layout – Top View

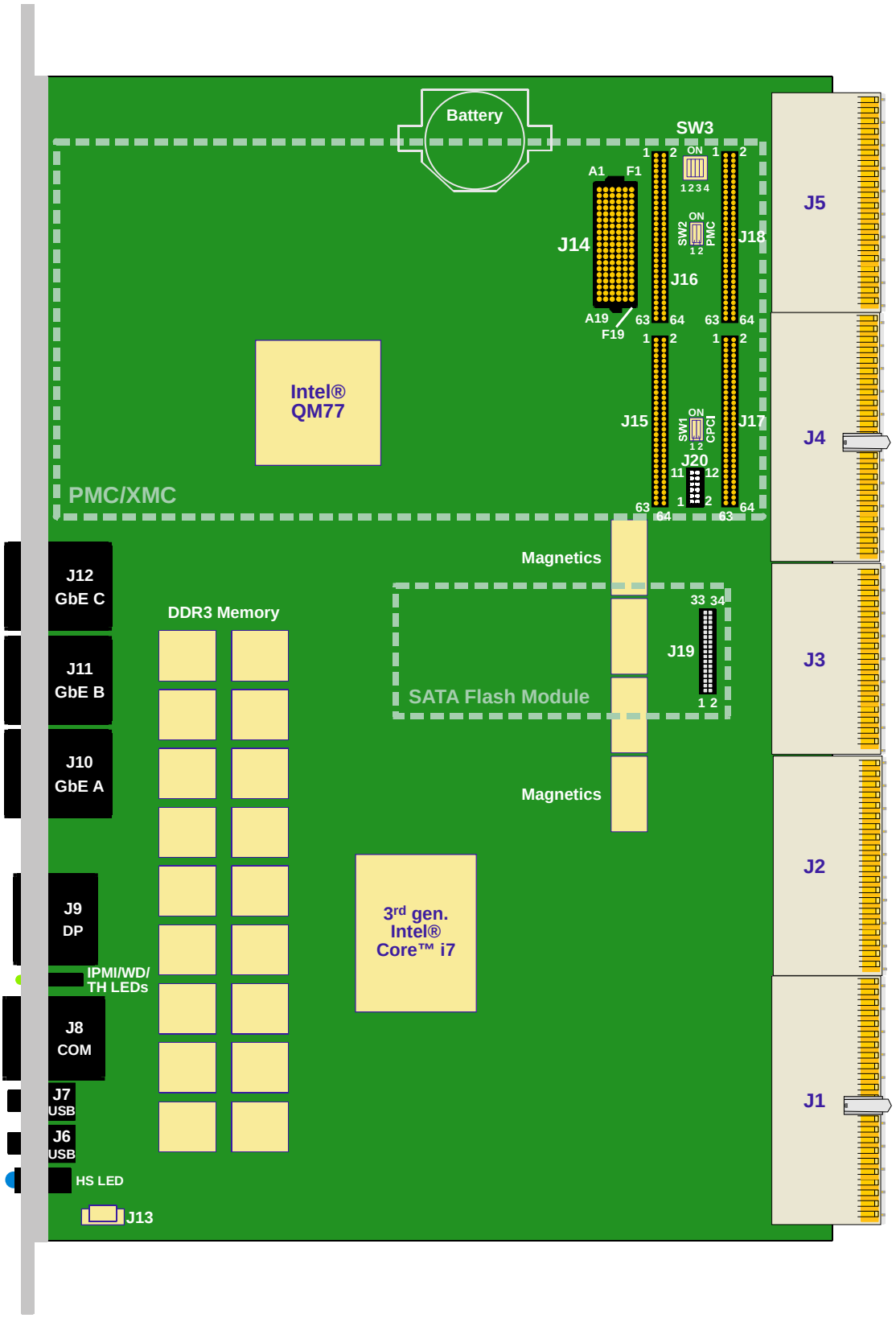


Figure 1-4: CP6004-RC Board Layout – Top View

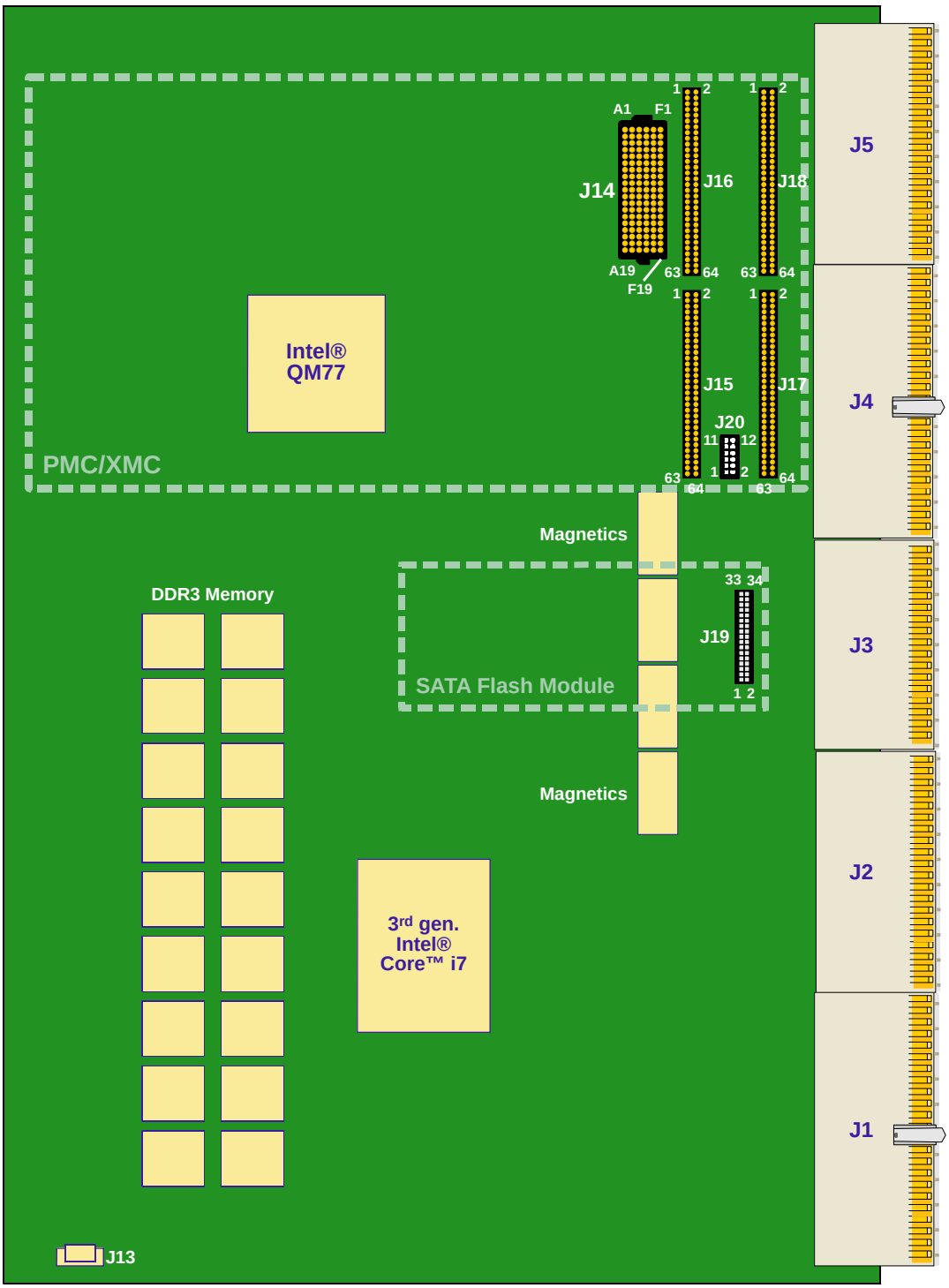


Figure 1-5: CP6004-RA Board Layout – Bottom View

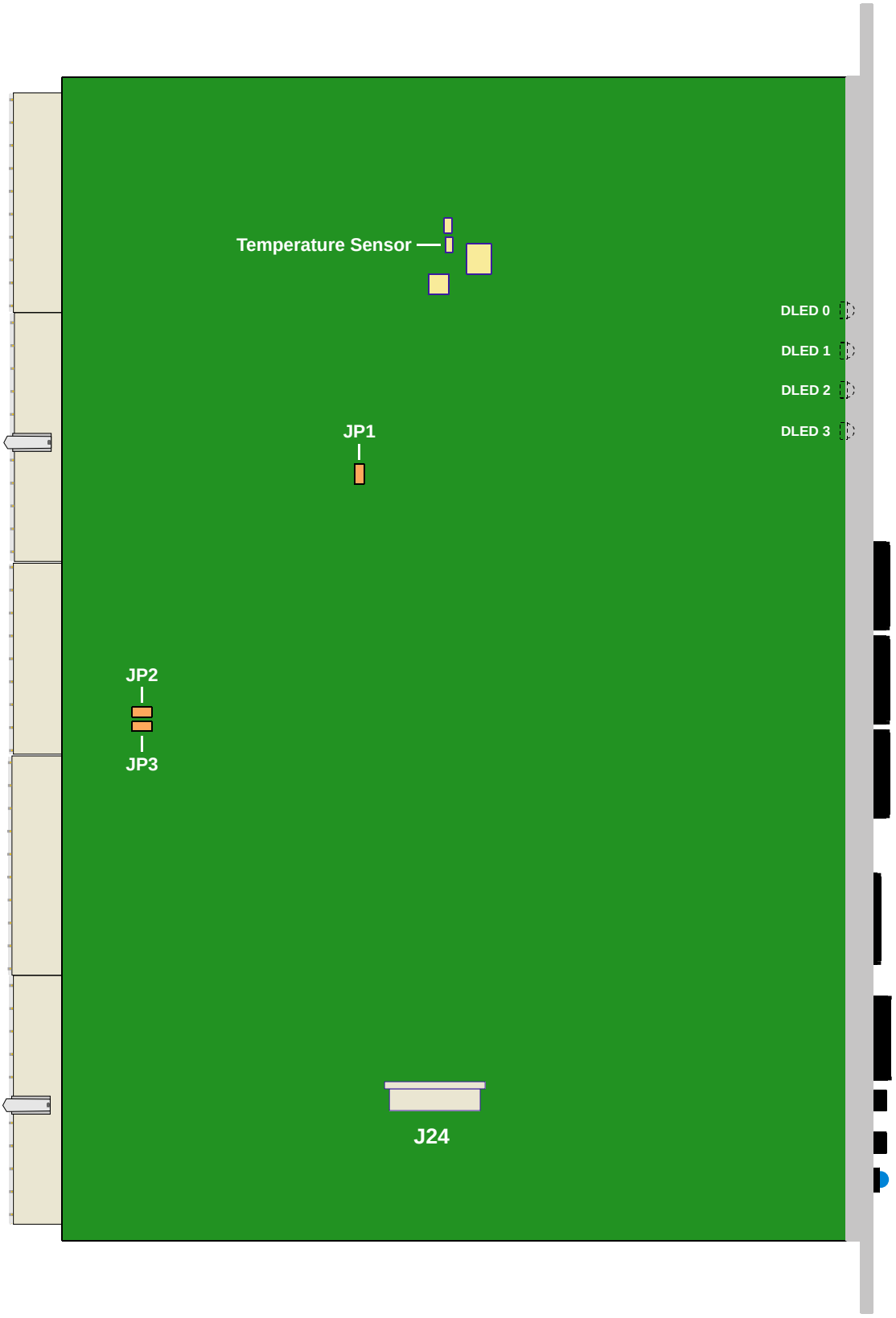
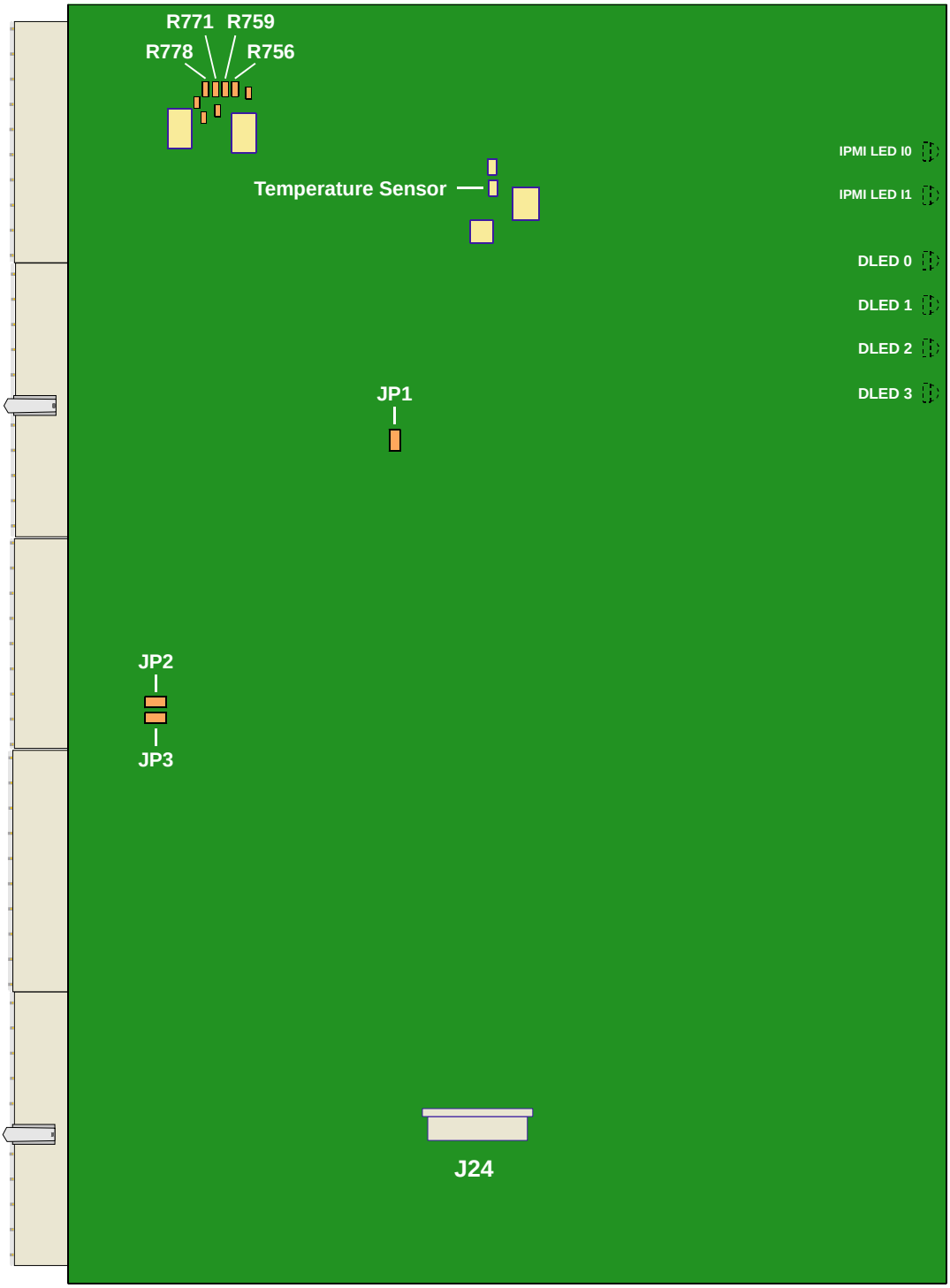


Figure 1-6: CP6004-RC Board Layout – Bottom View



1.7 Technical Specification

Table 1-2: CP6004-RA/-RC Main Specifications

FEATURES		SPECIFICATIONS
Processor and Memory	CPU	The CP6004-RA/-RC supports the following 3rd generation microprocessors: • Intel® Core™ i7-3612QE (SV) quad-core processor, 2.1 GHz, 6 MB L3 cache • Intel® Core™ i7-3555LE (LV) dual-core processor, 2.5 GHz, 4 MB L3 cache Further processor features: • Up to four execution cores • Intel® Hyper-Threading Technology (Intel® HT Technology) • Intel® 64 Architecture • Intel® Advanced Vector Extensions (AVX) floating point • Intel® Turbo Boost Technology 2.0 • Intel® Intelligent Power Sharing (IPS) • System memory interface with optimized support for dual-channel DDR3 SDRAM memory at 1600 MHz with ECC • Integrated 2D and 3D Graphics Engines • DMI 2.0 with 5 GT/s and FDI interfaces to the Intel® QM77 Chipset • One x8 and two x4 PCI Express 2.0 ports operating at 5 GT/s Please contact Kontron for further information concerning the suitability of other Intel processors for use with the CP6004-RA/-RC.

	Memory	Main Memory:
		• Up to 16 GB, dual-channel, soldered DDR3 SDRAM memory with ECC running at 1600 MHz
		Cache Structure:
		• 64 kB L1 cache for each core
		  • 32 kB instruction cache
		  • 32 kB data cache
		• 256 kB L2 shared instruction/data cache for each core
		• Up to 6 MB L3 shared instruction/data cache
		Flash Memory:
		• Two SPI flashes (2 x 8 MB) for uEFI BIOS and controlled by the IPMI controller
		• Up to 64 GB NAND flash via an onboard Serial ATA Flash module (SSD)
		Serial EEPROM with 64 kbit

Table 1-2: CP6004-RA/-RC Main Specifications (Continued)

FEATURES		SPECIFICATIONS

Chipset	Intel® QM77	Mobile Intel® QM77 Express Chipset:
		• Two x4 or eight x1 PCI Express 2.0 ports operating at 5 GT/s (only one x4 PCI Express port is used on the CP6004-RA/-RC)
		• SATA host controller with five ports and RAID 0/1/5/10 support
		  • One SATA 6 Gb/s ports accessible via an onboard connector
		  • Four SATA 3 Gb/s ports accessible via rear I/O
		• USB 2.0 host interface with up to 14 USB ports available (only six ports are used on the CP6004-RA/-RC)
		• USB 3.0 host interface with up to 4 USB ports available (not used on the CP6004-RA/-RC)
		• Integrated Ethernet controller
		• SPI flash interface support
		• Low Pin Count (LPC) interface
		• Power management logic support
		• Enhanced DMA controller, interrupt controller, and timer functions
		• System Management Bus (SMBus) compatible with most I²C™ devices
		• DMI 2.0 with 5 GT/s and FDI interfaces to the processor
		• High Definition Audio (HDA) interface
		• Analog display port
		• Three digital display ports
		• Integrated RTC

Integrated Controller	Graphics controller	High-performance 3D graphics controller integrated in the processor: • Support for two independent displays • Supports analog displays (CRT) up to a resolution of 2048 x 1536 pixels with 32-bit color @ 75 Hz • Supports digital displays (HDMI/DVI) up to a resolution of 1920 x 1200 pixels @ 60 Hz • Supports digital display (DP) up to a resolution of 2560 x 1600 pixels @ 60 Hz • Dynamic Video Memory Technology (DVMT)
Interfaces	CompactPCI	Compliant with the CompactPCI Specification PICMG 2.0 R 3.0: • System controller operation • 64-bit/66 MHz PCI or PCI-X master interface with dedicated PCIe-to-PCI-X bridge • 3.3V or 5V signaling levels (universal signaling support) Compliant with the Packet Switching Specification PICMG 2.16. The CP6004-RA/-RC supports System Master hot swap functionality and application-dependent hot swap functionality when used in a peripheral slot. When used as a System Master, the CP6004-RA/-RC supports individual clocks for each slot and the ENUM signal handling is in compliance with the PICMG 2.1 Hot Swap Specification. When installed in a peripheral slot, the CP6004-RA/-RC is isolated from the CompactPCI bus. It receives power from the backplane and supports rear I/O and, if the system supports it, packet switching (in this case up to two channels of Gigabit Ethernet).

Table 1-2: CP6004-RA/-RC Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Interfaces	Rear I/O	The following interfaces are routed to the rear I/O connectors J3 and J5. • COMA (RS-232 signaling) and COMB (RS-422/RS-232 signaling); no buffer on the rear I/O module is necessary • 4 x USB 2.0 • 1 x CRT VGA, 2 x HDMI/DVI • 1 x HDA • 2 x Gigabit Ethernet (compliant with PICMG 2.16, R 1.0) • 2 x Gigabit Ethernet • 4 x SATA 3 Gb/s • 4 x GPIs and 4 x GPOs (LVTTL signaling) The rear I/O connector J4 provides rear I/O interconnection to the PMC/XMC interface.
	Gigabit Ethernet	Up to five 10 Base-T/100 Base-TX/1000 Base-T Gigabit Ethernet interfaces based on one Intel® 82579LM Gigabit Ethernet controller and one Intel® 82580EB Quad Gigabit Ethernet controller: • Three RJ-45 connectors on the front panel (CP6004-RA) • Two ports switchable between front I/O and to rear I/O (CP6004-RA) • Two Gigabit Ethernet interfaces on rear I/O with disable option in uEFI BIOS (CP6004-RC) • Two ports on the rear I/O (PICMG 2.16) • Automatic mode recognition (Auto-Negotiation) • Automatic cabling configuration recognition (Auto-MDI/X)
	USB	Up to six USB ports supporting UHCI (USB 1.1) and EHCI (USB 2.0): • Two type A USB 2.0 connectors on the front panel (CP6004-RA) • Four USB 2.0 ports on the rear I/O interface
	Serial	The CP6004-RA provides two 16C550-compatible UARTs : • One RS-232 port either on the front panel or on the rear I/O, COMA • One RS-422/RS-232 port on the rear I/O, COMB The CP6004-RC provides two 16C550-compatible UARTs : • One RS-232 port on the rear I/O, COMA • One RS-422/RS-232 port on the rear I/O, COMB
	PMC	PMC interface: • Four onboard mezzanine connectors, (Jn1-Jn4), for connecting a PMC module • Up to 64-bit/66 MHz PCI or up to 64-bit/133 MHz PCI-X interface with dedicated PCIe-to-PCI-X bridge • Only 3.3V PCI signaling voltage • Rear I/O supported through the CompactPCI connector J4 • Supported voltages: 3.3 V, 5 V, +12 V, and -12 V • Support for PMC modules (CP6004-RA) • Support for CCPMC modules (CP6004-RC)
	XMC	XMC interface: • One onboard XMC connector (P15) • Up to x8 lanes PCI Express 2.0 ports operating at 5 GT/s • Rear I/O supported through the PMC connector (Jn4) to the CompactPCI connector J4 • Support for XMC modules (CP6004-RA) • Support for conductive-cooled XMC modules (CP6004-RC)

Table 1-2: CP6004-RA/-RC Main Specifications (Continued)

	FEATURES	SPECIFICATIONS
Interfaces	Serial ATA	One Serial ATA 6 Gb/s interfaces for: • One onboard SATA 6 Gb/s interface for the Serial ATA Flash module (up to 64 GB flash memory) Four SATA 3 Gb/s ports accessible via rear I/O
Sockets	Front Panel Connectors (CP6004-RA)	• DP: one 20-pin DisplayPort connector, J9 • USB: two 4-pin, type A connectors, J6 and J7 • Ethernet: three 8-pin, RJ-45 connectors, J10, J11 and J12 • Serial port: one 8-pin, RJ-45 connector, J8 (COMA) • PMC/XMC front panel bezel cutout
	Onboard Connectors	• PMC connectors J15 - J18 (Jn1 - Jn4) • XMC connector, J14 • One 34-pin, SATA extension connector, J19 • JTAG connector, J20 • Debug connector, J22 • XDP-SFF (debug) connector, J24 • CompactPCI Connectors J1 - J5
Switches	DIP Switches (CP6004-RA)	Three onboard DIP switches, SW1, SW2, and SW3, for board configuration
	Reset Switch (CP6004-RA)	One front panel hardware reset switch
	Hot Swap Switch (CP6004-RA)	One switch for hot swap purposes integrated in the front panel handle in accordance with PICMG 2.1 Rev. 2.0.
LEDs	System LEDs	System Status LEDs on the CP6004-RA: • I0/I1 (red/green): Indicate the software status of the IPMI controller • WD (green): Watchdog Status • TH (red/green): Temperature Status • HS (blue): Hot Swap Control System Status LEDs on the CP6004-RC: • I0/I1 (red/green): Indicate the software status of the IPMI controller (located on the rear side of the board) Debug LEDs (CP6004-RA/-RC): • DLED0-3 (red/green): Onboard LEDs for debugging purposes (located on the rear side of the board)
	Ethernet LEDs (CP6004-RA)	Gigabit Ethernet Status: • ACT (green): Ethernet Link/Activity • SPEED (green/orange/off): Ethernet Speed

Table 1-2: CP6004-RA/-RC Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Timer	Watchdog Timer	• Software-configurable, two-stage Watchdog with programmable timeout ranging from 125 ms to 4096 s in 16 steps • Serves for generating IRQ or hardware reset
	System Timer	• The Intel® QM77 Chipset contains three 8254-style counters which have fixed uses • In addition to the three 8254-style counters, the Intel® QM77 Chipset includes eight individual high-precision event timers that may be used by the operating system. They are implemented as a single counter each with its own comparator and value register.
IPMI	IPMI Controller	• NXP® ARM7 microcontroller with redundant 512 kB firmware flash and automatic roll-back strategy • The IPMI controller carries out IPMI commands such as monitoring several onboard temperature conditions, board voltages and the power supply status, and managing hot swap operations. • The IPMI controller is accessible via two IPMBs (through the J1 and J2 connectors) and one host Keyboard Controller Style (KCS) interface.

Thermal	Thermal Management	CPU and board overtemperature protection is provided by:
		• Temperature sensors integrated in the 3rd generation Intel® Core™ i7 processor:
		  • One temperature sensor for monitoring each processor core
		  • One temperature sensor for monitoring the graphics core
		  • One temperature sensor for monitoring the package die temperature
		• One temperature sensor integrated in the Intel® QM77 Chipset for monitoring the chipset
		• One onboard temperature sensor for monitoring the board temperature
		• Specially designed heat sink

Security	TPM	Trusted Platform Module (TPM) 1.2 for enhanced hardware- and software-based data and system security (on request)

Table 1-2: CP6004-RA/-RC Main Specifications (Continued)

	FEATURES	SPECIFICATIONS
Software	uEFI BIOS	AMI Aptio®, AMI's next-generation BIOS firmware based on the uEFI Specification and the Intel Platform Innovation Framework for EFI. • LAN boot capability for diskless systems (standard PXE) • Automatic fail-safe recovery in case of a damaged image • Non-volatile storage of setting in the SPI flash (battery only required for the RTC) • Compatibility Support Module (CSM) providing legacy BIOS compatibility based on AMIBIOS8 • Command shell for diagnostics and configuration • uEFI Shell commands executable from mass storage device in a Pre-OS environment (open interface) • IPMI support in the command shell
	Software IPMI	IPMI firmware providing the following features: • The IPMI controller is accessible via up to two IPMBs, IOL and one KCS interface with interrupt support • The IPMI firmware can be updated in field through all supported interfaces using the function "fwum..." of the open-source tool "ipmitool". For further information on the ipmitool refer to the sourceforge.net website. • Two IPMI controller flash banks with automatic roll-back capability in case of an upgrade firmware failure • Board supervision and control extensions such as board reset, power and SPI flash control, etc.
	Operating Systems	The board is offered with various Board Support Packages including Windows, VxWorks and Linux operating systems. For further information concerning the operating systems available for the CP6004-RA/-RC, please contact Kontron.

Table 1-2: CP6004-RA/-RC Main Specifications (Continued)

FEATURES		SPECIFICATIONS
General	Mechanical	6U, 4HP, CompactPCI-compliant form factor
	Power Consumption	See Chapter 5 for details.
	Temperature Ranges	Operational temperature of CP6004-RA without TPM (with forced airflow): • CP6004-RA with Core™ i7-3612QE (SV): -40°C to +70°C • CP6004-RA with Core™ i7-3555LE (LV): -40°C to +70°C Operational temperature of CP6004-RC without TPM: • Card edge temperature of CP6004-RC with Core™ i7-3612QE (SV) at the maximum frequency of 2.1 GHz: -40°C to + 75°C • Card edge temperature of CP6004-RC with Core™ i7-3612QE (SV) at a reduced frequency of 1.5 GHz: -40°C to + 85°C • Card edge temperature of CP6004-RC with Core™ i7-3555LE (LV) at the maximum frequency of 2.5 GHz: -40°C to + 70°C • Card edge temperature of CP6004-RC with Core™ i7-3555LE (LV) at a reduced frequency of 1.8 GHz: -40°C to + 80°C Operational temperature of TPM: -25°C to +70°C Storage temperature of CP6004-RA without hard disk and without battery: -40°C to +85°C Storage temperature of CP6004-RC without hard disk and without battery: -55°C to +105°C  *Note ...* When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CP6004-RA (See "Battery" below).  *Note ...* When additional components are installed, refer to their operational specifications as this will influence the operational and storage temperature of the CP6004-RA/-RC.
	Battery (CP6004-RA)	3.0V lithium battery for RTC with battery socket. Battery type: UL-approved CR2025 Temperature ranges: Operational: -20°C to +70°C typical (refer to the battery manufacturer's specifications for exact range) Storage: -55°C to +70°C typical (no discharge)
	Dimensions	233.35 mm x 160 mm
	Board Weight	CP6004-RA: 725 g (with heat sink but without mezzanine cards) CP6004-RC: 828 g (with heat sink but without mezzanine cards)

1.8 Standards

The CP6004-RA/-RC complies with the requirements of the following standards:

Table 1-3: Standards for the CP6004-RA

TYPE	ASPECT	STANDARD	REMARKS
CE	Emission	EN55022 EN61000-6-3	--
	Immission	EN55024 EN61000-6-2	--
	Electrical Safety	EN60950-1	--
Mechanical	Mechanical Dimensions	IEEE1101.10	--
Environmental	Climatic Humidity	IEC60068-2-78	93% RH at 40°C, non-condensing See note below.
	WEEE	Directive 2002/96/EC	Waste electrical and electronic equipment
	RoHS 2	Directive 2011/65/EU	Restriction of the use of certain hazardous substances in electrical and electronic equipment
	Random Vibration (Broadband)	ANSI/VITA 47 (Class V2)	Test parameters: • 5-100 (Hz) frequency range: +3dB slope • 100-1000 (Hz) freq. range: 0.04 (g^2/Hz) • 1000-2000 (Hz) freq. range: -6dB slope • 7.619 g (rms) • 60 (min) test duration/axis • 3 axes
	Single Shock	ANSI/VITA 47 (Class OS1)	Test parameters: • 20 (g) acceleration • 11 (ms) shock duration half sine • 3 shocks per direction • 6 directions • 5 (s) recovery time

Note ...

Kontron performs comprehensive environmental testing of its products in accordance with applicable standards.

Customers desiring to perform further environmental testing of Kontron products must contact Kontron for assistance prior to performing any such testing. This is necessary, as it is possible that environmental testing can be destructive when not performed in accordance with the applicable specifications.

In particular, for example, boards **without conformal coating** must not be exposed to a change of temperature exceeding 1K/minute, averaged over a period of not more than five minutes. Otherwise, condensation may cause irreversible damage, especially when the board is powered up again.

Kontron does not accept any responsibility for damage to products resulting from destructive environmental testing.

Table 1-4: Standards for the CP6004-RC

TYPE	ASPECT	STANDARD	REMARKS
CE	Emission	EN55022 EN61000-6-3	--
	Immission	EN55024 EN61000-6-2	--
	Electrical Safety	EN60950-1	--
Mechanical	Mechanical Dimensions	ANSI/VITA 30.1	--
Environmental	Climatic Humidity	ANSI/VITA 47	95% RH at +30°C to +60°C, condensing
	WEEE	Directive 2002/96/EC	Waste electrical and electronic equipment
	RoHS 2	Directive 2011/65/EU	Restriction of the use of certain hazardous substances in electrical and electronic equipment
	Random Vibration (Broadband)	ANSI/VITA 47 (Class V3)	Test parameters: • 5-100 (Hz) frequency range: +3dB slope • 100-1000 (Hz) freq. range: 0.1 (g^2/Hz) • 1000-2000 (Hz) freq. range: -6dB slope • 12.05 g (rms) • 60 (min) test duration/axis • 3 axes
	Single Shock	ANSI/VITA 47 (Class OS2)	Test parameters: • 40 (g) acceleration • 11 (ms) shock duration half sine • 3 shocks per direction • 6 directions • 5 (s) recovery time

1.9 Related Publications

The following publications contain information relating to this product.

Table 1-5: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems and Boards	CompactPCI Specification PICMG 2.0, Rev. 3.0 CompactPCI Packet Switching Backplane Specification PICMG 2.16 Rev. 1.0 CompactPCI System Management Specification PICMG 2.9 Rev. 1.0 CompactPCI Hot Swap Specification PICMG 2.1 Rev. 2.0
	IPMI - Intelligent Platform Management Interface Specification v2.0
	Kontron CompactPCI Backplane Manual, ID 24229
PMC Module	IEEE 1386-2001, IEEE Standard for a Common Mezzanine Card (CMC) Family IEEE 1386.1-2001, IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)
XMC Module	ANSI/VITA 42.0-200x XMC Switched Mezzanine Card Auxiliary Standard ANSI/VITA 42.3-2006 XMC PCI Express Protocol Layer Standard
Platform Firmware	Unified Extensible Firmware Interface (uEFI) Specification, Version 2.1
All Kontron products	Product Safety and Implementation Guide, ID 1021-9142
Kontron	CP6004-RA/-RC uEFI BIOS User Guide
	CP6004-RA/-RC IPMI Firmware User Guide

Chapter 2

Functional Description

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2. Functional Description

The CP6004-RA/-RC supports the 3rd generation the 3rd generation Intel® Core™ i7-3612QE quad-core processor with 2.1 GHz and the 3rd generation Intel® Core™ i7-3555LE dual-core processor with 2.5 GHz.

The 3rd generation Intel® Core™ i7 processor used on the CP6004-RA/-RC include an integrated high-performance graphics controller and a DDR3 dual-channel memory controller with ECC support as well as one x8 and two x4 PCI Express 2.0 ports operating at 5 GT/s. They support various technologies, such as:

- Intel® Hyper-Threading Technology
- Intel® Turbo Boost Technology 2.0
- Intel® Intelligent Power Sharing (Intel® IPS)
- Intel® Enhanced SpeedStep® Technology
- Intel® Virtualization Technology (Intel® VT-x)
- Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Advanced Vector Extensions (Intel® AVX)
- Intel® Streaming SIMD Extensions 4.1 (Intel® SSE4.1)
- Intel® Streaming SIMD Extensions 4.2 (Intel® SSE4.2)
- Intel® 64 Architecture
- Execute Disable Bit

The Intel® Turbo Boost Technology and the Intel® Intelligent Power Sharing technology allow the processor and the graphics controller to opportunistically and automatically run faster than its rated operating clock frequency if it is operating below power, temperature, and current limits.

The Intel® Enhanced SpeedStep® technology enables real-time dynamic switching of the voltage and frequency between several modes. This is achieved by switching the bus ratios, the core operating voltage, and the core processor speeds without resetting the system.

The Intel® Advanced Vector Extensions (AVX) is a 256-bit instruction set extension to SSE designed for applications that are Floating Point (FP) intensive. Intel® AVX accelerates compute performance for signal and image processing applications.

The 3rd generation Intel® Core™ i7 processor used on the CP6004-RA/-RC have the following multi-level cache structure:

- 64 kB L1 cache for each core
  - 32 kB instruction cache
  - 32 kB data cache
- 256 kB L2 instruction/data cache for each core
- Up to 6 MB L3 shared instruction/data cache shared between both cores

Table 2-1: Features of the Processors Supported on the CP6004-RA/-RC

FEATURE	Core™ i7-3612QE (SV) 2.1 GHz	Core™ i7-3555LE (LV) 2.5 GHz
Processor Cores	four	two
Processor Base Frequency	2.1 GHz	2.5 GHz
Maximum Turbo Frequency	3.3 GHz	3.2 GHz
L1 cache per core	64 kB	64 kB
L2 cache per core	256 kB	256 kB
L3 cache	6 MB	4 MB
DDR3 Memory	up to 16 GB / 1600 MHz	up to 16 GB / 1600 MHz
Graphics Base Frequency	650 MHz	550 MHz
Graphics Max. Dynamic Frequency	1.0 GHz	950 MHz
Thermal Design Power	35 W	25 W

2.1 Memory

The CP6004-RA/-RC supports a soldered, dual-channel (144-bit), Double Data Rate (DDR3) memory with Error Checking and Correction (ECC) running at 1600 MHz (memory error detection and reporting of 1-bit and 2-bit errors and correction of 1-bit failures). The available memory configuration ca be either 4 GB, 8 GB or 16 GB.

However, when the internal graphics controller is enabled, the amount of memory available to applications is less than the total physical memory in the system. For example, the chipset's Dynamic Video Memory Technology dynamically allocates the proper amount of system memory required by the operating system and the application.

2.2 Intel® QM77 Express Chipset

The CP6004-RA/-RC is equipped with the mobile Intel® QM77 Express Chipset, a highly integrated platform controller hub (PCH) with the following features:

- Two x4 or eight x1 PCI Express 2.0 ports operating at 5 GT/s (only one x4 PCI Express port is used on the CP6004-RA/-RC)
- SATA host controller with six ports and RAID 0/1/5/10 support
- One SATA 6 Gb/s port accessible via onboard connector
- Four SATA 3 Gb/s ports accessible via rear I/O
- USB 2.0 host interface with up to 14 USB ports available (only up to six ports are used on the CP6004-RA/-RC)
- USB 3.0 host interface with up to 4 USB ports available (not used on the CP6004-RA/-RC)
- Integrated Ethernet controller
- SPI flash interface support
- Low Pin Count (LPC) interface
- Power management logic support
- Enhanced DMA controller, interrupt controller, and timer functions

- System Management Bus (SMBus) compatible with most I²C™ devices
- DMI 2.0 with 5 GT/s and FDI interfaces to the processor

2.3 Timer

The CP6004-RA/-RC is equipped with the following timers:

- Real-Time Clock
  The Intel® QM77 Chipset integrates an MC146818B-compatible real-time clock with 256 byte CMOS RAM. All CMOS RAM data remain stored in an additional EEPROM device to prevent data loss.
- Counter/Timer
  Three 8254-style counter/timers are included on the CP6004-RA/-RC as defined for the PC/AT.
- The Intel® QM77 Chipset integrates eight high-precision event timers.

2.4 Watchdog Timer

The CP6004-RA/-RC provides a Watchdog timer that is programmable for a timeout period ranging from 125 ms to 4096 s in 16 steps. Failure to trigger the Watchdog timer in time results in a system reset or an interrupt. In dual-stage mode, it results in a combination of both interrupt and reset if the Watchdog is not serviced. A hardware status flag will be provided to determine if the Watchdog timer generated the reset.

2.5 Battery

The CP6004-RA is provided with a 3.0 V “coin cell” lithium battery for the RTC. For further information concerning the battery and its replacement, refer to Chapter 3.2.6, Battery Replacement.

2.6 Reset

The CP6004-RA/-RC is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit or in the event of a power failure of the DC/DC converters. Other reset sources include the Watchdog timer and the push-button switch on the front panel. The CP6004-RA/-RC responds to any of these sources by initializing local peripherals.

A reset will be generated if one the following events occurs:

- Drop in voltage below the acceptable operating limit
- Power failure of at least one onboard DC/DC converter
- Push-button "RESET" pressed (on the front panel of the CP6004-RA)
- Watchdog expired
- CPCI backplane PRST input
- CPCI backplane RST input (software-configurable when the board is in peripheral mode)

2.7 Flash Memory

The CP6004-RA/-RC provides flash interfaces for the uEFI BIOS and the SATA Flash module.

2.7.1 SPI Boot Flash for uEFI BIOS

The CP6004-RA/-RC provides two 8 MB SPI boot flashes for two separate uEFI BIOS images, a standard SPI boot flash and a recovery SPI boot flash. The fail-over mechanism for the uEFI BIOS recovery can be controlled via the IPMI controller or the DIP switch SW3 on the CP6004-RA and a configuration resistor on the CP6004-RC. If the standard SPI boot flash is corrupted, the IPMI controller automatically enables the recovery SPI boot flash and boots the system again.

The SPI flash includes a hardware write protection option, which can be configured via the uEFI BIOS. If write protection is enabled, the SPI flash cannot be written to.

Note ...

The uEFI BIOS code and settings are stored in the SPI boot flash. Changes made to the uEFI BIOS settings are available only in the currently selected SPI boot flash.Thus, switching over to the other SPI boot flash may result in operation with different uEFI BIOS code and settings.

2.7.2 Serial ATA Flash Module (Optional)

The CP6004-RA/-RC supports up to 64 GB of NAND flash memory in combination with an optional Serial ATA Flash module, which is connected to the onboard connector J19.

The Serial ATA Flash module is an SLC-based SATA NAND flash drive with a built-in full hard-disk emulation and a high data transfer rate (sustained read rate with up to 100 MB/s and sustained write rate with up to 90 MB/s). It is optimized for embedded systems providing high performance, reliability and security.

Note ...

Write protection is available for this module. Contact Kontron for further assistance if write protection is required.

2.8 Trusted Platform Module 1.2 (On Request)

The CP6004-RA/-RC has been designed to support the Trusted Platform Module (TPM) 1.2. This feature is available on request. TPM1.2 is a security chip specifically designed to provide enhanced hardware- and software-based data and system security. It stores sensitive data such as encryption and signature keys, certificates and passwords, and is able to withstand software attacks to protect the stored information.

Hardware features of the TPM 1.2:

- TCG 1.2 compliant Trusted Platform Module (TPM)
- Security architecture based on the Infineon SLE66CXxxPE security controller family
- EEPROM for TCG firmware enhancements and for user data and keys
- Advanced Crypto Engine (ACE) with RSA support up to 2048-bit key length
- Hardware accelerator for SHA-1 hash algorithm
- True Random Number Generator (TRNG)
- Tick counter with tamper detection
- Protection against Dictionary Attack
- Intel® Trusted Execution Technology Support
- Full personalization with Endorsement Key (EK) and EK certificate

2.9 Board Interfaces

2.9.1 Onboard and Front Panel LEDs

The CP6004-RA is equipped with two IPMI LEDs (I0 and I1), one Watchdog Status LED (WD LED), one Temperature Status LED (TH LED), and one Hot Swap LED (HS LED) on the front panel and four onboard Debug LEDs (DLED 0..3) located on the rear side of the board.

The CP6004-RC is equipped with two onboard IPMI LEDs and four onboard Debug LEDs (DLED 0..3) located on the rear side of the board.

The functionality of the Debug LEDs is described in Chapter 2.10.1.3 and reflected in the registers mentioned in Chapter 4, Configuration.

2.9.1.1 IPMI LEDs and Hot Swap LED

The IPMI LEDs I0 and I1 show the software status of the IPMI controller. The Hot Swap LED (CP6004-RA) indicates when the board may be extracted. It can be switched on or off by software and may be used, for example, to indicate that the shutdown process is finished and the board is ready for extraction.

The following table indicates the function of the IPMI LEDs and the Hot Swap LED.

Table 2-2: IPMI LEDs and Hot Swap LED Function

LED	COLOR	NORMAL MODE	OVERRIDE MODE
I0 (right)	red	Off = board powered / running	Selectable by user • Only lamp test
		On = board out of service (firmware not running)	
	green	Pulsing = traffic on the IPMB bus	
I1 (left)	red	On = health error detected	Selectable by user • Only lamp test
	green	Off = no health error detected Pulsing = KCS interface active Blinking = IPMI controller running showing its heart beat	
	red/amber	Slow blinking = health error detected, IPMI controller running showing its heart beat Pulsing = health error detected, KCS interface active	
HS LED (CP6004-RA)	blue	On = a) board ready for hot swap extraction, or b) board has just been inserted in a powered system Off = board in normal operation (do not extract the board) Blinking = board hot swap in progress; board not ready for extraction	Selectable by user • Only lamp test

2.9.1.2 Watchdog LED and Temperature Status LED

The CP6004-RA provides one Watchdog Status LED (WD LED) and one Temperature Status LED (TH LED).

Note ...

If the TH LED flashes red at regular intervals, it indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature.

Once activated, THERMTRIP# remains latched until a cold restart of the CP6004-RA is undertaken (all power off and then on again).

Table 2-3: Watchdog LED and Temperature Status LED Function

LED	COLOR	FUNCTION DURING BOOT-UP	FUNCTION AFTER BOOT-UP
WD LED (CP6004-RA)	red / green	The WD LED is not lit during boot-up.	Watchdog Status The WD LED states are: • Off: Watchdog inactive • Green: Watchdog active, waiting to be triggered • Red: Watchdog expired
TH LED (CP6004-RA)	red / green	The TH LED is lit green during boot-up.	Temperature Status The TH LED states are: • Off: Power failure • Green: If the CPU temperature is below 105°C • Red: In case of overtemperature of the CPU, i.e. the CPU has reached a temperature above 105°C • Red blinks: If the CPU has been shut off, i.e. the CPU has reached a temperature above 125°C In this event, all Debug LEDs (DLED3..0) are blinking red as well.

2.9.1.3 Debug LEDs

The CP6004-RA/-RC provides four onboard Debug LEDs (DLED0..3) located on the rear side of the board. They indicate the boot-up POST code after which they are available to the application.

If the DLED0..3 are lit red during boot-up, a failure is indicated before the uEFI BIOS has started. In this case, check the power supply. If the power supply appears to be functional and the LEDs are still red, please contact Kontron for further assistance.

The POST code is indicated during the boot-up phase. After boot-up, the LEDs indicate Debug or Port 80 signals, depending on the uEFI BIOS settings. The default setting after boot-up is Debug.

Table 2-4: Debug LEDs Function

LED	COLOR	FUNCTION DURING BOOT-UP	FUNCTION DURING uEFI BIOS POST (if POST code config. is enabled)	FUNCTION AFTER BOOT-UP
DLED3	red	When lit up during boot-up, it indicates a power-on reset.	--	Debug or Port 80 *Default: Debug*
	green	--	uEFI BIOS POST bit 3 and bit 7	
	amber	--	--	
DLED2	red	When lit, it indicates a catastrophic CPU error.	--	Debug or Port 80 *Default: Debug*
	green	--	uEFI BIOS POST bit 2 and bit 6	
	amber	--	--	
DLED1	red	When lit up during boot-up, it indicates a hardware reset.	--	Debug or Port 80 *Default: Debug*
	green	--	uEFI BIOS POST bit 1 and bit 5	
	amber	--	--	
DLED0	red	When lit up during boot-up, it indicates a uEFI BIOS boot failure.	--	Debug or Port 80 *Default: Debug*
	green	--	uEFI BIOS POST bit 0 and bit 4	
	amber	--	--	

Note ...

The bit allocation for Port 80 is the same as for the POST code.

For further information regarding the configuration of the Debug LEDs, refer to Chapter 4.5.14, LED Configuration Register, and Chapter 4.5.15, LED Control Register.

How to Read the 8-Bit POST Code

Due to the fact that only 4 bits are available and 8 bits must be displayed, the POST code output is multiplexed on the Debug LEDs.

Table 2-5: POST Code Sequence

STATE	DEBUG LEDs
0	All LEDs are OFF; start of sequence
1	High nibble
2	Low nibble

The following is an example of the Debug LEDs' operation if the POST configuration is enabled (see also Table 2-4, "Debug LEDs Function").

Table 2-6: POST Code Example

	DLED3	DLED2	DLED1	DLED0	RESULT
HIGH NIBBLE	off (0)	on (1)	off (0)	off (0)	0x4
LOW NIBBLE	off (0)	off (0)	off (0)	on (1)	0x1
POST CODE					0x41

Note ...

Under normal operating conditions, the Debug LEDs should not remain lit red during boot-up. They are intended to be used for debugging purposes. In the event that a Debug LED lights up red during boot-up or the CP6004-RA/-RC does not boot, please contact Kontron for further assistance.

2.9.2 DIP Switches SW1, SW2 and SW3 (CP6004-RA)

The CP6004-RA is equipped with two 2-bit DIP switches, SW1 and SW2, and one 4-bit DIP switch, SW3, which enable the board to be configured according to the application requirements. DIP Switch SW1 is used to configure the CompactPCI interface. DIP Switch SW2 is used to configure the PMC interface. DIP Switch SW3 is used for uEFI BIOS boot configuration.

Table 2-7: DIP Switch SW1 Function

SWITCH	FUNCTION
1	PCI frequency of the CompactPCI interface
2	PCI/PCI-X mode of the CompactPCI interface

Table 2-8: DIP Switch SW2 Function

SWITCH	FUNCTION
1	PCI/PCI-X frequency multiplier configuration
2	PCI/PCI-X mode of the PMC interface

Table 2-9: DIP Switch SW3 Function

SWITCH	FUNCTION
1	POST Code indication
2	SPI flash boot selection
3	Reserved
4	Clear uEFI BIOS settings

For further information on the configuration of the DIP switches, refer to Chapter 4.1, “DIP Switches SW1, SW2 and SW3 Configuration”.

2.9.3 Configuration Resistors (CP6004-RC)

The CP6004-RC is equipped with four configuration resistors, R756, R759, R771, and R778, used for uEFI BIOS boot configuration.

Table 2-10: Configuration Resistors

RESISTOR	FUNCTION
R756	POST Code indication
R759	SPI flash boot selection
R771	Reserved
R778	Clear uEFI BIOS settings

2.9.4 USB Interfaces

The CP6004-RA supports six USB 2.0 ports: two on the front I/O, and four on the rear I/O. The CP6004-RC supports four USB 2.0 ports on the rear I/O. On the rear I/O ports it is strongly recommended to use a cable below 3 metres in length for USB 2.0 devices. All six ports are high-speed, full-speed, and low-speed capable.

One USB peripheral may be connected to each port. For connecting more USB devices to the CP6004-RA/-RC than there are available ports, an external USB hub is required.

Note ...

The USB host interfaces can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

2.9.4.1 USB Connectors J6 and J7

The CP6004-RA has two USB 2.0 interfaces implemented as two 4-pin, type A USB connectors on the front panel, J6 and J7, with the following pinout:

Figure 2-1: USB Con. J6 and J7

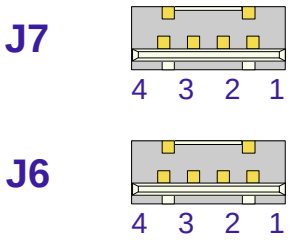


Table 2-11: USB Con. J6 and J7 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	GND	GND	--

2.9.5 Integrated Graphics Controller

The 3rd gen. Intel® Core™ i7 processor includes a highly integrated graphics accelerator delivering high-performance 3D, 2D graphics capabilities with the following features:

- Intel® Dynamic Video Memory Technology
- Intel® Smart 2D Display Technology
- DirectX Video Acceleration (DXVA) support for accelerating video processing (Full AVC/VC1/MPEG2 HW Decode)
- DirectX11, DirectX10.1, DirectX10 and DirectX9 support
- OpenGL 3.0 support
- 2 x HDMI/DVI display interface with 1920 x 1200 pixels @ 60 Hz
- 1 x DisplayPort interface with 2560 x 1600 pixels @ 60 Hz (CP6004-RA)
- 1 x CRT display interface with 2048 x 1536 pixels with 32-bit color @ 75 Hz

2.9.5.1 Graphics Memory Usage

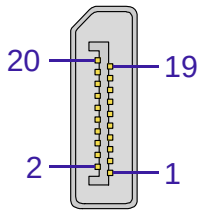
The 3rd gen. Intel® Core™ i7 processor supports Dynamic Video Memory Technology (Intel® DVMT) with up to 512 MB memory. This technology ensures the most efficient use of all available memory for maximum 3D graphics performance. DVMT dynamically responds to application requirements allocating display and texturing memory resources as required.

2.9.5.2 DisplayPort Interface (CP6004-RA)

The CP6004-RA provides one DisplayPort interface implemented as a 20-pin DisplayPort connector, J9, on the front panel. Additionally, the Intel® QM67 chipset provides a DisplayPort interoperability support for CRT / DVI / HDMI displays through a cable adapter.

The following figure illustrates the DisplayPort connector J9.

Figure 2-2: DisplayPort Connector J9



The following table indicates the pinout of the DisplayPort connector J9.

Table 2-12: DisplayPort Connector J9 Pinout

I/O	FUNCTION	SIGNAL	PIN		SIGNAL	FUNCTION	I/O
--	Power 3.3 V, 0.5 A fuse protection	PWR	20	19	RETURN	Return for power	--
I	Hot Plug Detect	HP_DET	18	17	AUX_CH-	Auxiliary Channel-	I/O
--	Signal ground	GND	16	15	AUX_CH+	Auxiliary Channel+	I/O
--	Signal ground	GND	14	13	HDMI_SEL	DP/HDMI/DVI Select	I
--	Signal ground	GND	12	11	ML(3)-	Data Lane3-	O
O	Data Lane3+	ML(3)+	10	9	GND	Signal ground	--
O	Data Lane2-	ML(2)-	8	7	ML(2)+	Data Lane2+	O
--	Signal ground	GND	6	5	ML(1)-	Data Lane1-	O
O	Data Lane1+	ML(1)+	4	3	ML(0)-	Data Lane0-	O
--	Signal ground	GND	2	1	ML(0)+	Data Lane0+	O

2.9.6 COM Ports

The CP6004-RA provides two COM ports, COMA and COMB. COMA is available on the front panel as a serial RS-232, 8-pin, RJ-45 connector, J8, and on the rear I/O simultaneously. COMB is only available as an RS-422/RS-232 interface on the rear I/O.

The CP6004-RC provides two COM ports on the rear I/O, COMA (RS-232) and COMB (RS-422/RS-232).

COMA and COMB are fully compatible with the 16550 controller. The rear I/O COMA port includes a complete set of handshaking and modem control signals. The COMA and COMB ports provide maskable interrupt generation. The data transfer on the COM ports is up to 115.2 kbit/s.

The following figure and table provide pinout information for the serial connector J8 (COMA).

Figure 2-3: Serial Con. J8 (COMA)

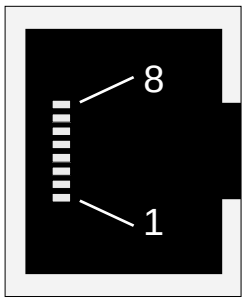


Table 2-13: Serial Con. J8 (COMA) Pinout

PIN	SIGNAL	FUNCTION	I/O
1	RTS	Request to send	O
2	DTR	Data terminal ready	O
3	TXD	Transmit data	O
4	GND	Signal ground	--
5	GND	Signal ground	--
6	RXD	Receive data	I
7	DSR	Data set ready	I
8	CTS	Clear to send	I

Note ...

On the CP6004-RA, COMA can be used either on the front panel or on the rear I/O. It is not possible to use COMA on the front panel and the rear I/O simultaneously.

Note ...

The CP6004-RA/-RC provides two jumpers, JP2 and JP3, used to activate the bus termination for the RS-422/RS-232 (COMB) port.

For further information on the JP2 and JP3 jumpers, refer to Chapter 4.3, Jumper Description.

2.9.7 Gigabit Ethernet

The CP6004-RA board provides five 10Base-T/100Base-TX/1000Base-T Ethernet interfaces. They are based on one Intel® 82580EB Quad Gigabit Ethernet controller and one Intel® 82579LM Gigabit Ethernet controller. The Intel® 82580EB Quad Gigabit Ethernet controller provides four Gigabit Ethernet interfaces, two on the front panel, GbE A and GbE B, configurable to rear I/O (LPc and LPd), and two on the rear I/O, PICMG 2.16 LPa and PICMG 2.16 LPb. The Intel® 82579LM Gigabit Ethernet controller provides one Gigabit Ethernet interface on the front panel, GbE C.

The CP6004-RC board provides four 10Base-T/100Base-TX/1000Base-T Ethernet interfaces. They are based on the Intel® 82580EB Quad Gigabit Ethernet controller which provides four Gigabit Ethernet interfaces on the rear I/O, PICMG 2.16 LPa, PICMG 2.16 LPb, LPc and LPd.

The Boot from LAN feature is supported on the CP6004-RA/-RC.

The following table indicates the Gigabit Ethernet port mapping of the CP6004-RA/-RC.

Table 2-14: Gigabit Ethernet Port Mapping

ETHERNET CONTROLLER	PORT MAPPING
Intel® 82580EB, port 0	Rear I/O port PICMG 2.16 LPb
Intel® 82580EB, port 1	Rear I/O port PICMG 2.16 LPa
Intel® 82580EB, port 2	CP6004-RA: front I/O connector J10 (GbE A) or Rear I/O port LPc CP6004-RC: Rear I/O port LPc
Intel® 82580EB, port 3	CP6004-RA: front I/O connector J11 (GbE B) or Rear I/O port LPd CP6004-RC: Rear I/O port LPd
Intel® 82579LM	CP6004-RA: front I/O connector J12 (GbE C) CP6004-RC: not available

The J10, J11 and J12 Ethernet connectors on the front panel of the CP6004-RA are realized as RJ-45 connectors. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto MDI-X).

Figure 2-4: GbE Connectors J10, J11 and J12

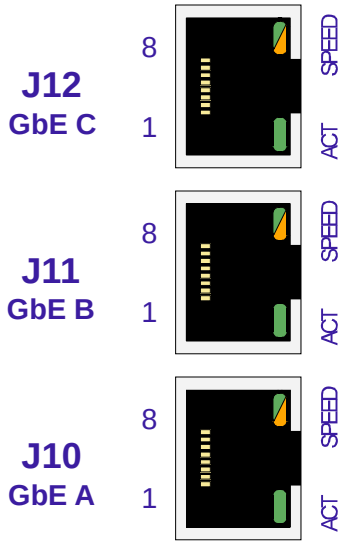


Table 2-15: Pinout of GbE Con. J10, J11 and J12

PIN	MDI / STANDARD ETHERNET CABLE					
	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-	-	I/O	BI_DC+
5	-	-	-	-	I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-	-	I/O	BI_DD+
8	-	-	-	-	I/O	BI_DD-

Ethernet LED Status

ACT (green): This LED monitors network connection and activity. When this LED is lit, it means that a link has been established. The LED blinks when network packets are sent or received through the RJ-45 port. When this LED is not lit, there is no link established.

SPEED (green/orange/off): This LED lights up to indicate a successful 100Base-TX or 1000Base-T connection. When green it indicates a 100Base-TX connection and when orange it indicates a 1000Base-TX connection. When not lit and the ACT LED is active, the connection is operating at 10Base-T.

2.9.8 Serial ATA Interface

The CP6004-RA/-RC provides five Serial ATA (SATA) interfaces with RAID support, one interface is implemented as onboard SATA connector and four SATA interfaces are available only on the rear I/O. The onboard SATA connector, J19, is used for mounting the SATA Flash module. All five SATA ports provide high-performance RAID 0/1/5/10 functionality.

2.9.9 GPI and GPO Signals

The CP6004-RA/-RC provides four general purpose inputs (GPI) and four general purpose outputs (GPO) on the rear I/O CompactPCI interface.

2.9.10 PMC Interface

The CP6004-RA/-RC provides a PMC interface with a dedicated PCI Express-to-PCI-X bridge from Pericom (PI7C9X130). This interface is configurable for either 64-bit/66 MHz PCI or 64-bit/133 MHz PCI-X operation and is compliant with the IEEE 1386.1-2001 specification, which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor. The board provides only 3.3V PMC PCI/PCI-X signaling environment.

A PMC (CP6004-RA) or a CCPMC (CP6004-RC) module can be connected to the CP6004-RA/-RC via the J15 (Jn3), J16 (Jn1), J17 (Jn4) and J18 (Jn2). The J16 (Jn1) and J18 (Jn2) connectors provide the signals for the 32-bit PCI bus. The 64-bit extension for the PMC interface is supported by the J15 (Jn3) connector. User-defined I/O signals are supported on J17 (Jn4) and are connected to the CompactPCI rear I/O connector J4.

The PCI Express-to-PCI-X bridge detects the PCI mode (PCI or PCI-X) and the bus speed (33 MHz, 66 MHz, 100 MHz or 133 MHz) via two PCI control signals: PCIXCAP on J16 (pin 39) and M66EN on J18 (pin 47). The following configurations are supported by the PMC interface.

Table 2-16: PMC PCI/PCI-X Configuration

FREQUENCY	MODE	M66EN J18 (Jn2), PIN 47	PCIXCAP J16 (Jn1), PIN 39	DIP SWITCH SW2 SWITCH 1
33 MHz	PCI	Low	Low	OFF
66 MHz	PCI	High	Low	OFF
66 MHz	PCI-X	--	Pull-down resistor	OFF
100 MHz	PCI-X	--	High	ON
133 MHz	PCI-X	--	High	OFF

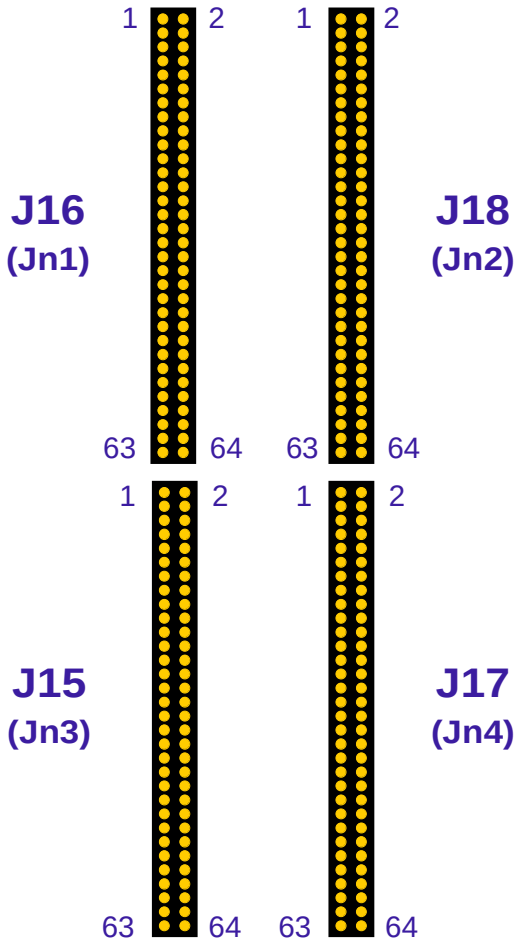
The default configuration of the DIP switch SW2, switch 1, is OFF. If this switch is set to OFF, the PCI/PCI-X interface frequency is 33 MHz, 66 MHz or 133 MHz.

Warning!

DIP switch SW2, switch 1, must be set in accordance with Table 2-16.

Failure to comply with the above will cause unexpected system error due to non-compliance of the PMC subsystem with the PCI-X specification.

Figure 2-5: PMC Connectors J15, J16, J17 and J18



2.9.10.1 PMC Connectors J15, J16, J17 and J18 Pinout

Table 2-17: PMC Connectors J16 and J18 Pinout

J16 (Jn1)				J18 (Jn2)			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
TCK (pull-up)	1	2	-12V	+12V	1	2	TRST# (pull-down)
Ground	3	4	INTA#	TMS (pull-up)	3	4	TDO (NC)
INTB#	5	6	INTC#	TDI (pull-up)	5	6	Ground
BUSMODE1# (NC)	7	8	+5V	Ground	7	8	PCI-RSV (NC)
INTD#	9	10	PCI-RSV (NC)	PCI-RSV (NC)	9	10	PCI-RSV (NC)
Ground	11	12	3V3-AUX (NC)	BUSMODE2# (pull-up)	11	12	+3.3V
CLK	13	14	Ground	RST#	13	14	BUSMODE3# (GND)
Ground	15	16	GNT#	+3.3V	15	16	BUSMODE4# (GND)
REQ#	17	18	+5V	RSV	17	18	Ground
V (I/O)	19	20	AD[31]	AD[30]	19	20	AD[29]
AD[28]	21	22	AD[27]	Ground	21	22	AD[26]
AD[25]	23	24	Ground	AD[24]	23	24	+3.3V
Ground	25	26	C/BE[3]	IDSEL	25	26	AD[23]
AD[22]	27	28	AD[21]	+3.3V	27	28	AD[20]
AD[19]	29	30	+5V	AD[18]	29	30	Ground
V (I/O)	31	32	AD[17]	AD[16]	31	32	C/BE[2]#
FRAME#	33	34	Ground	Ground	33	34	PMC-RSV (NC)
Ground	35	36	IRDY#	TRDY#	35	36	+3.3V
DEVSEL#	37	38	+5V	Ground	37	38	STOP#
PCIXCAP	39	40	LOCK#	PERR#	39	40	Ground
PCI-RSV (NC)	41	42	PCI-RSV (NC)	+3.3V	41	42	SERR#
PAR	43	44	Ground	C/BE[1]#	43	44	Ground
V (I/O)	45	46	AD[15]	AD[14]	45	46	AD[13]
AD[12]	47	48	AD[11]	M66EN	47	48	AD[10]
AD[09]	49	50	+5V	AD[08]	49	50	+3.3V
Ground	51	52	C/BE[0]#	AD[07]	51	52	PMC-RSV (NC)
AD[06]	53	54	AD[05]	+3.3V	53	54	PMC-RSV (NC)
AD[04]	55	56	Ground	PMC-RSV (NC)	55	56	Ground
V (I/O)	57	58	AD[03]	PMC-RSV (NC)	57	58	PMC-RSV (NC)
AD[02]	59	60	AD[01]	Ground	59	60	PMC-RSV (NC)
AD[00]	61	62	+5V	ACK64#	61	62	+3.3V
Ground	63	64	REQ64#	Ground	63	64	PMC-RSV (NC)

Table 2-18: PMC Connectors J15 and J17 Pinout

J15 (Jn3)				J17 (Jn4)			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
PCI-RSV (NC)	1	2	Ground	Rear I/O	1	2	Rear I/O
Ground	3	4	C/BE[7]	Rear I/O	3	4	Rear I/O
C/BE[6]	5	6	C/BE[5]	Rear I/O	5	6	Rear I/O
C/BE[4]	7	8	Ground	Rear I/O	7	8	Rear I/O
V(I/O)	9	10	PAR64	Rear I/O	9	10	Rear I/O
AD[63]	11	12	AD[62]	Rear I/O	11	12	Rear I/O
AD[61]	13	14	Ground	Rear I/O	13	14	Rear I/O
Ground	15	16	AD[60]	Rear I/O	15	16	Rear I/O
AD[59]	17	18	AD[58]	Rear I/O	17	18	Rear I/O
AD[57]	19	20	Ground	Rear I/O	19	20	Rear I/O
V(I/O)	21	22	AD[56]	Rear I/O	21	22	Rear I/O
AD[55]	23	24	AD[54]	Rear I/O	23	24	Rear I/O
AD[53]	25	26	Ground	Rear I/O	25	26	Rear I/O
Ground	27	28	AD[52]	Rear I/O	27	28	Rear I/O
AD[51]	29	30	AD[50]	Rear I/O	29	30	Rear I/O
AD[49]	31	32	Ground	Rear I/O	31	32	Rear I/O
Ground	33	34	AD[48]	Rear I/O	33	34	Rear I/O
AD[47]	35	36	AD[46]	Rear I/O	35	36	Rear I/O
AD[45]	37	38	Ground	Rear I/O	37	38	Rear I/O
V(I/O)	39	40	AD[44]	Rear I/O	39	40	Rear I/O
AD[43]	41	42	AD[42]	Rear I/O	41	42	Rear I/O
AD[41]	43	44	Ground	Rear I/O	43	44	Rear I/O
Ground	45	46	AD[40]	Rear I/O	45	46	Rear I/O
AD[39]	47	48	AD[38]	Rear I/O	47	48	Rear I/O
AD[37]	49	50	Ground	Rear I/O	49	50	Rear I/O
Ground	51	52	AD[36]	Rear I/O	51	52	Rear I/O
AD[35]	53	54	AD[34]	Rear I/O	53	54	Rear I/O
AD[33]	55	56	Ground	Rear I/O	55	56	Rear I/O
V(I/O)	57	58	AD[32]	Rear I/O	57	58	Rear I/O
PCI-RSV (NC)	59	60	PCI-RSV (NC)	Rear I/O	59	60	Rear I/O
PCI-RSV (NC)	61	62	Ground	Rear I/O	61	62	Rear I/O
Ground	63	64	PCI-RSV (NC)	Rear I/O	63	64	Rear I/O

2.9.11 XMC Interface

The CP6004-RA/-RC provides a x8 PCI Express 2.0 XMC interface operating at 5.0 GT/s and compliant with the ANSI/VITA 42.0 and ANSI/VITA 42.3 specifications.

An XMC module (CP6004-RA) or a conductive-cooled XMC module (CP6004-RC) can be connected to the CP6004-RA/-RC via the J14 connector.

User-defined I/O signals are also supported on PMC/XMC slot via the PMC connector J17 (Jn4) and are connected to the CompactPCI rear I/O connector J4.

Figure 2-6: XMC Con. J14

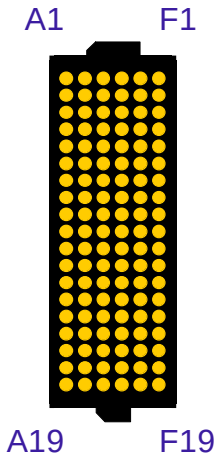


Table 2-19: XMC Connector J14 Pinout

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR
4	GND	GND	TCK	GND	GND	MRSTO#
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR
8	GND	GND	TDI	GND	GND	-12V
9	RFU (NC)	RFU (NC)	RFU (NC)	RFU (NC)	RFU (NC)	VPWR
10	GND	GND	TDO	GND	GND	GA0 (high)
11	PER0p0	PER0n0	MBIST#	PER0p1	PER0n1	VPWR
12	GND	GND	GA1 (low)	GND	GND	MPRE-SENT#
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR
14	GND	GND	GA2 (low)	GND	GND	MSDA
15	PER0p4	PER0n4	RFU (NC)	PER0p5	PER0n5	VPWR
16	GND	GND	MVMRO (NC)	GND	GND	MSCL
17	PER0p6	PER0n6	RFU (NC)	PER0p7	PER0n7	RFU (NC)
18	GND	GND	RFU (NC)	GND	GND	RFU (NC)
19	CLK+0	CLK-0	RFU (NC)	WAKE#	ROOT0#	RFU (NC)

Legend:

RFU Reserved for future use

VPWR 5V power supply for the XMC module

2.9.12 Debug Interface

The CP6004-RA/-RC provides several onboard options for hardware and software debugging, such as:

- Four bicolor Debug LEDs (DLED0..3), which indicate hardware failures, uEFI BIOS POST codes and user-configurable outputs
- A JTAG connector, J20, for programming the onboard logic
- An XDP-SFF, processor JTAG connector, J24, for facilitating the debug and uEFI BIOS software development

2.9.13 CompactPCI Interface

The CP6004-RA/-RC supports a flexibly configurable, hot swap CompactPCI interface. In the system slot the PCI/PCI-X interface is in the transparent mode, and in the peripheral slot the CompactPCI interface is isolated so that it cannot communicate with the CompactPCI bus. This mode is known as "passive mode".

2.9.13.1 Board Functionality when Installed in System Slot

In a system slot, the CompactPCI interface can be either a 64-bit/66 MHz PCI or PCI-X interface via a dedicated PCI Express-to-PCI-X bridge from Pericom (PI7C9X130).

The CP6004-RA/-RC supports up to seven peripheral slots with 33 MHz and up to 4 peripheral slots with 66 MHz through a backplane.

The PCI Express-to-PCI-X bridge detects the PCI mode (PCI or PCI-X) and the bus speed (33 MHz or 66 MHz) via two PCI control signals on J1: PCIXCAP (pin B16) and M66EN (pin D21). The following configurations are supported by the CompactPCI interface.

Table 2-20: CompactPCI PCI/PCI-X Configuration

FREQUENCY	MODE	M66EN J1, PIN D21	PCIXCAP J1, PIN B16	DIP SWITCH SW1 SWITCH 1	DIP SWITCH SW1 SWITCH 2
33 MHz	PCI	Low	Low	OFF	OFF
33 MHz	PCI	--	Low	OFF	ON
66 MHz	PCI	High	Low	OFF	OFF
66 MHz	PCI	High	--	ON	OFF
66 MHz	PCI-X	--	Pull-down resistor	OFF	OFF

Note ...

To support 66 MHz PCI/PCI-X frequency, the CompactPCI signaling voltage (VI/O) must be 3.3 V.

The CP6004-RA/-RC provides automatic voltage detection for the VI/O to switch the PCI frequency to 33 MHz in an 5V environment.

2.9.13.2 Board Functionality when Installed in Peripheral Slot (Passive Mode)

In a peripheral slot, the board receives power but does not communicate on the CompactPCI bus; all CompactPCI signals are isolated. In this configuration, the communication is achieved via the two PICMG 2.16-compliant Gigabit Ethernet ports.

2.9.13.3 Packet Switching Backplane (PICMG 2.16)

The CP6004-RA/-RC supports two Gigabit Ethernet ports on the J3 connector in accordance with the CompactPCI Packet Switching Backplane Specification PICMG 2.16. The two ports are connected in the chassis via the CompactPCI Packet Switching Backplane to the Fabric slots "A" and "B".

The PICMG 2.16 feature can be used in the system slot and in the peripheral slot as well.

2.9.13.4 Hot Swap Support

To ensure that a board may be removed and replaced in a working CompactPCI bus without disturbing the system, the following additional features are required:

- Power ramping
- Precharge
- Hot swap control and status register bits
- Automatic interrupt generation whenever a board is about to be removed or replaced
- A Hot Swap LED on the CP6004-RA is used to indicate that the board may be safely removed.

2.9.13.5 Power Ramping

On the CP6004-RA/-RC a special hot swap controller is used to ramp up the onboard supply voltage. This is done to avoid transients on the +3.3V, +5V, +12V and -12V power supplies from the hot swap system. When the power supply is stable, the hot swap controller generates an onboard reset to put the board into a definite state.

2.9.13.6 Precharge

Precharge is provided on the CP6004-RA/-RC by a resistor on each signal line (PCI bus) connected to a +1V reference voltage.

2.9.13.7 Handle Switch (CP6004-RA)

On a CP6004-RA, a microswitch is situated in the extractor handle. The status of the handle is included in the onboard logic. The microswitch is connected to the onboard connector J13.

2.9.13.8 ENUM# Interrupt

If the board is operated in the system slot, the ENUM signal is an input.

2.9.13.9 Hot Swap LED (CP6004-RA)

The blue HS LED is available only on the CP6004-RA and can be switched on or off by software. It may be used, for example, to indicate that the shutdown process is finished and the board is ready for extraction.

2.9.14 CompactPCI Bus Connector

The complete CompactPCI connector configuration comprises up to five connectors designated as J1 to J5. Their functions are as follows:

- J1/J2: 64-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J3, J4 and J5 have rear I/O interface functionality
- only J4 has rear I/O functionality from the PMC/XMC module

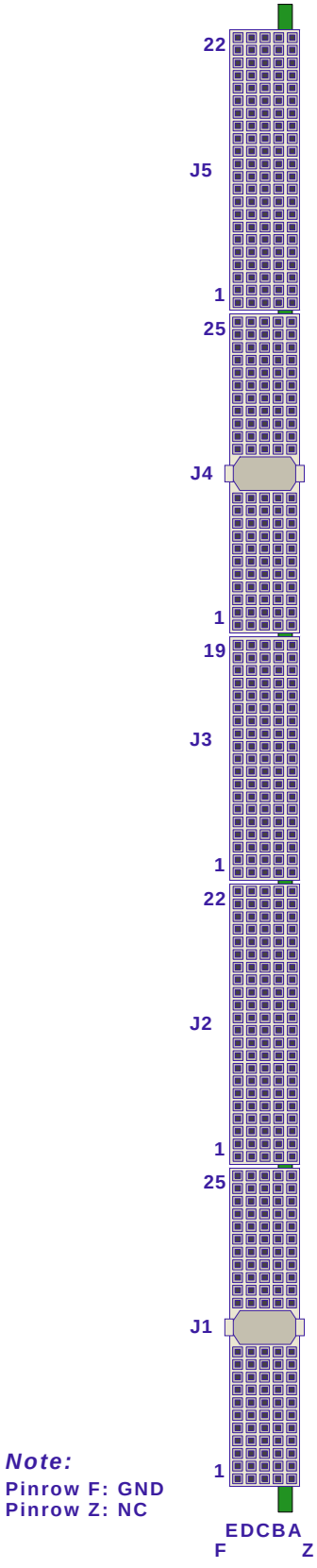
The CP6004-RA/-RC is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

2.9.14.1 CompactPCI Connector Keying

The CompactPCI connectors support guide lugs to ensure a correct polarized mating.

The CP6004-RA/-RC supports universal PCI VI/O signaling voltages with one common termination resistor configuration and includes a PCI VI/O voltage detection circuit. If the PCI VI/O voltage is 5 V, the maximum supported PCI frequency is 33 MHz.

Figure 2-7: CompactPCI Con. J1-J5



2.9.14.2 CompactPCI Connectors J1 and J2 Pinout

The CP6004-RA/-RC is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Table 2-21: CompactPCI Bus Connector J1 System Slot Pinout

PIN	Z	A	B	C	D	E	F
25	NC	5V	REQ64#	ENUM#	3.3V	5V	GND
24	NC	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	NC	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	NC	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	NC	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	NC	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	NC	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	NC	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	NC	3.3V	IPMB SCL	IPMB SDA	GND	PERR#	GND
16	NC	DEVSEL#	PCIXCAP	V(I/O)	STOP#	LOCK#	GND
15	NC	3.3V	FRAME#	IRDY#	BDSEL#	TRDY#	GND
14-12	Key Area						
11	NC	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	NC	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	NC	C/BE[3]#	NC	AD[23]	GND	AD[22]	GND
8	NC	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	NC	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	NC	REQ0#	CPCI_Present#	3.3V	CLK0	AD[31]	GND
5	NC	RSV	RSV	RST#	GND	GNT0#	GND
4	NC	IPMB PWR	Health#	V(I/O)	RSV	RSV	GND
3	NC	INTA#	INTB#	INTC#	5V	INTD#	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	-12V	TRST#	+12V	5V	GND

Table 2-22: CompactPCI Bus Connector J1 Peripheral Slot Pinout

PIN	Z	A	B	C	D	E	F
25	NC	5V	*	*	3.3V	5V	GND
24	NC	*	5V	V(I/O)	*	*	GND
23	NC	3.3V	*	*	5V	*	GND
22	NC	*	GND	3.3V	*	*	GND
21	NC	3.3V	*	*	*	*	GND
20	NC	*	GND	V(I/O)	*	*	GND
19	NC	3.3V	*	*	GND	*	GND
18	NC	*	GND	3.3V	*	*	GND
17	NC	3.3V	IPMB SCL	IPMB SDA	GND	*	GND
16	NC	*	*	V(I/O)	*	*	GND
15	NC	3.3V	*	*	BDSEL#	*	GND
14-12	Key Area						
11	NC	*	*	*	GND	*	GND
10	NC	*	GND	3.3V	*	*	GND
9	NC	*	NC	*	GND	*	GND
8	NC	*	GND	V(I/O)	*	*	GND
7	NC	*	*	*	GND	*	GND
6	NC	*	CPCI_Present#	3.3V	*	*	GND
5	NC	RSV	RSV	RST#**	GND	*	GND
4	NC	IPMB PWR	Healthy#	V(I/O)	RSV	RSV	GND
3	NC	*	*	*	5V	*	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	-12V	TRST#	+12V	5V	GND

Note ...

A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP6004-RA/-RC is inserted in a peripheral slot.

** When the CP6004-RA/-RC is inserted in a peripheral slot, the function of the RST# signal can be enabled or disabled.

Table 2-23: 64-bit CompactPCI Bus Connector J2 System Slot Pinout

PIN	Z	A	B	C	D	E	F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	CLK6	GND	RSV	RSV	RSV	GND
20	NC	CLK5	GND	RSV	GND	RSV	GND
19	NC	GND	GND	IPMB2_SDA	IPMB2_SCL	IPMB2_Alert	GND
18	NC	RSV	RSV	RSV	GND	RSV	GND
17	NC	RSV	GND	PRST#	REQ6#	GNT6#	GND
16	NC	RSV	RSV	DEG#	GND	RSV	GND
15	NC	RSV	GND	FAL#	REQ5#	GNT5#	GND
14	NC	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	NC	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	NC	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	NC	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	NC	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	NC	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	NC	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	NC	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	NC	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	NC	C/BE[5]#	NC	V(I/O)	C/BE[4]#	PAR64	GND
4	NC	V(I/O)	RSV	C/BE[7]#	GND	C/BE[6]#	GND
3	NC	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	NC	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	NC	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Table 2-24: 64-bit CompactPCI Bus Connector J2 Peripheral Slot Pinout

PIN	Z	A	B	C	D	E	F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	*	GND	RSV	RSV	RSV	GND
20	NC	*	GND	RSV	GND	RSV	GND
19	NC	GND	GND	IPMB2_SDA	IPMB2_SCL	IPMB2_Alert	GND
18	NC	RSV	RSV	RSV	GND	RSV	GND
17	NC	RSV	GND	*	*	*	GND
16	NC	RSV	RSV	DEG#	GND	RSV	GND
15	NC	RSV	GND	FAL#	*	*	GND
14	NC	*	*	*	GND	*	GND
13	NC	*	GND	V(I/O)	*	*	GND
12	NC	*	*	*	GND	*	GND
11	NC	*	GND	V(I/O)	*	*	GND
10	NC	*	*	*	GND	*	GND
9	NC	*	GND	V(I/O)	*	*	GND
8	NC	*	*	*	GND	*	GND
7	NC	*	GND	V(I/O)	*	*	GND
6	NC	*	*	*	GND	*	GND
5	NC	*	NC	V(I/O)	*	*	GND
4	NC	V(I/O)	RSV	*	GND	*	GND
3	NC	*	GND	*	*	*	GND
2	NC	*	*	SYSEN#	*	*	GND
1	NC	*	GND	*	*	*	GND

Note ...

A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP6004-RA/-RC is inserted in a peripheral slot.

2.9.14.3 CompactPCI Rear I/O Connectors J3-J5 and Pinout

The CP6004-RA/-RC board provides optional rear I/O connectivity for peripherals. Standard PC interfaces are implemented and assigned to the front panel and to the rear I/O connectors J3, and J5. The J4 connector serves for providing rear I/O interfacing for the PMC module.

When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus, the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system rear I/O feature a special backplane is necessary. The CP6004-RA/-RC with rear I/O is compatible with all standard 6U CompactPCI passive backplanes with rear I/O support.

The CP6004-RA/-RC conducts all I/O signals through the rear I/O connectors J3, J4 and J5.

Table 2-25: CompactPCI Rear I/O Connector J3 Pinout

PIN	Z	A	B	C	D	E	F
19	NC	RIO_5V	RIO_5V	RIO_3.3V	RIO_+12V	RIO_-12V	GND
18	NC	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
17	NC	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	NC	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	GND
15	NC	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-	GND
14	NC	LPa:LINK	LPb:LINK	LPab:CT1	LPc:LINK	FAN:SENSE2	GND
13	NC	LPa:ACT	LPb:ACT	LPcd:CT1	LPc:ACT	FAN:SENSE1	GND
12	NC	LPc:DA+	LPc:DA-	GND	LPc:DC+	LPc:DC-	GND
11	NC	LPc:DB+	LPc:DB-	GND	LPc:DD+	LPc:DD-	GND
10	NC	USB1:VCC	USB0:VCC	GND	USB3:VCC	USB2:VCC	GND
9	NC	USB1:D-	USB1:D+	GND	USB3:D-	USB3:D+	GND
8	NC	USB0:D-	USB0:D+	GND	USB2:D-	USB2:D+	GND
7	NC	RIO_3.3V	GPI0	GPI1	GPI2	SPEAKER	GND
6	NC	VGA:RED	VGA:GREEN	VGA:SDA	DEBUG:CLK	DEBUG:DAT	GND
5	NC	VGA:BLUE	VGA:HSYNC	VGA:VSYNC	VGA:SCL	LPd:DC+	GND
4	NC	LPd:DA+	LPd:DA-	SPB:TX-/TX	SPB:TX+/RTS	LPd:DC-	GND
3	NC	LPd:DB+	LPd:DB-	SPB:RX-/CTS	SPB:RX+/RX	LPd:DD+	GND
2	NC	SPA:RI	SPA:DTR	SPA:CTS	SPA:TX	LPd:DD-	GND
1	NC	SPA:RTS	SPA:RX	SPA:DSR	SPA:DCD	RIO_ID1	GND

Warning!

The RIO_XXX signals are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

The following table describes the signals of the J3 connector.

Table 2-26: CompactPCI Rear I/O Connector J3 Signals

SIGNAL	DESCRIPTION
SPA	COMA signaling (RS-232)
SPB	COMB signaling (RS-422/RS-232)
VGA	Graphic signaling
USB0 to USB3	USB Port signaling
SPEAKER	Standard PC speaker
FAN	Fan speed sensoring
DEBUG	Debug output
LPa	Rear I/O Link Port A (PICMG 2.16)
LPb	Rear I/O Link Port B (PICMG 2.16)
LPab	Center tap voltage for LPa and LPb
LPc	Rear I/O Link Port C
LPd	Rear I/O Link Port D
LPcd	Center tap voltage for LPc and LPd
GPIO	General purpose digital input/output; 3.3V only

Note ...

On the CP6004-RA, COMA can be used either on the front panel or on the rear I/O. It is not possible to use COMA on the front panel and on the rear I/O simultaneously.

Table 2-27: CompactPCI Rear I/O Connector J4 Pinout

PIN	Z	A	B	C	D	E	F
25	NC	PIM:1	PIM:3	GND	PIM:2	PIM:4	GND
24	NC	PIM:5	PIM:7	GND	PIM:6	PIM:8	GND
23	NC	NC	RIO_5V	GND	NC	RIO_3.3V	GND
22	NC	PIM:9	PIM:11	GND	PIM:10	PIM:12	GND
21	NC	PIM:13	PIM:15	GND	PIM:14	PIM:16	GND
20	NC	GND	GND	GND	GND	GND	GND
19	NC	PIM:17	PIM:19	GND	PIM:18	PIM:20	GND
18	NC	PIM:21	PIM:23	GND	PIM:22	PIM:24	GND
17	NC	GND	GND	GND	GND	GND	GND
16	NC	PIM:25	PIM:27	GND	PIM:26	PIM:28	GND
15	NC	PIM:29	PIM:31	GND	PIM:30	PIM:32	GND
14 -12	Key Area						
11	NC	PIM:33	PIM:35	GND	PIM:34	PIM:36	GND
10	NC	PIM:37	PIM:39	GND	PIM:38	PIM:40	GND
9	NC	GND	GND	GND	GND	GND	GND
8	NC	PIM:41	PIM:43	GND	PIM:42	PIM:44	GND
7	NC	PIM:45	PIM:47	GND	PIM:46	PIM:48	GND
6	NC	GND	GND	GND	GND	GND	GND
5	NC	PIM:49	PIM:51	GND	PIM:50	PIM:52	GND
4	NC	PIM:53	PIM:55	GND	PIM:54	PIM:56	GND
3	NC	GND	GND	GND	GND	GND	GND
2	NC	PIM:57	PIM:59	GND	PIM:58	PIM:60	GND
1	NC	PIM:61	PIM:63	GND	PIM:62	PIM:64	GND

The signals from the J4 CompactPCI rear I/O connector are routed to the J17 (Jn4) PMC connector in such a way that they can only be used for low-speed signals.

Table 2-28: CompactPCI Rear I/O Connector J5 Pinout

PIN	Z	A	B	C	D	E	F
22	NC	GPI3	PWM1:OUT	GND	PWM2:OUT	BATT (3.0V)	GND
21	NC	HDA:SYNC	HDA:RST#	GND	HDA:SDOUT	SYS_WP#	GND
20	NC	GPO0	HDA:SDIN1	GND	GPO1	HDA:SDIN2	GND
19	NC	GND	GND	GND	HDA:SDIN0	HDA:BITCLK	GND
18	NC	HDMI2:D0+	HDMI2:D0-	GND	GND	GND	GND
17	NC	HDMI2:D2+	HDMI2:D2-	GND	HDMI2:D1+	HDMI2:D1-	GND
16	NC	RSV	HDMI2:HPDET	GND	GPO2	GPO3	GND
15	NC	HDMI2:CLK+	HDMI2:CLK-	GND	HDMI2:SDA	HDMI2:SDC	GND
14	NC	GND	GND	GND	GND	GND	GND
13	NC	HDMI1:D0+	HDMI1:D0-	GND	HDMI1:D1+	HDMI1:D1-	GND
12	NC	HDMI1:D2+	HDMI1:D2-	GND	RSV	RSV	GND
11	NC	RSV	HDMI1:HPDET	GND	HDMI1:SDA	HDMI1:SDC	GND
10	NC	HDMI1:CLK+	HDMI1:CLK-	GND	RSV	RSV	GND
9	NC	GND	GND	GND	GND	GND	GND
8	NC	SATA3:TX+	SATA3:TX-	GND	SATA3:RX+	SATA3:RX-	GND
7	NC	GND	GND	GND	GND	GND	GND
6	NC	SATA2:TX+	SATA2:TX-	GND	SATA2:RX+	SATA2:RX-	GND
5	NC	GND	GND	GND	GND	GND	GND
4	NC	SATA1:TX+	SATA1:TX-	GND	SATA1:RX+	SATA1:RX-	GND
3	NC	GND	GND	GND	GND	GND	GND
2	NC	SATA0:TX+	SATA0:TX-	GND	SATA0:RX+	SATA0:RX-	GND
1	NC	GND	GND	GND	GND	GND	GND

The following table describes the signals of the J5 connector.

Table 2-29: CompactPCI Rear I/O Connector J5 Signals

SIGNAL	DESCRIPTION
SATA0..3	SATA Port 0..3 Signaling
HDMI1	HDMI signaling
HDMI2	HDMI signaling
HDA	High-definition audio signaling
PWM	Pulse width modulation output for fan
GPIO	General purpose digital input/output; 3.3 V only
SYS_WP#	System write protection for non-volatile memory devices; 3.3 V only
BATT (3.0V)	Back-up power input for RTC and CMOS RAM; 3 V only

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Chapter 3

Installation

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3. Installation

The CP6004-RA/-RC has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the CP6004-RA/-RC. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

Caution!

If your board type is not specifically qualified as being hot swap capable, switch off the CompactPCI system power before installing the board in a free CompactPCI slot. Failure to do so could endanger your life or health and may damage your board or system.

Note...

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.

ESD Equipment!

This CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

3.2 CP6004-RA Installation

3.2.1 CP6004-RA Initial Installation Procedures

The following procedures are applicable only for the initial installation of the CP6004-RA in a system. Procedures for standard removal and hot swap operations are found in their respective chapters.

To perform an initial installation of the CP6004-RA in a system proceed as follows:

1. Ensure that the safety requirements indicated Chapter 3.1 are observed.

Warning!

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the CP6004-RA refer to Chapter 4. For the installation of CP6004-RA specific peripheral devices and rear I/O devices refer to the appropriate sections in Chapter 3.

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6004-RA/-RC nor other system boards are physically damaged by the application of these procedures.

3. To install the CP6004-RA perform the following:
   1. Ensure that no power is applied to the system before proceeding.

Warning!

Even though power may be removed from the system, the CP6004-RA front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

Warning!

When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
3. Using both ejector handles, engage the board with the backplane. When the ejector handles are locked, the board is engaged.
4. Fasten the two front panel retaining screws.
5. Connect all external interfacing cables to the board as required.
6. Ensure that the board and all required interfacing cables are properly secured.

The CP6004-RA is now ready for initial operation. Except for the uEFI BIOS, at this point there is no other software installed. For software installation and further operation of the CP6004-RA, refer to the appropriate CP6004-RA software (uEFI BIOS, BSP, OS), application, and system documentation.

3.2.2 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6004-RA nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.

Warning!

Even though power may be removed from the system, the CP6004-RA front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.
7. Dispose of the board as required.

3.2.3 Hot Swap Procedures

The CP6004-RA is designed for hot swap operation. When installed in the system slot, it is capable of supporting peripheral board hot swapping. When installed in a peripheral slot, its hot swap capabilities depend on the type of backplane in use and the system controller's capabilities. The reason for this being that communications with the system controller requires either front panel Ethernet I/O or use of a packet switching backplane. In any event, hot swap is also a function of the application running on the CP6004-RA.

3.2.3.1 System Master Hot Swap

Hot swapping of the CP6004-RA itself when used as the system controller is possible, but will result in any event in a cold start of the CP6004-RA and consequently a reinitialization of all peripheral boards. Exactly what transpires in such a situation is a function of the application and is not addressed in this manual. The user must refer to the appropriate application documentation for applicable procedures for this case. In any event, the safety requirements above must be observed.

3.2.3.2 Peripheral Hot Swap Procedure

This procedure assumes that the system supports hot swapping, and that the replacement for the board to be hot swapped is configured hardware- and software-wise for operation in the application.

To hot swap the CP6004-RA proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6004-RA nor other system boards are physically damaged by the application of these procedures.

2. Unlock both board ejection handles ensuring that the bottom handle has activated the hot swap switch (this occurs with a very small amount of movement of the handle).

Note ...

What transpires at this time is a function of the application. If hot swap is supported by the application, then the blue HS LED should light up after a short time period. This indicates that the system has recognized that the CP6004-RA is to be hot swapped and now indicates to the operator that hot swapping of the CP6004-RA may proceed.

If the blue HS LED does not light up after a short time period, either the system does not support hot swap or a malfunction has occurred. In this event, the application is responsible for handling this situation and must provide the operator with appropriate guidance to remedy the situation.

3. After approximately 1 to 15 seconds, the blue HS LED should light up. If the LED lights up, proceed with the next step of this procedure. If the LED does not light up, refer to the appropriate application documentation for further action.

4. Disconnect any interfacing cables that may be connected to the board.

Warning!

The CP6004-RA front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

5. Unscrew the front panel retaining screws.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

6. Using the ejector handles, disengage the board from the backplane and carefully remove it from the system.
7. Dispose of the “old” board as required observing the safety requirements indicated in Chapter 3.1.
8. Obtain the replacement CP6004-RA board.

Warning!

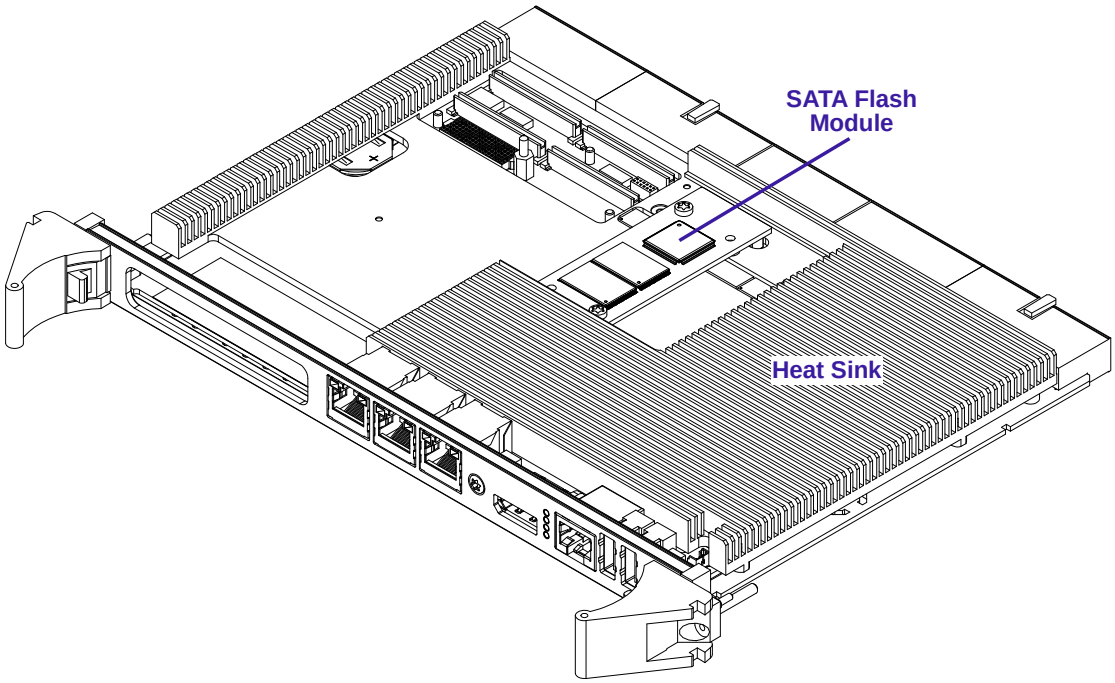
When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

9. Carefully insert the “new” board into the “old” board slot until it makes contact with the backplane connectors.
10. Using both ejector handles, engage the board with the backplane. When the ejector handles are locked, the board is engaged.
11. Fasten the front panel retaining screws.
12. Connect all required interfacing cables to the board.
    Hot swap of the CP6004-RA is now complete.

3.2.4 Installation of CP6004-RA Peripheral Devices

The CP6004-RA is designed to accommodate various peripheral devices, such as USB devices, PMC/XMC modules, rear I/O devices, a SATA Flash module, etc. The following figure shows the placement of the SATA Flash module on the CP6004-RA.

Figure 3-1: Connecting a Peripheral Device to the CP6004-RA



The following chapters provide information regarding installation aspects of peripheral devices.

3.2.4.1 USB Device Installation

The CP6004-RA supports all USB Plug and Play computer peripherals (e.g. keyboard, mouse, printer, etc.).

Note ...

All USB devices may be connected or removed while the host or other peripherals are powered up.

3.2.4.2 SATA Flash Module Installation

A SATA Flash module may be connected to the CP6004-RA via the onboard connector, J19.

This optionally available module must be physically installed on the CP6004-RA prior to installation of the CP6004-RA in a system.

During installation it is necessary to ensure that the SATA Flash module is properly seated in the onboard connector J19, i.e. the pins are aligned correctly and not bent.

Note ...

Only qualified SATA Flash modules from Kontron are authorized for use with the CP6004-RA. Failure to comply with the above will void the warranty and may result in damage to the board or the system.

3.2.5 PMC/XMC Module Installation

The CP6004-RA supports the installation of a PMC module via the connectors J15 to J18 or an XMC module via the connector J14.

For the initial installation and standard removal of all PMC/XMC modules, refer to the documentation provided with the module.

Prior to installation or removal, ensure that the safety requirements indicated in Chapter 3.1 of this user guide are observed. Particular attention must be paid to the warning regarding the heat sink!

3.2.5.1 Rear I/O Device Installation

For physical installation of rear I/O devices, refer to the documentation provided with the device itself.

Note ...

COMA can be used either on the front panel or on rear I/O. It is not possible to use COMA on the front panel and the rear I/O simultaneously.

3.2.6 Battery Replacement

The CP6004-RA is provided with a 3.0 V “coin cell” lithium battery of type CR2025 approved by UL. The battery is used for RTC data storage.

Warning!

Use only batteries of type CR2025 approved by UL.

Replacement of the battery by an incorrect type may result in explosion.

To replace the battery, proceed as follows:

- Turn off power.
- Remove the battery.
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

Note ...

The user must be aware that the battery’s operational temperature range is less than the CP6004-RA’s storage temperature range.

For exact range information, refer to the battery manufacturer’s specifications.

Note ...

Care must be taken to ensure that the battery is correctly replaced.

Dispose of used batteries according to the manufacturer’s instructions.

The typical life expectancy of a 170 mAh battery (CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.
To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 4 - 5 years.

3.3 CP6004-RC Installation

3.3.1 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the CP6004-RC in a system. Procedures for standard removal and hot swap operations of the CP6004-RC are found in their respective chapters.

To perform an initial installation of the CP6004-RC in a system, proceed as follows:

1. Ensure that the safety requirements indicated Chapter 3.1 are observed.

Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the CP6004-RC refer to Chapter 4. For the installation of CP6004-RC specific peripheral devices and rear I/O devices refer to the appropriate sections in Chapter 3.

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6004-RC nor other system boards are physically damaged by the application of these procedures.

3. To install the CP6004-RC perform the following:
    1. Ensure that no power is applied to the system before proceeding.
    2. Ensure that both extractor handle retaining screws are properly fastened.
    3. Before inserting the board in the system chassis, ensure that both the top and bottom wedge locks are fully relaxed.

       To relax the wedge lock, turn the wedge lock's screw counter-clockwise using a 2.5 mm hex key until the screw is against the stop. The screw should turn lightly. If, when turning the screw, perceptible resistance is encountered, it is at the stop. Do not apply more force than necessary.
    4. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.

Note ...

In rugged systems, the slot tolerances are very narrow. In the event that the board jams during insertion, remove it and ensure that both wedge locks are fully relaxed before proceeding with insertion. The board should allow insertion to the point of contact with the backplane connectors without applying undo force.

5. Using both hands, steadily apply enough force on the top and bottom of the front surface of the board to engage it with the backplane.

Note ...

The chassis of rugged systems do not necessarily provide an objective means of determining when the board is properly seated in the backplane. During insertion it is possible however to sense when the board “gives way” and seats into the connector. At this point, the application of more force does not result in further movement of the board.

In the event that more boards are installed in a chassis, it is possible to compare the board’s front plane with the other boards. If they are all even with one another, then they are all properly seated.

If in doubt that the board is properly seated, remove it and repeat steps 3 and 4 above.

6. Complete securing of the board by expanding the top and bottom wedge locks. This is done using a torque screwdriver with a 2.5 mm hex socket head. The recommended torque value is 0.8 N-m (115 oz-in).

   The CP6004-RC is now ready for initial operation. Except for the BIOS, at this point there is no other software installed. For software installation and further operation of the CP6004-RC, refer to appropriate CP6004-RC software (BIOS, BSP, OS), application, and system documentation.

3.3.2 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must not only be paid to the warning regarding the heat sink, but the user must also be aware that the surrounding rugged system components and chassis can get very hot!

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6004-RC nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Unfasten both extractor handle retaining screws.
4. Ensure that both the top and bottom wedge locks are fully relaxed.

To relax the wedge lock, turn the wedge lock's screw counter-clockwise using a 2.5 mm hex key until the screw is against the stop.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot - danger of burns. In addition, the surrounding rugged system components and chassis may be very hot.

If required, use protective gloves to handle the CP6004-RC when removing it.

5. Disengage the board from the backplane using the ejector handles as required until the board is disengaged from the backplane.
6. After disengaging the board from the backplane, pull the board out of the slot.
7. Ensure that both extractor handle retaining screws are properly fastened.
8. Dispose of the board as required.

3.3.3 Hot Swap Procedures

The CP6004-RC is designed for hot swap operation. When installed in the system slot it is capable of supporting peripheral board hot swapping. When installed in a peripheral slot, its hot swap capabilities depend on the type of backplane in use and the system controller's capabilities. The reason for this being that communications with the system controller requires either use of a packet switching backplane or via IPMI. In any event, hot swap is also a function of the application running on the CP6004-RC.

Note ...

The hot swap functionality - hot swap LED and extractor handle hot swap micro-switch - are not available on the CP6004-RC. Therefore, implementations requiring hot swap functionality must provide other means to support these requirements. For example, provision of chassis external LEDs or switches, or other appropriate operator accessible functionality. In any event, application software including IPMI software must provide hot swap support.

3.3.3.1 System Master Hot Swap

Hot swapping of the CP6004-RC itself when used as the system controller is possible, but will result in any event in a cold start of the CP6004-RC and consequently a reinitialization of all peripheral boards actively interfacing with the CPCI bus. Exactly what transpires in such a situation is a function of the application and is not addressed in this manual. The user must refer to appropriate application documentation for applicable procedures for this case. In any event, the safety requirements above must be observed.

3.3.3.2 CP6004-RC Hot Swap Procedure

This procedure assumes that the system supports hot swapping, and that the replacement for the board to be hot swapped is configured hardware and software wise for operation in the application.

To hot swap the CP6004-RC proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must not only be paid to the warning regarding the heat sink, but the user must also be aware that the surrounding rugged system components and chassis can get very hot!

   Warning!

   Care must be taken when applying the procedures below to ensure that neither the CP6004-RC nor other system boards are physically damaged by the application of these procedures.

2. Ensure that the CP6004-RC is ready for hot-swapping.

   Note ...

   What transpires at this time is a function of the application. In any event, some means of indication or notice must be made available that the CP6004-RC requires and is ready to be hot-swapped.

   Do not proceed with the remaining procedures until it is verified that a hot-swap may be performed.

3. Unfasten both extractor handle retaining screws.
4. Ensure that both the top and bottom wedge locks are fully relaxed.

   To relax the wedge lock, turn the wedge lock's screw counter-clockwise using a 2.5 mm hex key until the screw is against the stop.

   Warning!

   Due care should be exercised when handling the board due to the fact that the heat spreader can get very hot - danger of burns. In addition, the surrounding rugged system components and chassis may be very hot.

   If required, use protective gloves to handle the CP6004-RC when removing it.

5. Disengage the board from the backplane using the ejector handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.
7. Ensure that both extractor handle retaining screws are properly fastened.
8. Dispose of the "old" board as required observing the safety requirements indicated in Chapter 3.1.
9. Obtain the replacement CP6004-RC board.
10. Before inserting the board in the system chassis, ensure that both the top and bottom wedge locks are fully relaxed.

    To relax the wedge lock, turn the wedge lock's screw counter-clockwise using a 2.5 mm hex key until the screw is against the stop. The screw should turn lightly. If, when turning the screw, perceptible resistance is encountered, it is at the stop. Do not apply more force than necessary.

11. Ensure that both extractor handle retaining screws are properly fastened.

12. Carefully insert the “new” board into the “old” board’s slot until it makes contact with the backplane connectors.

Note ...

In rugged systems, the slot tolerances are very narrow. In the event that the board jams during insertion, remove it and ensure that both wedge locks are fully relaxed before proceeding with insertion. The board should allow insertion to the point of contact with the backplane connectors without applying undo force.

13. Using both hands, steadily apply enough force on the top and bottom of the front surface of the board to engage it with the backplane.

Note ...

The chassis of rugged systems do not necessarily provide an objective means of determining when the board is properly seated in the backplane. During insertion it is possible however to sense when the board “gives way” and seats into the connector. At this point, the application of more force does not result in further movement of the board.

In the event that more boards are installed in a chassis, it is possible to compare the board’s front plane with the other boards. If they are all even with one another, then they are all properly seated.

If in doubt that the board is properly seated, remove it and repeat steps 3 and 4 above.

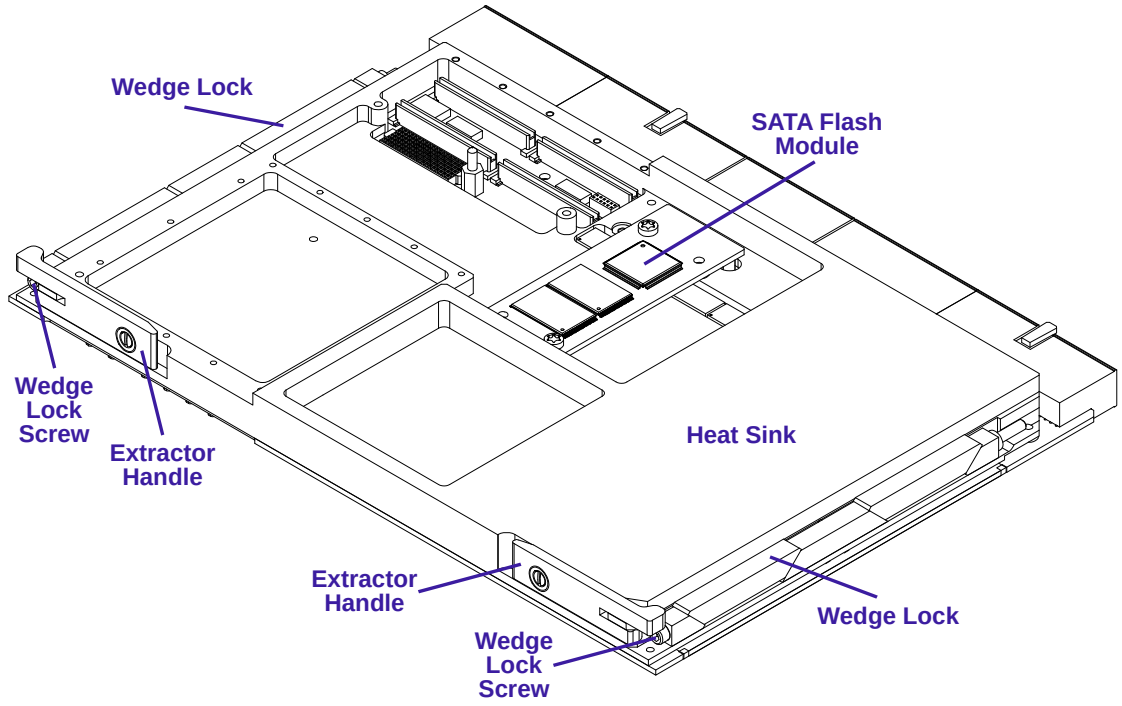
14. Complete securing of the board by expanding the top and bottom wedge locks. This is done using a torque screwdriver with a 2.5 mm hex socket head. The recommended torque value is 0.8 N-m (115 oz-in). Hot swap of the CP6004-RC is now complete.

Exactly what should transpire after the hot swap of the CP6004-RC is a function of the application and is not addressed in this user guide. The user must refer to appropriate application documentation for further information or applicable procedures.

3.3.4 Installation of CP6004-RC Peripheral Devices

The CP6004-RC is designed to accommodate various peripheral devices, such as USB devices, CCPMC/conduction-cooled XMC modules, rear I/O devices, a SATA Flash module, etc.The following figure shows the placement of the SATA Flash module on the CP6004-RC.

Figure 3-2: Connecting a Peripheral Device to the CP6004-RC



The following chapters provide information regarding installation aspects of peripheral devices.

3.3.4.1 USB Device Installation

The CP6004-RC supports all USB Plug and Play computer peripherals (e.g. keyboard, mouse, printer, etc.). Support for these devices is only provided via rear I/O.

Note ...

All USB devices may be connected or removed while the host or other peripherals are powered up.

3.3.4.2 Rear I/O Device Installation

For physical installation of rear I/O devices, refer to the documentation provided with the device itself.

3.3.5 CCPMC/Conduction-Cooled XMC Module Installation

The CP6004-RA supports the installation of a CCPMC module via the connectors J15 to J18 or a conduction-cooled XMC module via the connector J14.

For the initial installation and standard removal of all CCPMC/conduction-cooled XMC modules, refer to the documentation provided with the module.

Prior to installation or removal, ensure that the safety requirements indicated in Chapter 3.1 of this user guide are observed. Particular attention must be paid to the warning regarding the heat sink!

3.4 Software Installation

Installation of an operating system is a function of the OS software and is not addressed in this manual. Refer to the appropriate OS software documentation for installation.

Note ...

Users working with pre-configured operating system installation images for plug-and-play-compliant operating systems, such as Windows®, must take into consideration that the stepping and revision ID of the chipset and/or other on-board PCI devices may change. Thus, a re-configuration of the operating system installation image deployed for a previous chipset stepping or revision ID is in most cases required. The corresponding operating system will detect new devices according to the plug-and-play configuration rules.

Chapter 4

Configuration

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4. Configuration

4.1 DIP Switches SW1, SW2 and SW3 Configuration (CP6004-RA)

The CP6004-RA is equipped with two 2-bit DIP switches, SW1 and SW2, and one 4-bit DIP switch, SW3, which enable the board to be configured according to the application requirements. DIP Switch SW1 is used to configure the CompactPCI interface. DIP Switch SW2 is used to configure the PMC interface. DIP Switch SW3 is used for uEFI BIOS boot configuration.

Figure 4-1: DIP Switches SW1, SW2 and SW3 (CP6004-RA)

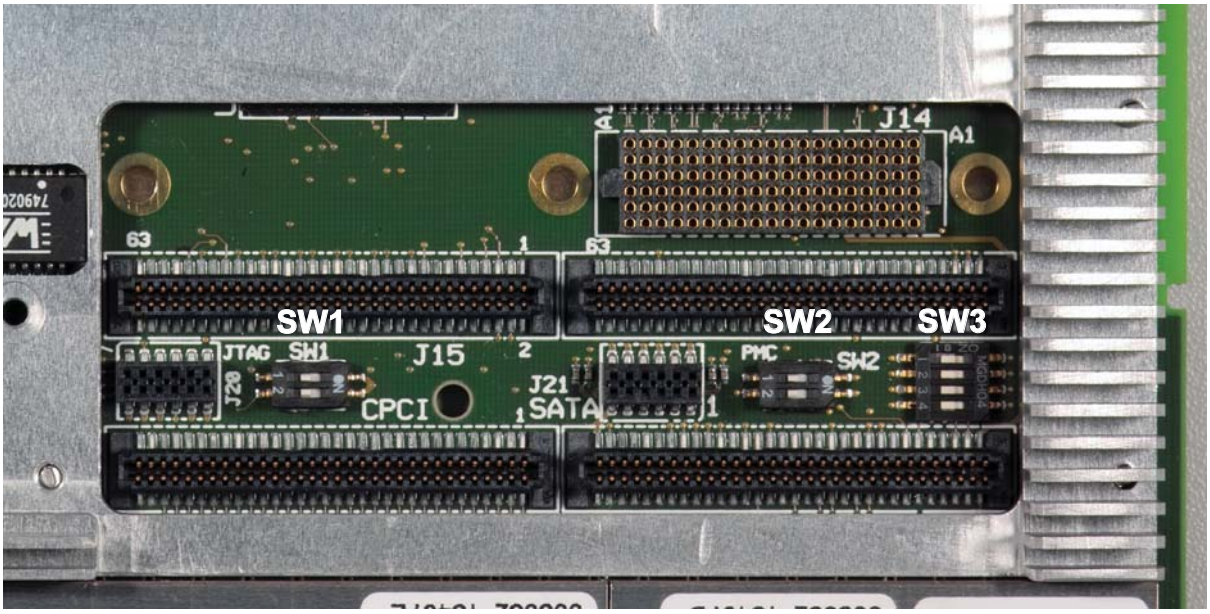

Table 4-1: DIP Switch SW1 for CompactPCI Interface Configuration

SWITCH	SETTING	DESCRIPTION
1	*OFF*	*PCI 33 MHz/66 MHz auto detection via the CompactPCI backplane*
	ON	PCI frequency configured to 33 MHz
2	*OFF*	*PCI/PCI-X mode auto detection via the CompactPCI backplane*
	ON	CP6004-RA/-RC configured to PCI mode

Table 4-2: DIP Switch SW2 for PMC Interface Configuration

SWITCH	SETTING	DESCRIPTION
1	*OFF*	*PCI/PCI-X frequency multiplier configured to 33 MHz*
	ON	PCI/PCI-X frequency multiplier configured to 25 MHz
2	*OFF*	*PCI/PCI-X mode auto detection via the PMC module*
	ON	PMC interface configured to PCI mode

The default settings of the DIP switches SW1 and SW2 are indicated by using italic bold.

Table 4-3: DIP Switch SW3 for Boot Configuration

SWITCH	SETTING	DESCRIPTION
1	*OFF*	*Boot-up with POST Code indication on the Debug LEDs*
	ON	Boot-up with no POST Code indication on the Debug LEDs
2	*OFF*	*Boot from the standard SPI boot flash*
	ON	Boot from the recovery SPI boot flash
3	*OFF*	Reserved
	ON	
4	*OFF*	*Boot using the currently saved uEFI BIOS settings*
	ON	Clear the uEFI BIOS settings and use the default values

The default settings of the DIP switch SW3 are indicated by using italic bold.

Note ...

If the DIP switch SW3, switch 2, is set to ON, the SPI boot flash selection cannot be overwritten by the IPMI controller.

To clear the uEFI BIOS settings, proceed as follows:

1. Set the DIP Switch SW3, switch 4, to the ON position.
2. Apply power to the system.
3. After 30 seconds, remove power from the system.
   During this time period of approx. 30 seconds, no messages are displayed.
4. Set the DIP Switch SW3, switch 4 to the OFF position.

4.2 Configuration Resistors (CP6004-RC)

The CP6004-RC is equipped with four configuration resistors, R756, R759, R771, and R778, used for uEFI BIOS boot configuration.

Figure 4-2: Configuration Resistors (CP6004-RC)

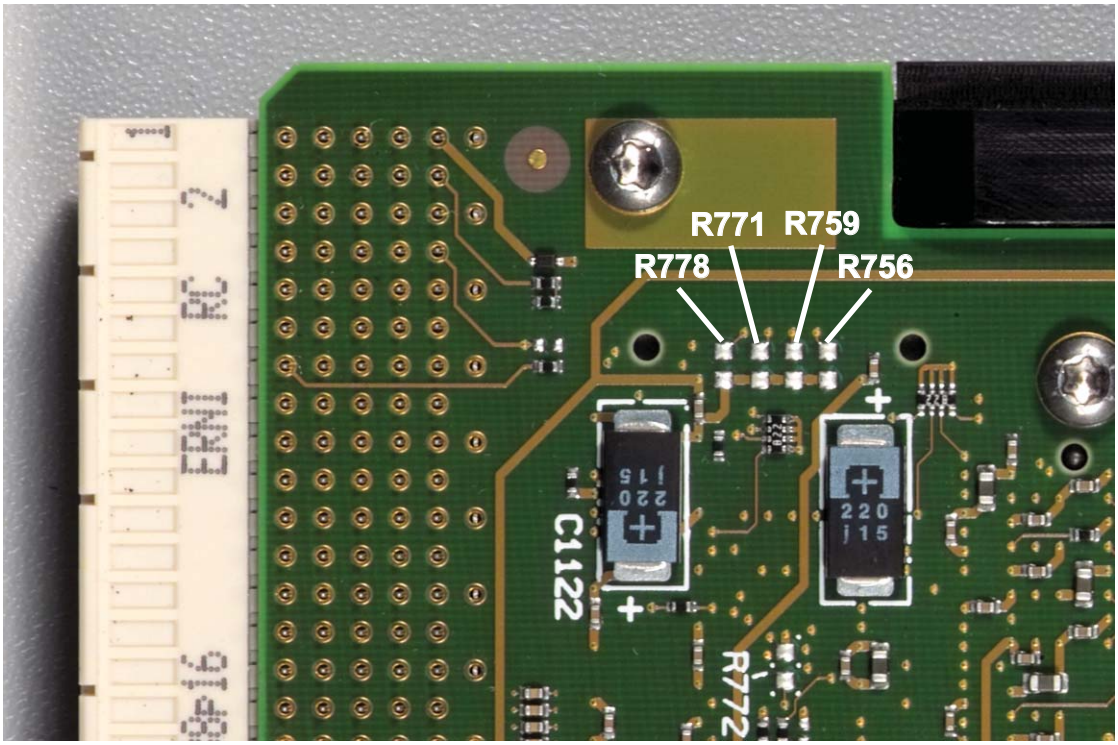

Table 4-4: Configuration Resistors' Settings

RESISTOR	SETTING	DESCRIPTION
R756	*Open*	*Boot-up with POST Code indication on the Debug LEDs*
	Closed	Boot-up with no POST Code indication on the Debug LEDs
R759	*Open*	*Boot from the standard SPI boot flash*
	Closed	Boot from the recovery SPI boot flash
R771	*Open*	Reserved
	Closed	
R778	*Open*	*Boot using the currently saved uEFI BIOS settings*
	Closed	Clear the uEFI BIOS settings and use the default values

The default setting is indicated by using italic bold.

Note ...

If R759 is set to Closed, the SPI boot flash selection cannot be overwritten by the IPMI controller.

4.3 Jumper Description

The CP6004-RA/-RC has three jumpers JP1, JP2, and JP3. JP1 is reserved for further use. JP2 and JP3 are used to activate the bus termination for COMB. For the location of the jumpers, refer to Figures 1-5 and 1-6.

4.3.1 COMB Termination Jumper Settings

When COMB is used and is the last device on the RS-422 bus, then the RS-422 interface must provide termination resistance. The purpose of the jumpers JP2 and JP3 is to enable this line termination resistor (120 ohm).

Table 4-5: JP2 Jumper Setting for RS-422 TXD Termination (COMB)

JP2	DESCRIPTION
Open	*TXD termination inactive*
Closed	TXD termination active (soldered jumper or 0 ohm resistor in 0805 package)

The default setting is indicated by using italic bold.

Table 4-6: JP3 Jumper Setting for RS-422 RXD Termination (COMB)

JP3	DESCRIPTION
Open	*RXD termination inactive*
Closed	RXD termination active (soldered jumper or 0 ohm resistor in 0805 package)

The default setting is indicated by using italic bold.

4.4 I/O Address Map

The following table indicates the CP6004-RA/-RC-specific registers.

Table 4-7: I/O Address Map

ADDRESS	DEVICE
0x080	uEFI BIOS POST Code Low Byte Register (POSTL)
0x081	uEFI BIOS POST Code High Byte Register (POSTH)
0x082 - 0x083	Reserved
0x084	Debug Low Byte Register (DBGL)
0x085	Debug High Byte Register (DBGH)
0x280	Status Register 0 (STAT0)
0x281	Status Register 1 (STAT1)
0x282	Control Register 0 (CTRL0)
0x283	Control Register 1 (CTRL1)
0x284	Device Protection Register (DPROT)
0x285	Reset Status Register (RSTAT)
0x286	Board Interrupt Configuration Register (BICFG)
0x287	Status Register 2 (STAT2)
0x288	Board ID High Byte Register (BIDH)
0x289	Board and PLD Revision Register (BREV)
0x28A	Geographic Addressing Register (GEOAD)
0x28B	Reserved
0x28C	Watchdog Timer Control Register (WTIM)
0x28D	Board ID Low Byte Register (BIDL)
0x28E - 0x28F	Reserved
0x290	LED Configuration Register (LCFG)
0x291	LED Control Register (LCTRL)
0x292	General Purpose Output Register (GPOUT)
0x293	General Purpose Input Register (GPIN)
0x294 - 0x29C	Reserved
0xCA2; 0xCA3	IPMI KCS interface

4.5 CP6004-RA/-RC-Specific Registers

The following registers are special registers which the CP6004-RA/-RC uses to watch the onboard hardware special features and the CompactPCI control signals.

Normally, only the system uEFI BIOS uses these registers, but they are documented here for application use as required.

Note ...
Take care when modifying the contents of these registers as the system uEFI BIOS may be relying on the state of the bits under its control.

4.5.1 Status Register 0 (STAT0)

The Status Register 0 holds general/common status information.

Table 4-8: Status Register 0 (STAT0)

REGISTER NAME		STATUS REGISTER 0 (STAT0)		
ADDRESS		0x280		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	HSHS	Hot swap handle status: 0 = Hot swap handle in closed position 1 = Hot swap handle in open position	N/A	R
6	BBEI	uEFI BIOS boot end indication: 0 = uEFI BIOS is booting 1 = uEFI BIOS boot is finished	0	R
5 - 4	BFSS	SPI boot flash selection status: 00 = Standard SPI boot flash active 01 = Recovery SPI boot flash active 10 = External SPI boot flash active 11 = Reserved	N/A	R
3	DIP4	DIP switch SW3, switch 4 (CP6004-RA) R778 (CP6004-RC)	N/A	R
2	DIP3	DIP switch SW3, switch 3 (CP6004-RA) R771 (CP6004-RC)	N/A	R
1	DIP2	DIP switch SW3, switch 2 (CP6004-RA) R759 (CP6004-RC)	N/A	R
0	DIP1	DIP switch SW3, switch 1 (CP6004-RA) R756 (CP6004-RC)	N/A	R

4.5.2 Status Register 1 (STAT1)

The Status Register 1 holds board-specific status information.

Table 4-9: Status Register 1 (STAT1)

REGISTER NAME		STATUS REGISTER 1 (STAT1)		
ADDRESS		0x281		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	C66EN	CPCI PCI speed (M66EN signal): 0 = 33 MHz 1 = 66 MHz	N/A	R
6	CVIO	CPCI backplane VI/O voltage configuration: 0 = 3.3V VI/O voltage 1 = 5V VI/O voltage	N/A	R
5	P66EN	PMC PCI speed (M66EN signal): 0 = 33 MHz 1 = 66 MHz	N/A	R
4	Res.	Reserved	0	R
3	CSYS	CPCI system slot identification (SYSEN# signal): 0 = Installed in a system slot 1 = Installed in a peripheral slot	N/A	R
2	CENUM	CPCI system enumeration (ENUM# signal): 0 = Indicates the insertion or removal of a hot swap system board 1 = No hot swap event	N/A	R
1	CFAL	CPCI power supply status (FAL# signal): 0 = Power supply failure 1 = Power in normal state	N/A	R
0	CDEG	CPCI power supply status (DEG# signal): 0 = Power derating 1 = Power in normal state	N/A	R

4.5.3 Control Register 0 (CTRL0)

The Control Register 0 holds general/common control information.

Table 4-10: Control Register 0 (CTRL0)

REGISTER NAME		CONTROL REGISTER 0 (CTRL0)		
ADDRESS		0x282		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 6	VGAM	VGA CRT mode configuration: 00 = Reserved 01 = Reserved 10 = Rear VGA CRT 11 = VGA CRT disabled	N/A	R/W
5 - 4	Res.	Reserved	00	R
3 - 2	CPMCB	COMB port mode configuration: 00 = RS-232 mode 01 = RS-422 mode 10 = Reserved 11 = Reserved	01	R/W
1 - 0	Res.	Reserved	00	R

4.5.4 Control Register 1 (CTRL1)

The Control Register 1 holds board-specific control information.

Table 4-11: Control Register 1 (CTRL1)

REGISTER NAME		CONTROL REGISTER 1 (CTRL1)		
ADDRESS		0x283		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	SRST	SATA Flash module reset: 0 = Reset of SATA Flash module 1 = SATA Flash module running	1	R/W
6	VRST	Integrated graphics controller configuration: 0 = Graphics controller disabled 1 = Graphics controller enabled	1	R
5	Res.	Reserved	0	R
4	CRST	Board reset via CPCI interface when installed in peripheral slot: 0 = Disable board reset via CPCI interface 1 = Enable board reset via CPCI interface	0	R/W
3	XRST	Board reset via XMC module: 0 = Disable board reset via XMC module 1 = Enable board reset via XMC module	0	R/W
2	Res.	Reserved	1	R
1	SETHB	Ethernet I/O configuration front port B: 0 = Front I/O (CP6004-RA) / Disabled (CP6004-RC) 1 = Rear I/O	0	R/W
0	SETHA	Ethernet I/O configuration front port A: 0 = Front I/O (CP6004-RA) / Disabled (CP6004-RC) 1 = Rear I/O	0	R/W

4.5.5 Device Protection Register (DPROT)

The Device Protection Register holds the write protect signals for flash devices.

Table 4-12: Device Protection Register (DPROT)

REGISTER NAME		DEVICE PROTECTION REGISTER (DPROT)		
ADDRESS		0x284		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	SWP	System write protection: 0 = Onboard non-volatile memory devices not write protected 1 = Onboard non-volatile memory devices write protected This bit reflects the state of the system hardware write protection signal SYS_WP#.	0	R
6 - 2	Res.	Reserved	00000	R
1	EEWP	EEPROM write protection: 0 = EEPROM not write protected 1 = EEPROM write protected Writing a '1' to this bit sets the bit. If this bit is set, it cannot be cleared.	0	R/W
0	BFWP	SPI flash write protection: 0 = SPI flash not write protected 1 = SPI flash write protected Writing a '1' to this bit sets the bit. If this bit is set, it cannot be cleared.	0	R/W

4.5.6 Reset Status Register (RSTAT)

The Reset Status Register is used to determine the host's reset source.

Table 4-13: Reset Status Register (RSTAT)

REGISTER NAME		RESET STATUS REGISTER (RSTAT)		
ADDRESS		0x285		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	PORS	Power-on reset status: 0 = System reset generated by software (warm reset) 1 = System reset generated by power-on (cold reset) Writing a '1' to this bit clears the bit.	N/A	R/W
6	Res.	Reserved	0	R
5	SRST	Software reset status: 0 = Reset is logged by the IPMI controller 1 = Reset is not logged by IPMI controller The uEFI BIOS/software sets this bit to inform the IPMI controller that the next reset should not be logged.	0	R/W
4	Res.	Reserved	0	R
3	IPRS	IPMI controller reset status: 0 = System reset not generated by IPMI 1 = System reset generated by IPMI Writing a '1' to this bit clears the bit.	0	R/W
2	FPRS	Front panel push button reset status: 0 = System reset not generated by front panel reset 1 = System reset generated by front panel reset Writing a '1' to this bit clears the bit.	0	R/W
1	CPRS	CompactPCI reset status (PRST signal): 0 = System reset not generated by CPCI reset input 1 = System reset generated by CPCI reset input Writing a '1' to this bit clears the bit.	0	R/W
0	WTRS	Watchdog timer reset status: 0 = System reset not generated by Watchdog timer 1 = System reset generated by Watchdog timer Writing a '1' to this bit clears the bit.	0	R/W

Note ...

The Reset Status Register is set to the default values by power-on reset, not by a warm reset.

4.5.7 Board Interrupt Configuration Register (BICFG)

The Board Interrupt Configuration Register holds a series of bits defining the interrupt routing for the Watchdog. If the Watchdog timer fails, it can generate an IRQ5 interrupt.

The enumeration signal is generated by a hot swap compatible board after insertion and prior to removal. The system uses this interrupt signal to force software to configure the new board. The derate signal indicates that the power supply is beginning to derate its power output.

Table 4-14: Board Interrupt Configuration Register (BICFG)

REGISTER NAME		BOARD INTERRUPT CONFIGURATION REGISTER (BICFG)		
ADDRESS		0x286		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	Res.	Reserved	0	R/W
6	CFICF	CPCI fail signal to IRQ5 routing (FAL# signal): 0 = Disabled 1 = Enabled	0	R/W
5	CEICF	CPCI enumeration signal to IRQ5 routing (ENUM# signal): 0 = Disabled 1 = Enabled	0	R/W
4	CDICF	CPCI derate signal to IRQ5 routing (DEG# signal): 0 = Disabled 1 = Enabled	0	R/W
3 - 2	KICF	IPMI KCS interrupt configuration 00 = Disabled 01 = IRQ11 10 = IRQ10 11 = Reserved	00	R
1 - 0	WICF	Watchdog interrupt configuration: 00 = Disabled 01 = IRQ5 10 = Reserved 11 = Reserved	00	R/W

4.5.8 Status Register 2 (STAT2)

The Status Register 2 holds board-specific status information.

Table 4-15: Status Register 2 (STAT2)

REGISTER NAME		STATUS REGISTER 2 (STAT2)		
ADDRESS		0x287		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 2	Res.	Reserved	000000	R
1	XAP	XMC module: 0 = Not present 1 = Present	N/A	R
0	Res.	Reserved	0	R

4.5.9 Board ID High Byte Register (BIDH)

Each Kontron board is provided with a unique 16-bit board-type identifier in the form of a hexadecimal number. The Board ID High Byte Register is located in the address 0x288. The Board ID Low Byte Register is located in the address 0x28D.

Table 4-16: Board ID High Byte Register (BIDH)

REGISTER NAME		BOARD ID HIGH BYTE REGISTER (BIDH)		
ADDRESS		0x288		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 0	BIDH	Board identification: CP6004-RA: 0xB3D9 CP6004-RC: 0xB3D8	0xB3	R

4.5.10 Board and PLD Revision Register (BREV)

The Board and PLD Revision Register signals to the software when differences in the board and the Programmable Logic Device (PLD) require different handling by the software. It starts with the value 0x00 and will be incremented with each change in hardware as development continues.

Table 4-17: Board and PLD Revision Register (BREV)

REGISTER NAME		BOARD AND PLD REVISION REGISTER (BREV)		
ADDRESS		0x289		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	BREV	Board revision	N/A	R
3 - 0	PREV	PLD revision	N/A	R

4.5.11 Geographic Addressing Register (GEOAD)

This register holds the CompactPCI geographic address (site number) used to assign the Intelligent Platform Management Bus (IPMB) address to the CP6004-RA/-RC.

Table 4-18: Geographic Addressing Register (GEOAD)

REGISTER NAME		GEOGRAPHIC ADDRESSING REGISTER (GEOAD)		
ADDRESS		0x28A		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 5	Res.	Reserved	000	R
4 - 0	GA	Geographic address	N/A	R

Note ...

The Geographic Addressing Register is set to the default values by power-on reset, not by warm reset.

4.5.12 Watchdog Timer Control Register (WTIM)

The CP6004-RA/-RC has one Watchdog timer provided with a programmable timeout ranging from 125 msec to 4096 sec. Failure to strobe the Watchdog timer within a set time period results in a system reset or an interrupt. The interrupt mode can be configured via the Board Interrupt Configuration Register (0x286).

There are four possible modes of operation involving the Watchdog timer:

- Timer only mode
- Reset mode
- Interrupt mode
- Dual stage mode

At power on the Watchdog is not enabled. If not required, it is not necessary to enable it. If required, the bits of the Watchdog Timer Control Register must be set according to the application requirements. To operate the Watchdog, the mode and time period required must first be set and then the Watchdog enabled. Once enabled, the Watchdog can only be disabled or the mode changed by powering down and then up again. To prevent a Watchdog timeout, the Watchdog must be retriggered before timing out. This is done by writing a ’1’ to the WTR bit. In the event a Watchdog timeout does occur, the WTE bit is set to ’1’. What transpires after this depends on the mode selected.

The four operational Watchdog timer modes can be configured by the WMD[1:0] bits, and are described as follows:

Timer only mode - In this mode the Watchdog is enabled using the required timeout period. Normally, the Watchdog is retriggered by writing a ’1’ to the WTR bit. In the event a timeout occurs, the WTE bit is set to ’1’. This bit can then be polled by the application and handled accordingly. To continue using the Watchdog, write a ’1’ to the WTE bit, and then retrigger the Watchdog using WTR. The WTE bit retains its setting as long as no power down-up is done. Therefore, this bit may be used to verify the status of the Watchdog.

Reset mode - This mode is used to force a hard reset in the event of a Watchdog timeout. In addition, the WTE bit is not reset by the hard reset, which makes it available if necessary to determine the status of the Watchdog prior to the reset.

Interrupt mode - This mode causes the generation of an interrupt in the event of a Watchdog timeout. The interrupt handling is a function of the application. If required, the WTE bit can be used to determine if a Watchdog timeout has occurred.

Dual stage mode - This is a complex mode where in the event of a timeout two things occur: 1) an interrupt is generated, and 2) the Watchdog is retriggered automatically. In the event a second timeout occurs immediately following the first timeout, a hard reset will be generated. The second timeout period is the same as the first. If the Watchdog is retriggered normally, operation continues. The interrupt generated at the first timeout is available to the application to handle the first timeout if required. As with all of the other modes, the WTE bit is available for application use.

Table 4-19: Watchdog Timer Control Register (WTIM)

REGISTER NAME		WATCHDOG TIMER CONTROL REGISTER (WTIM)		
ADDRESS		0x28C		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	WTE	Watchdog timer expired status bit 0 = Watchdog timer has not expired 1 = Watchdog timer has expired. Writing a '1' to this bit resets it to 0.	0	R/W
6 - 5	WMD	Watchdog mode 00 = Timer only mode 01 = Reset mode 10 = Interrupt mode 11 = Cascaded mode (dual-stage mode)	00	R/W
4	WEN/WTR	Watchdog enable / Watchdog trigger control bit: 0 = Watchdog timer not enabled Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog timer is enabled, it will indicate a '1'. 1 = Watchdog timer enabled Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by bits WTM[3:0].	0	R/W
3 - 0	WTM	Watchdog timeout settings: 0000 = 0.125 s 0001 = 0.25 s 0010 = 0.5 s 0011 = 1 s 0100 = 2 s 0101 = 4 s 0110 = 8 s 0111 = 16 s 1000 = 32 s 1001 = 64 s 1010 = 128 s 1011 = 256 s 1100 = 512 s 1101 = 1024 s 1110 = 2048 s 1111 = 4096 s	0000	R/W

4.5.13 Board ID Low Byte Register (BIDL)

Each Kontron board is provided with a unique 16-bit board-type identifier in the form of a hexadecimal number. The Board ID Low Byte Register is located in the address 0x28D. The Board ID High Byte Register is located in the address 0x288.

Table 4-20: Board ID Low Byte Register (BIDL)

REGISTER NAME		BOARD ID LOW BYTE REGISTER (BIDL)		
ADDRESS		0x28D		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 0	BIDL	Board identification: CP6004-RA: 0xB3D9 CP6004-RC: 0xB3D8	0xDx	R

4.5.14 LED Configuration Register (LCFG)

The LED Configuration Register holds a series of bits defining the onboard configuration of the Debug LEDs (DLED 0..3). For the location of the Debug LEDs, refer to Figures 1-5 and 1-6.

Table 4-21: LED Configuration Register (LCFG)

REGISTER NAME		LED CONFIGURATION REGISTER (LCFG)		
ADDRESS		0x290		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	Res.	Reserved	0000	R
3-0	LCON	LED Configuration: 0000 = POST [1)] 0001 = Mode A [2)] 0010 - 1111 = Reserved	0001	R/W

[1)] In uEFI BIOS POST mode, the Debug LEDs build a binary vector to display uEFI BIOS POST code during the pre-boot phase. In doing so, the higher 4-bit nibble of the 8-bit uEFI BIOS POST code is displayed followed by the lower nibble followed by a pause. The uEFI BIOS POST code is displayed in general in green color.

DLED3: POST bit 3 and bit 7 (green)
DLED2: POST bit 2 and bit 6 (green)
DLED1: POST bit 1 and bit 5 (green)
DLED0: POST bit 0 and bit 4 (green)

[2)] Configured for Mode A, the Debug LEDs are dedicated to functions as follows:

DLED3: LED 3 (red/green/red+green)
DLED2: LED 2 (red/green/red+green)
DLED1: LED 1 (red/green/red+green)
DLED0: LED 0 (red/green/red+green)

Besides the configurable functions described above, the Debug LEDs fulfill also a basic debug function during the power-up phase as long as the first access to Port 80 is processed. If an LED lights red and stays red, than a basic error is present on the board. The following debug functions are defined and displayed during this initialization phase.

DLED3: PGOOD, Power Good status not reached (red)
DLED2: CPU catastrophic error (red)
DLED1: RST, PCI reset active / not deactivated (red)
DLED0: uEFI BIOS boot failure (red)

4.5.15 LED Control Register (LCTRL)

This register is used to switch on and off the Debug LEDs (DLED 0..3).

Table 4-22: LED Control Register (LCTRL)

REGISTER NAME		LED CONTROL REGISTER (LCTRL)		
ADDRESS		0x291		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	LCMD	Debug LED command: 0000 = Get DLED 0 0001 = Get DLED 1 0010 = Get DLED 2 0011 = Get DLED 3 0100 - 0111 = Reserved 1000 = Set DLED 0 1001 = Set DLED 1 1010 = Set DLED 2 1011 = Set DLED 3 1100 - 1111 = Reserved	0000	R/W
3-0	LCOL	Debug LED color: 0000 = Off 0001 = Green 0010 = Red 0011 = Red+green 0100 - 1111 = Reserved	0000	R/W

Note ...

This register can only be used if the Debug LEDs indicated in the “LED Configuration Register” (Table 4-21) are configured in Mode A.

4.5.16 General Purpose Output Register (GPOUT)

This register is used to control the general purpose output signals on the rear I/O CPCI connectors.

Table 4-23: General Purpose Output Register (GPOUT)

REGISTER NAME		GENERAL PURPOSE OUTPUT REGISTER (GPOUT)		
ADDRESS		0x292		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	Res.	Reserved	0000	R
3	GPO3	General Purpose Output 3: 0 = Output low 1 = Output high	0	R/W
2	GPO2	General Purpose Output 2: 0 = Output low 1 = Output high	0	R/W
1	GPO1	General Purpose Output 1: 0 = Output low 1 = Output high	0	R/W
0	GPO0	General Purpose Output 0: 0 = Output low 1 = Output high	0	R/W

4.5.17 General Purpose Input Register (GPIN)

This register is used to control the general purpose input signals on the rear I/O CPCI connectors.

Table 4-24: General Purpose Input Register (GPIN)

REGISTER NAME		GENERAL PURPOSE INPUT REGISTER (GPIN)		
ADDRESS		0x293		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	Res.	Reserved	0000	R
3	GPI3	General Purpose Input 3: 0 = Input low 1 = Input high	1	R
2	GPI2	General Purpose Input 2: 0 = Input low 1 = Input high	1	R
1	GPI1	General Purpose Input 1: 0 = Input low 1 = Input high	1	R
0	GPI0	General Purpose Input 0: 0 = Input low 1 = Input high	1	R

4.5.18 IPMI Keyboard Controller Style Interface

The host processor communicates with the IPMI controller using one Keyboard Controller Style (KCS) interface, which is defined in the IPMI specification. The KCS interface is on the I/O location 0xCA2 and 0xCA3, and configured as regular ISA interrupt.

Chapter 5

Power Considerations

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5. Power Considerations

5.1 System Power

The considerations presented in the ensuing chapters must be taken into account by system integrators when specifying the CP6004-RA/-RC system environment.

5.1.1 CP6004-RA/-RC Baseboard

The CP6004-RA/-RC baseboard itself has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the CP6004-RA/-RC should be carefully tested to ensure compliance with these ratings.

Table 5-1: Maximum Input Power Voltage Limits

SUPPLY VOLTAGE	MAXIMUM PERMITTED VOLTAGE
+3.3 V	+3.6 V
+5 V	+5.5 V
+12 V	+14.0 V
-12 V	-14.0 V

Warning!

The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with the above may result in damage to your board.

The following table specifies the ranges for the different input power voltages within which the board is functional. The CP6004-RA/-RC is not guaranteed to function if the board is not operated within the prescribed limits.

Table 5-2: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	RECOMMENDED RANGE
+3.3 V	3.2 V min. to 3.47 V max.	3.3 V min. to 3.47 V max.
+5 V	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.
+12 V	11.4 V min. to 12.6 V max.	12 V min. to 12.6 V max.
-12 V	-11.4 V min. to -12.6 V max.	Only for PMC/XMC

5.1.2 Backplane

Backplanes to be used with the CP6004-RA/-RC must be adequately specified. The backplane must provide optimal power distribution for the +3.3 V, +5 V and +12 V power inputs.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under-dimensioned cabling or bridges, high resistance connections, etc. must be avoided. It is recommended to use POSITRONIC or M-type connector backplanes and power supplies where possible.

5.1.3 Power Supply Units

Power supplies for the CP6004-RA/-RC must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires.

As the design of the CP6004-RA/-RC has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for backplane input line resistance variations due to temperature changes, etc.

5.1.3.1 Start-Up Requirement

Power supplies must comply with the following guidelines, in order to be used with the CP6004-RA/-RC:

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

5.1.3.2 Power-Up Sequence

The +5 VDC output level must always be equal to or higher than the +3.3 VDC output during power-up and normal operation. Both voltages must reach their minimum in-regulation level not later than 20 ms after the output power ramp start.

5.1.3.3 Tolerance

The tolerance of the voltage lines is described in the CompactPCI specification (PICMG 2.0 R3.0). The recommended measurement point for the voltage is the CompactPCI connector on the CPU board. The following table provides information regarding the required characteristics for each board input voltage.

Table 5-3: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (p-p)	REMARKS
5 V	+5.0 VDC	+5%/-3%	50 mV	Main voltage
3.3 V	+3.3 VDC	+5%/-3%	50 mV	–
+12 V	+12 VDC	+5%/-5%	240 mV	Required
-12 V	-12 VDC	+5%/-5%	240 mV	Not required
VI/O (PCI) voltage	+3.3 VDC or +5 VDC	+5%/-3%	50 mV	–
GND	Ground, not directly connected to potential earth (PE)			

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

5.1.3.4 Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

Warning!

All of the input voltages must be functionally coupled to each other so that if one input voltage fails, all other input voltages must be regulated proportionately to the failed voltage. For example, if the +5V begins to decrease, all other input voltages must decrease accordingly. This is required in order to preclude cross currents within the CP6004-RA/-RC.

Failure to comply with above may result in damage to the board or improper system operation.

Note ...

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until the capacitors are discharged. If the voltage rises again before it has gone below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.2 Power Consumption of CP6004-RA/-RC

The goal of this description is to provide a method to calculate the power consumption for the CP6004-RA/-RC baseboard and for additional configurations. The processor with the integrated graphics controller dissipates the majority of the thermal power.

The power consumption tables below list the voltage and the power specifications for the CP6004-RA/-RC board and its accessories.

The values were measured using the following testing parameters:

- board installed in an 8-slot passive CompactPCI backplane with two power supplies, one for the CPU, and the other for the hard disk
- board installed in the system slot
- 3.3 V and 5 V supply voltage
- 2.5 m/s airflow

The operating systems used were uEFI shell and Windows® 7, 64-bit. All measurements were conducted at a temperature of 25°C. The measured values varied because the power consumption was dependent on the processor activity.

Note ...

The power consumption values indicated in the tables below can vary depending on the ambient temperature or the system performance. This can result in deviations of the power consumption values of up to 15%.

The payload power consumption was measured using the following 3rd generation processors:

- Intel® Core™ i7-3612QE (SV) quad-core processor, 2.1 GHz, 6 MB L3 cache
- Intel® Core™ i7-3555LE (LV) dual-core processor, 2.5 GHz, 4 MB L3 cache

with the following firmware and under the following testing conditions:

- CP6004-RA/-RC in uEFI shell mode
  For this measurement the processor cores were active (no power management enabled), the graphics controller was in idle state (no application running) and Intel® Turbo Boost Technology was enabled.
- CP6004-RA/-RC running under Windows® 7, 64-bit, with processor and graphics controller in idle state
  For this measurement all processor cores and the graphics controller were in idle state (no application running) and Intel® Turbo Boost Technology was enabled.
- CP6004-RA/-RC running under Windows® 7, 64-bit, with reduced processor frequency and basic graphics operation
  For this measurement all processor cores were operating at a reduced frequency and maximum workload while the graphics controller was performing basic operation (e.g. dual screen output configuration with no 3D graphics application running) and Intel® Turbo Boost Technology was disabled. The frequency of the Intel® Core™ i7-3612QE (SV) was reduced to 1.5 GHz and that of the Intel® Core™ i7-3555LE (LV) to 1.8 GHz during this measurement.
- CP6004-RA/-RC running under Windows® 7, 64-bit, with maximum processor workload and basic graphics operation
  For this measurement all processor cores were operating at maximum workload and the graphics controller was performing basic operation (e.g. dual screen output configuration with no 3D graphics application running) while Intel® Turbo Boost Technology was disabled. These values represent the power dissipation reached under realistic, OS-controlled applications with the processor operating at maximum performance.
- CP6004-RA/-RC running under Windows® 7, 64-bit, with maximum processor and graphics controller workload
  These values represent the maximum power dissipation achieved through the use of specific tools to heat up the processor and the graphics controller. For this measurement Intel® Turbo Boost Technology was enabled. These values are unlikely to be reached in real applications.

The following tables indicate the typical power consumption of the CP6004-RA/-RC with 4 GB DDR3 SDRAM in dual-channel mode. The measurements were made with the CP6004-RA/-RC in uEFI shell mode as well as with the Windows® 7 operating system, 64-bit.

Table 5-4: uEFI Shell Mode

NOMINAL VOLTAGE	TYPICAL POWER CONSUMPTION	
	Intel® Core™ i7-3612QE (SV) 2.1 GHz	Intel® Core™ i7-3555LE (LV) 2.5 GHz
+12 V	0.1 W	0.1 W
5 V	7.0 W	6.0 W
3.3 V	12.0 W	12.0 W
Total	19.1 W	18.1 W

Table 5-5: Win. 7 with Processor and Graphics in Idle State

NOMINAL VOLTAGE	TYPICAL POWER CONSUMPTION	
	Intel® Core™ i7-3612QE (SV) 2.1 GHz	Intel® Core™ i7-3555LE (LV) 2.5 GHz
+12 V	0.1 W	0.1 W
5 V	5.1 W	2.1 W
3.3 V	10.0 W	10.0 W
Total	15.2 W	12.2 W

Table 5-6: Win. 7 with Reduced Processor Frequency and Basic Graphics Operation

NOMINAL VOLTAGE	TYPICAL POWER CONSUMPTION	
	Intel® Core™ i7-3612QE (SV) 2.1 GHz	Intel® Core™ i7-3555LE (LV) 2.5 GHz
+12 V	0.1 W	0.1 W
5 V	17.0 W	11.0 W
3.3 V	12.0 W	12.0 W
Total	29.1 W	23.1 W

Table 5-7: Win. 7 with Maximum Processor Workload and Basic Graphics Operation

NOMINAL VOLTAGE	TYPICAL POWER CONSUMPTION	
	Intel® Core™ i7-3612QE (SV) 2.1 GHz	Intel® Core™ i7-3555LE (LV) 2.5 GHz
+12 V	0.1 W	0.1 W
5 V	22.5 W	14.5 W
3.3 V	12.0 W	12.0 W
Total	34.6 W	26.6 W

Table 5-8: Win. 7 with Maximum Processor and Graphics Workload

NOMINAL VOLTAGE	TYPICAL POWER CONSUMPTION	
	Intel® Core™ i7-3612QE (SV) 2.1 GHz	Intel® Core™ i7-3555LE (LV) 2.5 GHz
+12 V	0.1 W	0.1 W
5 V	35.0 W	25.0 W
3.3 V	18.0 W	17.0 W
Total	53.1 W	42.1 W

5.2.1 Power Consumption of the CP6004-RA/-RC Accessories

The following table indicates the power consumption of the CP6004-RA/-RC accessories.

Table 5-9: Power Consumption of CP6004-RA/-RC Accessories

MODULE	POWER 5 V	POWER 3.3 V
Keyboard	approx. 0.1 W	—
DDR3 SDRAM update from 4 GB to 8 GB	—	approx. 1.0 W
DDR3 SDRAM update from 4 GB to 16 GB	—	approx. 2.0 W
SATA Flash module	—	approx. 1.0 W

5.2.2 Power Consumption per Gigabit Ethernet Port

The following table indicates the power consumption per Gigabit Ethernet port.

Table 5-10: Power Consumption per Gigabit Ethernet Port

POWER CONSUMPTION	POWER 5 V	POWER 3.3 V
One 1000 Mb/s Ethernet port connected	—	approx. 0.5 W

5.3 Maximum Power Consumption of PMC Modules

A maximum power of 7.5 W is available on the PMC slot. This is in accordance with the draft standard P1386/Draft 2.4a. The maximum power of 7.5 W can be arbitrarily divided on the 3.3 V and 5 V voltage lines.

The following table indicates the current of a (conduction-cooled) PMC module.

Table 5-11: PMC/CCPMC Module Current

VOLTAGE	CONTINUOUS CURRENT	PEAK CURRENT
3.3 V	2.27 A	3.0 A
5 V	1.5 A	2.0 A
+12 V	0.6 A	0.8 A
-12 V	0.4 A	0.4 A

5.4 Maximum Power Consumption of XMC Modules

A maximum power of 15 W is available on the XMC slot and it can be arbitrarily divided on the 3.3 V and 5 V (VPWR) voltage lines. XMC modules are based on 3.3 V power along with variable power (VPWR) defined as either 5 V or 12 V in the ANSI/VITA 42.0-200x XMC Switched Mezzanine Card Auxiliary Standard specification. On the CP6004-RA/-RC, the VPWR is configured to 5 V.

The following table indicates the current of a (conduction-cooled) XMC module.

Table 5-12: XMC/Conduction-Cooled XMC Module Current

VOLTAGE	CONTINUOUS CURRENT	PEAK CURRENT
3.3 V	0.75 A	1.0 A
5 V (VPWR)	2.5 A	3.0 A
+12 V	0.6 A	0.8 A
-12 V	0.4 A	0.4 A

Note ...

XMC integrators should carefully review the power ratings, cooling capacity and airflow requirements in the application prior to installation of an XMC module on the CP6004-RA/-RC.

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Chapter 6

Thermal Considerations

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6. Thermal Considerations

The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing CP6004-RA/-RC applications.

6.1 Board Internal Thermal Monitoring

To ensure optimal operation and long-term reliability of the CP6004-RA/-RC, all onboard components must remain within the maximum temperature specifications. The most critical components on the CP6004-RA/-RC are the processor and the chipset. Operating the CP6004-RA/-RC above the maximum operating limits will result in permanent damage to the board. To ensure functionality at the maximum temperature, the IPMI controller supports several temperature monitoring and control features.

The CP6004-RA/-RC includes several temperature sensors to measure the onboard temperature values:

- Thermal sensors integrated in the processor
- Thermal sensor integrated in the chipset
- Onboard temperature sensor Temp1 (see Figures 1-5 and 1-6 for its placement)

The onboard temperature sensor Temp1 is accessible via the IPMI controller. For information on the temperature sensors integrated in the CPU and the chipset, refer to Chapter 6.2 and Chapter 6.3.

6.2 Processor Thermal Monitoring

To allow optimal operation and long-term reliability of the CP6004-RA/-RC, the 3rd generation Intel® Core™ i7 processor must remain within the maximum die temperature specifications. The maximum operating temperature for the processor die is 105°C.

The 3rd generation Intel® Core™ i7 processor uses the Adaptive Thermal Monitor feature to protect the processor from overheating and includes the following on-die temperature sensors:

- One Digital Thermal Sensor (DTS) for monitoring each processor core
- One Digital Thermal Sensor (DTS) for monitoring the graphics core
- One Digital Thermal Sensor (DTS) for monitoring the die temperature
- Catastrophic Cooling Failure Sensor (THERMTRIP#)

These sensors are integrated in the processor and work without any interoperability of the IPMI Controller, the uEFI BIOS or the software application. Thermal Control Circuit allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

6.2.1 Digital Thermal Sensor (DTS)

The 3rd generation Intel® Core™ i7 processor includes up to six on-die Digital Thermal Sensors (DTS), up to four for the processor cores, one for the graphics core and one for the package die. They can be read via an internal register of the processor. The temperature returned by the Digital Thermal Sensor will always be at or below the maximum operating temperature (105°C). Via the Digital Thermal Sensors, the uEFI BIOS, the IPMI controller or the application software can measure the processor die temperature.

6.2.2 Adaptive Thermal Monitor

The Adaptive Thermal Monitor feature reduces the processor power consumption and the temperature when the processor silicon exceeds its maximum operating temperature until the processor operates at or below its maximum operating temperature.

The processor core power reduction is achieved by:

- Frequency/sVID Control (by reducing of processor core voltage)
- Clock Modulation (by turning the internal processor core clocks off and on)

Adaptive Thermal Monitor dynamically selects the appropriate method. uEFI BIOS is not required to select a specific method as with previous-generation processors supporting Intel® Thermal Monitor 1 (TM1) and Intel® Thermal Monitor 2 (TM2).

The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

6.2.2.1 Frequency/sVID Control

Frequency/sVID Control reduces the processor's operating frequency (using the core ratio multiplier) and the input voltage (using serial VID signals). This combination of lower frequency and VID results in a reduction of the processor power consumption.

When the processor temperature reaches the TCC activation point, the event is reported via an external signal to the IPMI controller.

Running the processor at the lower frequency and voltage will reduce power consumption and should allow the processor to cool off. If the processor temperature does not drop below its maximum operating temperature, a second frequency and voltage transition will take place. This sequence of temperature checking and Frequency/sVID reduction will continue until either the minimum frequency has been reached or the processor temperature has dropped below its maximum operating temperature. If the processor temperature remains above its maximum operating temperature even after the minimum frequency has been reached, then Clock Modulation at that minimum frequency will be initiated.

Note ...

When the TH LED on the front panel is lit red after boot-up, it indicates that the processor die temperature is above 105°C.

6.2.2.2 Clock Modulation

Clock Modulation reduces power consumption by rapidly turning the internal processor core clocks off and on at a duty cycle that should reduce power dissipation (typically a 30-50% duty cycle).

Once the temperature has dropped below the maximum operating temperature, the TCC goes inactive and clock modulation ceases.

Note ...

When the TH LED on the front panel is lit red after boot-up, it indicates that the processor die temperature is above 105°C.

6.2.3 Catastrophic Cooling Failure Sensor

The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating. The Catastrophic Cooling Failure Sensor threshold is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 125°C. Once activated, the event remains latched until the CP6004-RA/-RC undergoes a power-on restart (all power off and then on again).

This function cannot be enabled or disabled in the uEFI BIOS. It is always enabled to ensure that the processor is protected in any event.

Note ...

When the TH LED on the front panel is blinking red, it indicates that the processor temperature is above 125°C.

6.3 Chipset Thermal Monitor Feature

The Intel® QM77 Chipset includes one on-die Thermal Diode Sensor to measure the chipset die temperature.

The maximum Intel® QM77 Chipset junction temperature is 108°C.

6.4 External Thermal Regulation for CP6004-RA

To ensure the best possible basis for operational stability and long-term reliability, the CP6004-RA is equipped with a heat sink. Coupled together with system chassis, which provides variable configurations for forced airflow, controlled active thermal energy dissipation is guaranteed. The physical size, shape, and construction of the heat sink ensures the lowest possible thermal resistance. In addition, the CP6004-RA has been specifically designed to efficiently support forced airflow as found in modern CompactPCI systems.

Thermal Characteristic Graphs for CP6004-RA

The thermal characteristic graphs shown on the following sections illustrate the maximum ambient air temperature as a function of the volumetric airflow rate for the power consumption indicated. The diagrams are intended to serve as guidance for reconciling board and system with the required computing power considering the thermal aspect. One diagram per CPU version is provided. There are up to two curves representing upper level working points based on different levels of average CPU utilization. When operating below the corresponding curve, the CPU runs steadily without any intervention of thermal supervision. When operated above the corresponding curve, various thermal protection mechanisms may take effect resulting in temporarily reduced CPU performance or finally in an emergency stop in order to protect the CPU and the chipset from thermal destruction. In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

An airflow of 2.0 m/s to 3.0 m/s is a typical value for a standard *Kontron* ASM rack. For other racks or housings the available airflow will differ. The maximum ambient operating temperature must be recalculated and/or measured for such environments. For the calculation of the maximum ambient operating temperature, the processor and chipset junction temperature must never exceed the specified limit for the involved processor and chipset.

Thermal characteristic curves

- Thermal characteristic curve of the CP6004-RA with maximum processor workload and basic graphics operation
  This load complies with the values indicated in Chapter 5.2, “Power Consumption of the CP6004-RA/-RC”, Table 5-6.
- Thermal characteristic curve of the CP6004-RA with maximum processor and graphics controller workload
  This load complies with the values indicated in Chapter 5.2, “Power Consumption of the CP6004-RA/-RC”, Table 5-7.

How to read the diagram

Select a specific CPU and choose a specific working point. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, thermal supervision will not be activated. Above this operating point, thermal supervision will become active protecting the CPU from thermal destruction. The minimum airflow rate provided must be more than the value specified in the diagram.

Volumetric flow rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth. The volumetric flow rate is specified in m^3/h (cubic-meter-per-hour) or cfm (cubic-feet-per-minute) respectively.

Conversion: 1 cfm = 1.7 m^3/h; 1 m^3/h = 0.59 cfm

Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric flow rate / area.

The airflow is specified in m/s (meter-per-second) or in fps (feet-per-second) respectively.

Conversion: 1 fps = 0.3048 m/s; 1 m/s = 3.28 fps

The following figures illustrate the operational limits of the CP6004-RA taking into consideration power consumption vs. ambient air temperature vs. airflow rate. The measurements were made based on a 4HP slot and with both processor cores enabled.

6.4.1 Operational Limits for the CP6004-RA

Figure 6-1: CP6004-RA with Quad-Core Intel® Core™ i7-3612QE (SV) 2.1 GHz

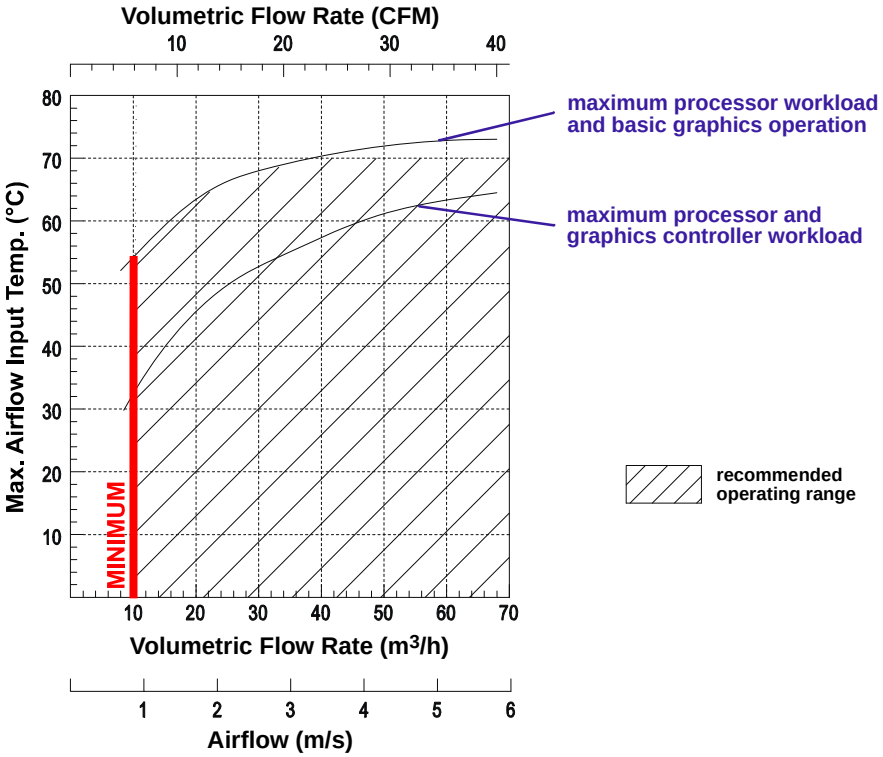
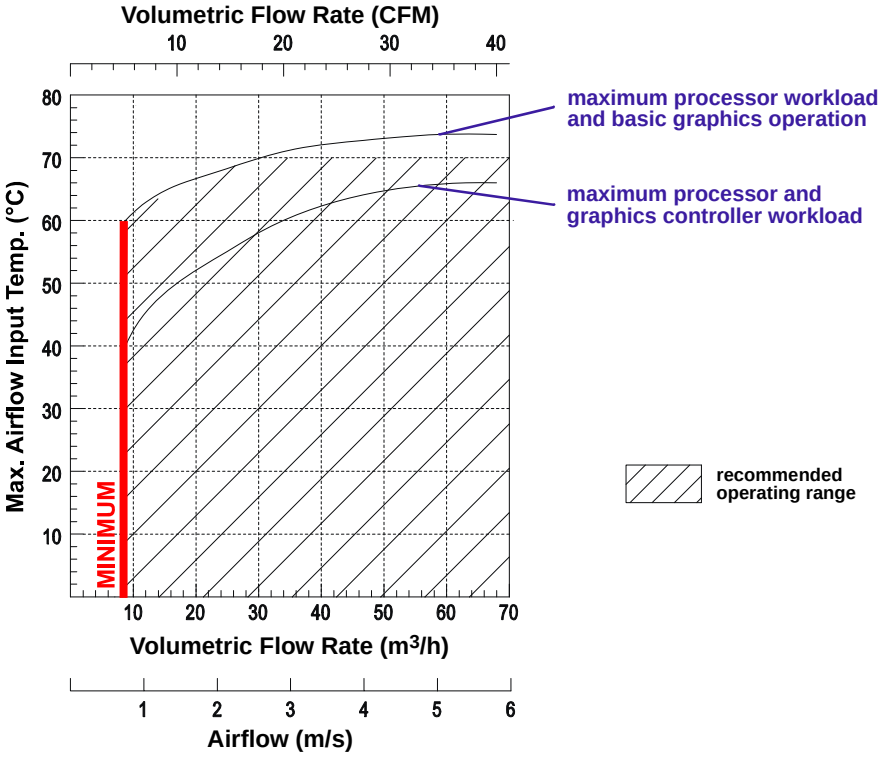


Figure 6-2: CP6004-RA with Dual-Core Intel® Core™ i7-3555LE (LV) 2.5 GHz



6.5 Thermal Characteristics for the CP6004-RC

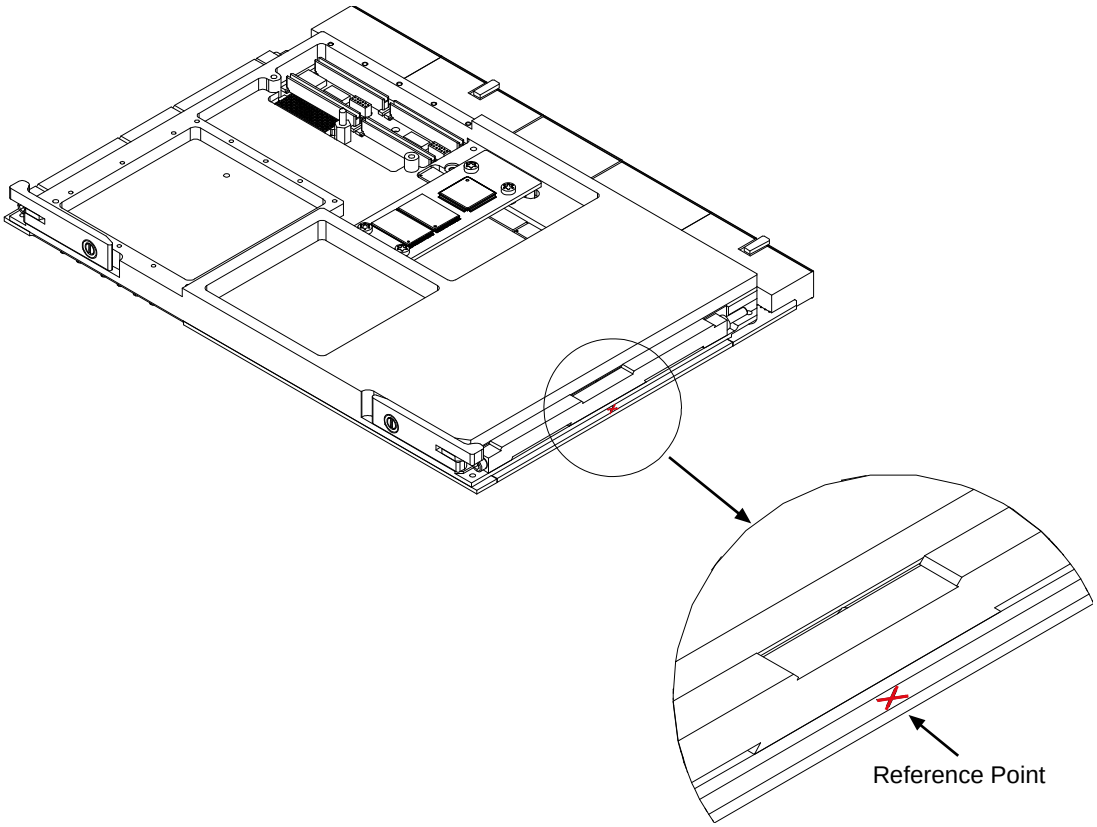
The thermal concept of the CP6004-RC is based on a specially designed full-board heat spreader and wedge lock clamping mechanisms.

The heat spreader provides optimal heat transfer to the board's top and bottom edges as well as enhanced structural support for ruggedized environments.

The wedge locks serve two functions. First, they provide a highly stable mechanical fixation of the board in the chassis slot. When expanded using the proper torque value, they form with the heat spreader practically a single physical unit capable of withstanding very high shock and vibration forces. Second, they are the primary mechanism for conduction of heat from the board to the system chassis.

Cooling of the CP6004-RC is a function of the system chassis which must provide adequate conduction cooling capability. To determine cooling performance, the board temperature can be measured at the reference point indicated in the figure below.

Figure 6-3: Position of the Reference Point on the CP6004-RC



The following table provides the maximum reference point temperature for the CP6004-RC under the indicated conditions. Operation at temperatures above those specified for the table below can result in reduced system performance or damage to the system.

Table 6-1: Maximum Reference Point Temperature with Core™ i7-3612QE

MAXIMUM REFERENCE POINT TEMPERATURE AT 105°C CPU DIE TEMPERATURE Intel® Core™ i7-3612QE (SV), 2.1 GHz		
MAXIMUM PROCESSOR AND GRAPHICS CONTROLLER WORKLOAD	TYPICAL PROCESSOR AND GRAPHICS CONTROLLER WORKLOAD	TYPICAL PROCESSOR AND GRAPHICS CONTROLLER WORKLOAD AT A REDUCED CPU FREQUENCY OF 1.5 GHz
75°C	80°C	85°C

Table 6-2: Maximum Reference Point Temperature with Core™ i7-3555LE

MAXIMUM REFERENCE POINT TEMPERATURE AT 105°C CPU DIE TEMPERATURE Intel® Core™ i7-3555LE (LV), 2.5 GHz		
MAXIMUM PROCESSOR AND GRAPHICS CONTROLLER WORKLOAD	TYPICAL PROCESSOR AND GRAPHICS CONTROLLER WORKLOAD	TYPICAL PROCESSOR AND GRAPHICS CONTROLLER WORKLOAD AT A REDUCED CPU FREQUENCY OF 1.8 GHz
70°C	75°C	80°C

Note ...

The temperature values indicated in the tables above can vary depending on the location of the measurement point or the system performance.

Warning!

As Kontron assumes no responsibility for any damage to the CP6004-RC or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the CP6004-RC complies with the thermal considerations set forth in this document.

6.6 Peripherals

When determining the thermal requirements for a given application, peripherals to be used with the CP6004-RA/-RC must also be considered. Devices such as PMC modules, CCPMC modules, XMC modules, conduction-cooled XMC modules and SATA Flash modules which are directly attached to the CP6004-RA/-RC must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions. In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

Warning!

As Kontron assumes no responsibility for any damage to the CP6004-RA/-RC or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the CP6004-RA/-RC complies with the thermal considerations set forth in this document.

Appendix A

SATA Flash Module

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A. SATA Flash Module

The CP6004-RA/-RC provides an optional SATA Flash module with up to 64 GB NAND flash memory. The SATA Flash module is connected to the CP6004-RA/-RC via the board-to-board connectors J19 located on the CP6004-RA/-RC and J1 located on the SATA Flash module. The SATA Flash module has been optimized for embedded systems providing high performance, reliability and security.

A.1 Technical Specifications

Table A-1: SATA Flash Module Main Specifications

SATA FLASH MODULE		SPECIFICATIONS
Interface	Board-to-Board Connector	One 34-pin, male, board-to-board connector, J1
Memory	Memory	Up to 64 GB SLC-based NAND flash memory • Built-in full hard disk emulation • Up to 100 MB/s read rate • Up to 90 MB/s write rate
General	Power Consumption	typ. 1.0 W 3.3 V supply
	Temperature Range	Operational: 0°C to +60°C Standard -40°C to +70°C Extended Storage: -55°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	70 mm x 28 mm
	Board Weight	ca. 14 grams

Note ...

Write protection is available for this module. Please contact Kontron for further assistance if write protection is required.

A.2 SATA Flash Module Layout

The SATA Flash module includes one board-to-board connector, J2, for connection to the CP6004-RA/-RC.

Figure A-1: SATA Flash Module Layout (Bottom View)