3U Open VPX Extender Card	**VITA 46 VITA 65**	

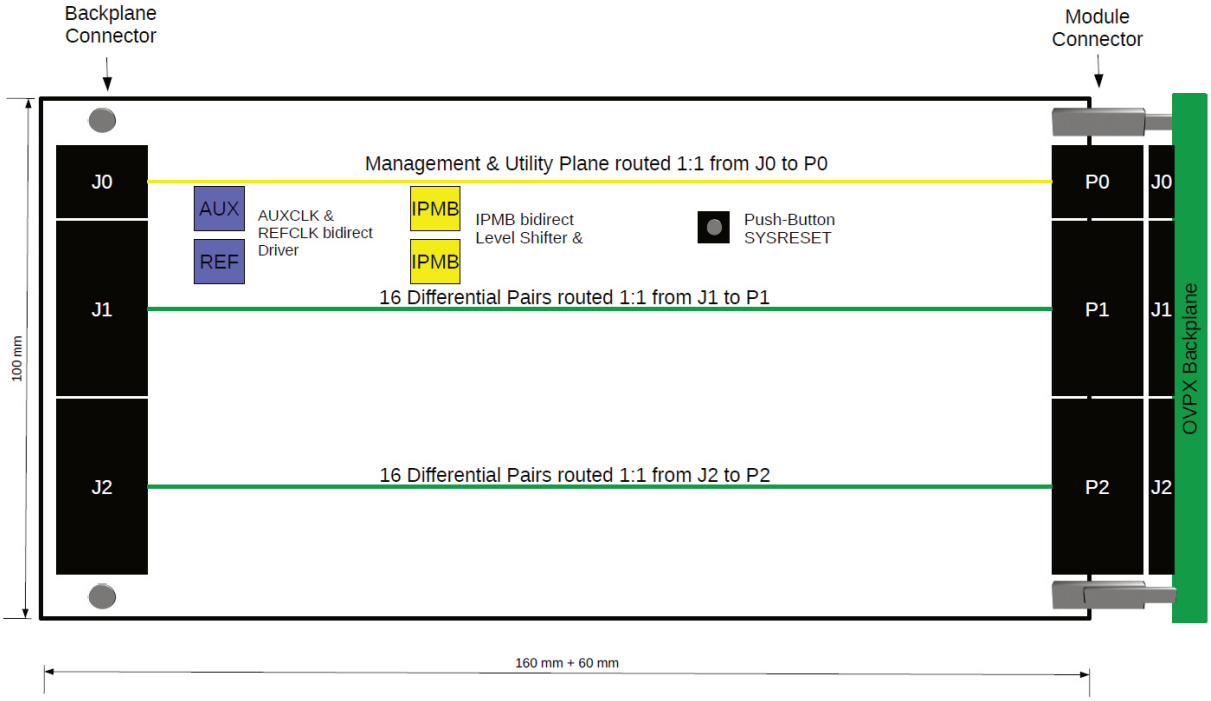
Key features:

- PCIe Gen. 3 Compatible (Extender generates 3.5 dB additive loss. SBC, Backplane and Module have to save 3.5 dB loss as a minimum, according to the specified VPX PCIe Gen.3 loss budget.)
- Data Rates up to 10 Gbit/s
- Access to IPMB-Bus A & B through Level Shifter
- AUX-Clock and REF-CLK Input and output selectable through Dip-Switches
- SYSRESET Push-Button
- Differential Pairs routed from P1 to J1 and from P2 to J2
- Suitable for all slot profiles with differential Connectors (wafer) on P1 and P2
- Available for Conduction Cooled and Air Flow Card Rails

Application

- Test & Development

Block Diagram



Order number:

1H00007411 Air Cooled
1H00007431 Conduction Cooled

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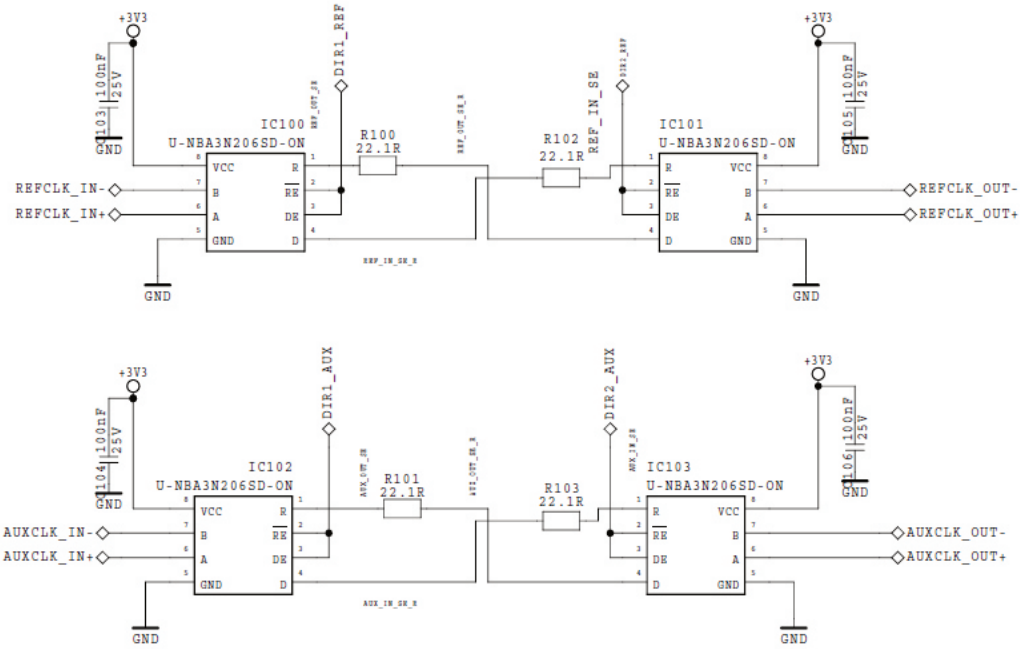
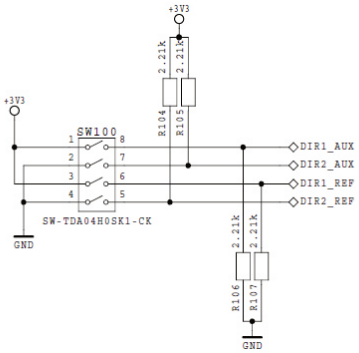
Clock Driver Interface

The VPX REF_CLK and the AUX_CLK can be configured as an output as well as an input to the backplane. The direction of the clock is controlled through Dip-Switch SW100. The table below shows, how the direction of each clock can be selected.



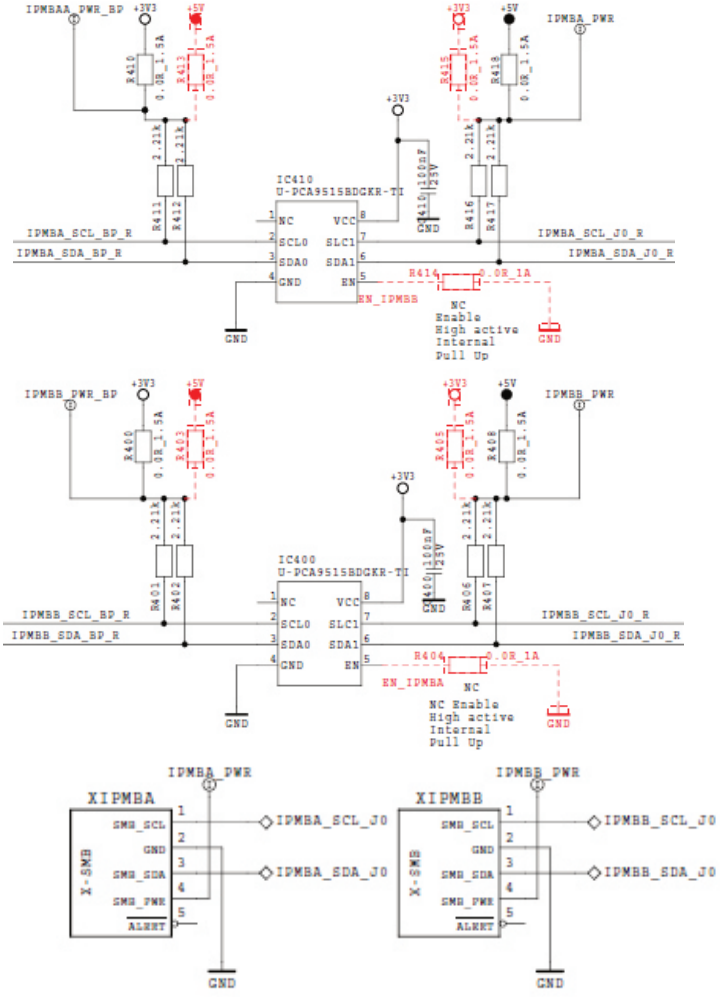
Dip Switch Settings

SW100		
Position [ ]	State "OFF"	State "ON"
1	AUX_CLK is an output to J0 connector	AUX_CLK is an input to P0 connector
2		
3	REF_CLK is an output to J0 connector	REF_CLK is an input to P0 connector
4		



IPMB-Bus Interface

The IPMB-bus can be accessed through IPMB connectors XIPMBA & XIPMBB (Molex, 53398-0510). The IPMB-Bus is level shifted to the P[x] module connectors, as shown in the block diagram. By default, the IPMB-busses at the IPMB connectors are sourced from +5V. The IPMB-busses at the P[x] module connectors are sourced from +3.3V by default. The extract of the schematic below shows the implementation of the IPMB-bus level shifters. The red marked components are not mount on PCB by default. The pull-up voltage resistors can be adopted in order to get the desired voltage translation functionality. Make sure to not short the +3.3V power Rail and the +5V power Rail, by mounting both pull-up voltage transistors on a single IPMB-bus.



SYSRESET Push-Button Switch

The System can be manually reset through pressing switch “SW400”. SW400 is implemented as a momentary push-button switch.
The image below shows the circuit implementation of the SYSRESET# push-button switch.