JILI - JUMPtec Intelligent LVDS Interface

Specification

Rev 2.0
07-April-2003

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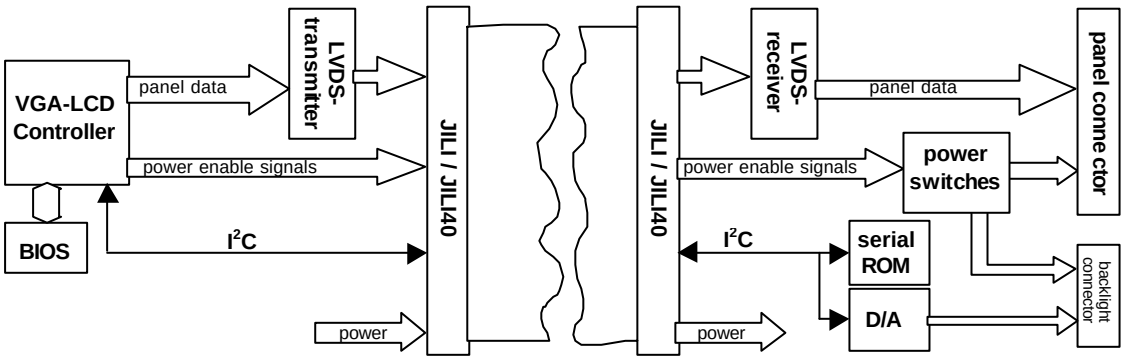
2. Overview

This document describes the JILI flat panel interface in the following order:
- physical definition: connector variants, pinouts...
- hardware definition: data mappings, control signals...
- software definition: configuration protocol, data layouts...



Notes: - LVDS transmitter sometimes located inside the VGA-LCD controller
- LVDS receiver sometimes located inside the flat panel module

The above diagram shows the main elements of a typical JILI system:

- Low Voltage Differential Signaling (LVDS) data transmission
- I2C serial panel cofiguration
- panel specific circuitry located on the adapter

3. Details

3.1 Physical Definition

3.1.1 Connector /Cable Types

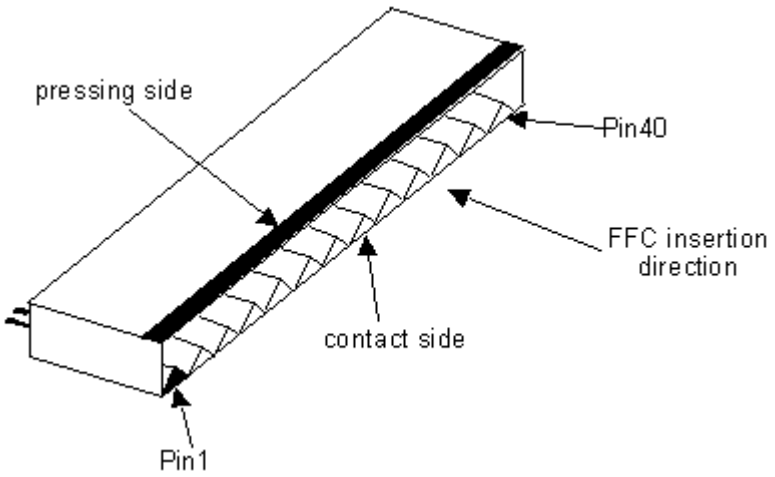
There are currently two JILI implementations:

a.) Standard JILI 40pin, 0.5mm pitch Flat Foil Connection (FFC)

b.) JILI40 40pin, 2mm pitch, double row pin header

a.) Standard JILI

Connector Parameters

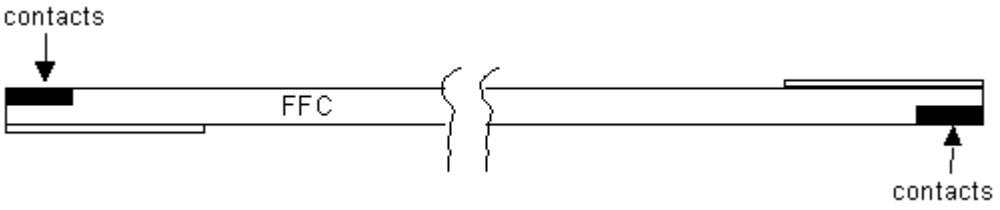


The above drawing should be used to determine pin1 location.
Dependent on different mechanical situations horizontal or vertical types may be used.
The table below lists the reference types:

Manufacturer	description	order no.
HIROSE	SMD flex cable connector, 40 positions, downside contact, pitch 0.5 mm	FH12-40S-0.5SH
HIROSE	SMD flex cable connector, 40 positions, vertical version, pitch 0.5 mm	FH12-40S-0.5SV

Cable Parameters

IMPORTANT NOTE: Since the same pinouts are valid for transmitter- and receiver-side, only FlatFoil cables (FFC) with contacts on opposite sides have to be used ! (see picture below)



side view of FFC

Reference type is:

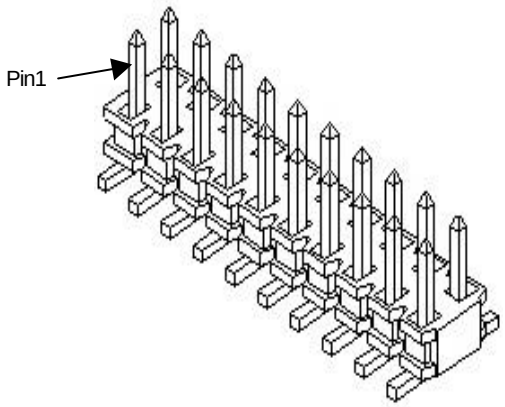
Manufacturer:	description	order no.:
AXON	FlatFoilCable, pitch 0.5mm, length 500mm, contacts on opposite sides	FFC 0.50D40/492L-4-4-08-08 SA

- to achieve low power impedances it is recommended to chose at least 0.1mm conductor thickness.
- cable length should not exceed 50...60cm.
- for longer distances twisted pair wires are recommended.

b**.) JILI40**

JILI40 is intended to be used as a direct panel interface. All signals are "final" and do not need any further processing. It should be implemented when connecting to LVDS panels with discrete wire connectors.

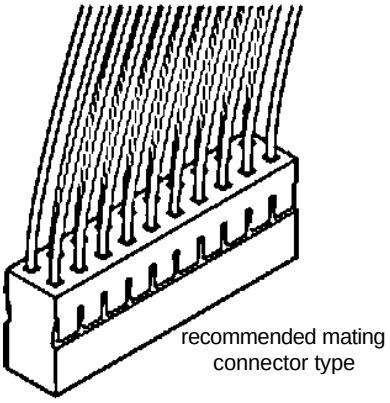
Connector Parameters



- 40 positions, double row, 2mm pitch pin header
- through-hole or smd type
- horizontal or vertical mounting

Reference type is:

Manufacturer:	**description**	**order no.:**
FCI (Berg)	MINITEK, 40 pos.	94270-540



Preferred mating connector is discrete wire type. However: in cases of short cable lengths (20...30cm) standard IDC connectors for ribbon cables may be used.

Cable Parameters

The cable type has to be chosen according to the connector parameters.
In case of longer cables (> 30cm) it is recommended to use twisted pair wires with an impedance of approx. 100R for the LVDS signals.

3.1.2 Pinout

Pin No:	std. JILI	JILI40
1	LCDFLM	SW_BACK / ENABKL
2	LCDDO0	SW_BACK / ENABKL
3	LCDDO1	BRIGHT
4	ENAVDD	LCDDO19
5	LCDDO2	LCDDO18
6	LCDDO3	RESERVED
7	LCDLP	LCDDO17
8	LCDDO4	LCDDO16
9	LCDDO5	RESERVED
10	GND	LCDDO15
11	LCDDO6	LCDDO14
12	LCDDO7	RESERVED
13	GND	LCDDO13
14	LCDDO8	LCDDO12
15	LCDDO9	RESERVED
16	JILI_DAT	LCDDO11
17	LCDDO10	LCDDO10
18	LCDDO11	RESERVED
19	JILI_CLK	LCDDO9
20	LCDDO12	LCDDO8

Pin No:	std. JILI	JILI40
21	LCDDO13	GND
22	DETECT	GND
23	LCDDO14	JILI_CLK
24	LCDDO15	JILI_DAT
25	GND	GND
26	LCDDO16	LCDDO7
27	LCDDO17	LCDDO6
28	GND	GND
29	LCDDO18	LCDDO5
30	LCDDO19	LCDDO4
31	+5V	GND
32	+5V	LCDDO3
33	+5V	LCDDO2
34	+5V	GND
35	ENABKL	LCDDO1
36	BKLGND	LCDDO0
37	BKLGND	GND
38	+12V	GND
39	+12V	SW_VDD
40	+12V	SW_VDD

Signal Descriptions

Signal Name	1 Pixel / Clock LVDS mode	2 Pixel / Clock LVDS mode	1 Pixel / Clock 18Bit RGB mode
LCDDO0	LVD0-	oddLVD0-	RED0
LCDDO1	LVD0+	oddLVD0+	RED1
LCDDO2	LVD1-	oddLVD1-	RED2
LCDDO3	LVD1+	oddLVD1+	RED3
LCDDO4	LVD2-	oddLVD2-	RED4
LCDDO5	LVD2+	oddLVD2+	RED5
LCDDO6	LVDC-	oddLVDC-	GREEN0
LCDDO7	LVDC+	oddLVDC+	GREEN1
LCDDO8	LVD3- (opt.24Bit)	oddLVD3- (opt.24Bit)	GREEN2
LCDDO9	LVD3+ (opt.24Bit)	oddLVD3+ (opt.24Bit)	GREEN3
LCDDO10	-	evenLVD0-	GREEN4
LCDDO11	-	evenLVD0+	GREEN5
LCDDO12	-	evenLVD1-	BLUE0
LCDDO13	-	evenLVD1+	BLUE1
LCDDO14	-	evenLVD2-	BLUE2
LCDDO15	-	evenLVD2+	BLUE3
LCDDO16	-	evenLVDC-	BLUE4
LCDDO17	-	evenLVDC+	BLUE5
LCDDO18	-	evenLVD3- (opt.24Bit)	SHFTCLK
LCDDO19	-	evenLVD3+ (opt.24Bit)	DE
LCDFLM	-	-	VSYNC
LCDLP	-	-	HSYNC
DETECT	(panel hot plug detection)		
JILI_DAT	JILI EEPROM I^2C Data		
JILI_CLK	JILI EEPROM I^2C Clock		
ENAVDD	panel power enable		
-ENABKL	backlight power enable, active low !!!		
GND	power return		
BKLGND	(backlight power return)		
+5V	fixed 5V		
+12V	fixed 12V		
SW_VDD	switched panel power (enabled by ENAVDD)		
SW_BACK	switched backlight power (enabled by ENABKL)		
BRIGHT	backlight brightness control signal		

The 1 pixel/clock 18 Bit TFT mode is based on 3.3V logic level TTL (not LVDS !). Only few JILI implementations support this mode !

3.2 Hardware Definition

3.2.1 Data Mappings

The following table describes the different possible ways flat panel data are multiplexed on the LVDS channels. Some JILI implementations only support a subset of the shown mappings.

LVDS channel	transmiss. order	interface types					
		TFT18	TFT24FPDI	TFT24LDI	TFT36	TFT48FPDI	TFT48LDI
TX10+/-	1	R0	R0	R2	R10	R10	R12
	2	R1	R1	R3	R11	R11	R13
	3	R2	R2	R4	R12	R12	R14
	4	R3	R3	R5	R13	R13	R15
	5	R4	R4	R6	R14	R14	R16
	6	R5	R5	R7	R15	R15	R17
	7	G0	G0	G2	G10	G10	G12
TX11+/-	1	G1	G1	G3	G11	G11	G13
	2	G2	G2	G4	G12	G12	G14
	3	G3	G3	G5	G13	G13	G15
	4	G4	G4	G6	G14	G14	G16
	5	G5	G5	G7	G15	G15	G17
	6	B0	B0	B2	B10	B10	B12
	7	B1	B1	B3	B11	B11	B13
TX12+/-	1	B2	B2	B4	B12	B12	B14
	2	B3	B3	B5	B13	B13	B15
	3	B4	B4	B6	B14	B14	B16
	4	B5	B5	B7	B15	B15	B17
	5	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	6	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
	7	DE	DE	DE	DE	DE	DE
TX13+/-	1	-	R6	R0	-	R16	R10
	2	-	R7	R1	-	R17	R11
	3	-	G6	G0	-	G16	G10
	4	-	G7	G1	-	G17	G11
	5	-	B6	B0	-	B16	B10
	6	-	B7	B1	-	B17	B11
	7	-	-	-	-	-	-
TXCLK1+/-		SCLK	SCLK	SCLK	SCLK	SCLK	SCLK
TX20+/-	1	-	-	-	R20	R20	R22
	2	-	-	-	R21	R21	R23
	3	-	-	-	R22	R22	R24
	4	-	-	-	R23	R23	R25
	5	-	-	-	R24	R24	R26
	6	-	-	-	R25	R25	R27
	7	-	-	-	G20	G20	G22
TX21+/-	1	-	-	-	G21	G21	G23
	2	-	-	-	G22	G22	G24
	3	-	-	-	G23	G23	G25
	4	-	-	-	G24	G24	G26
	5	-	-	-	G25	G25	G27
	6	-	-	-	B20	B20	B22
	7	-	-	-	B21	B21	B23
TX22+/-	1	-	-	-	B22	B22	B24
	2	-	-	-	B23	B23	B25
	3	-	-	-	B24	B24	B26
	4	-	-	-	B25	B25	B27
	5	-	-	-	-	-	-
	6	-	-	-	-	-	-
	7	-	-	-	-	-	-
TX23+/-	1	-	-	-	-	R26	R20
	2	-	-	-	-	R27	R21
	3	-	-	-	-	G26	G20
	4	-	-	-	-	G27	G21
	5	-	-	-	-	B26	B20
	6	-	-	-	-	B27	B21
	7	-	-	-	-	-	-
TXCLK2+/-		-	-	-	SCLK	SCLK	SCLK

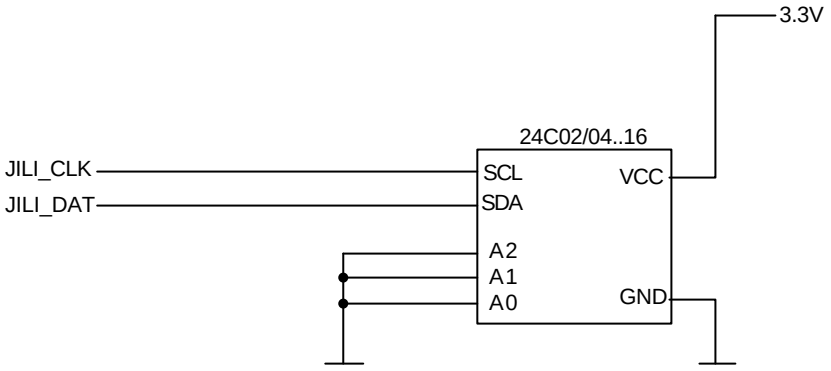
Since the TFT18 mode is common to all JILI implementations, the appropriate transmitter / receiver chipset from National Semiconductor serves as the reference:

Manufacturer:	**description**	**order no.:**
National Semiconductor	18 Bit LVDS FPD Link transmitter	DS90C363
National Semiconductor	18 Bit LVDS FPD Link receiver	DS90CF364

Other Flatpanel LVDS chipset manufacturers are:
- Texas Instruments, LVDS Flat Panel Display, Serdes Family (www.ti.com)
- Thine Semiconductor, THC63LVD series (www.thine.co.jp)

3.2.2 Configuration EEPROM

For detection and configuration of attached panels, JILI uses a standard I²C bus EEPROM.

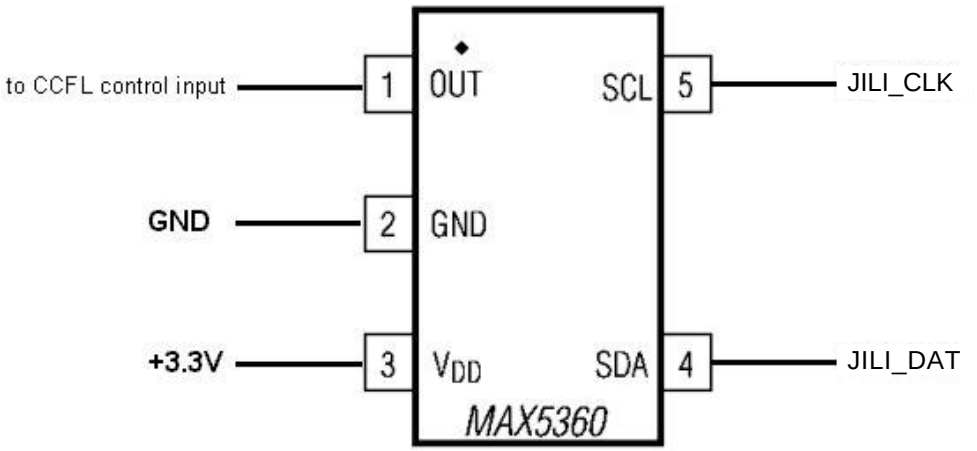


The EEPROM device / circuitry may be selected by the following rules:
- supply voltage: 3.3V
- programming algorithm compatible to FAIRCHILD NM24C16 (Reference type)
- memory size according to configuration file size (see next section).
- tie address pin A0 to VCC for EEPROMS larger than 16kBit (different programming algorithm)
- disable the "Write Protect" pin (if applicable) in order to keep the EEPROM reprogrammable

JILI currently supports the devices:	24C02, 24C04, 24C08, 24C16 at address	A0
	24C32, 24C64 at address	A2

3.2.3 Brightness Control

Full JILI compatible implementations support brightness control (JIDA/JIDA32) when CCFL converters with voltage controlled dimming capability are used.

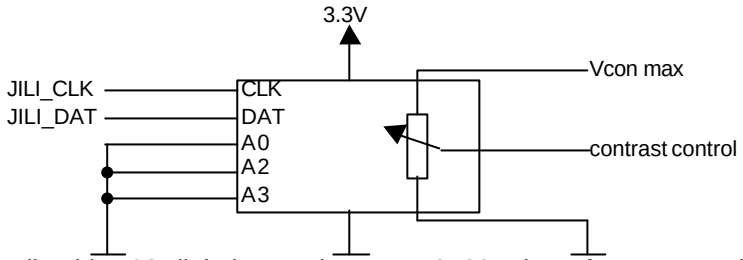


This function is realized by I²C D/A converter MAX5360. The reference type is:

Manufacturer:	**description**	**order no.:**
Maxim	6 Bit I²C D/A converter, Adress 0x62H, 2.7V...5.5V	MAX5362MEUK

3.2.4 Contrast Control

Full JILI compatible implementations support contrast control (JIDA/JIDA32) for STN panels.

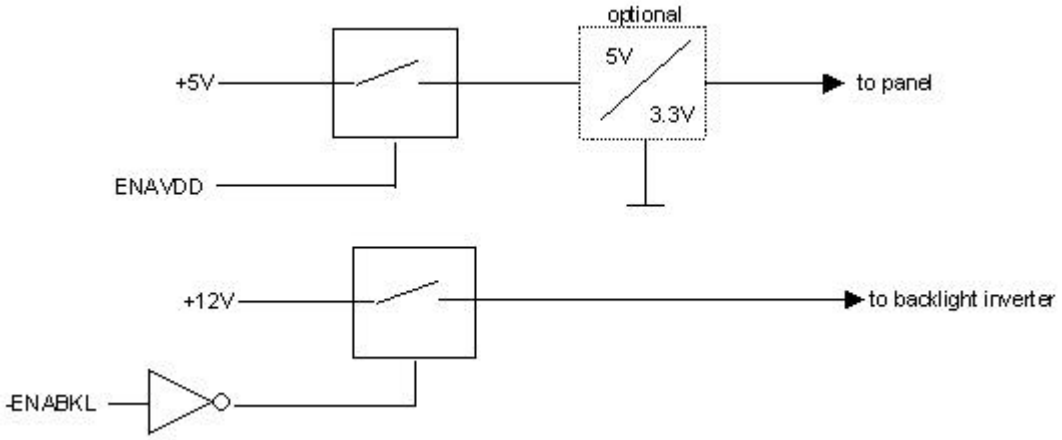


This function is realized by I²C digital potentiometer X9429. The reference type is:

Manufacturer:	**description**	**order no.:**
Xicor	6 Bit I²C digital potentiometer, Adress 0x50H	X9429WV

3.2.5 Power Sequencing

Panel and backlight power supply should be switched in correct order according to panel manufacturer's power sequencing timing. The signals "ENAVDD" and "-ENABKL" serve as the appropriate timing signals:



Please note that the backlight enable signal "-ENABKL" is an active low signal, so an additional inverter may be required.
The max.current on the standard JILI FFC cable is 2A (5V) and 1,5A (12V). If the panel or backlight power exceeds these values an external power supply should be implemented.

3.3 Software Definition

3.3.1 JILI mechanism

During VGA BIOS initialization the I^2C bus is scanned for a configuration EEPROM. A valid JILI implementation is detected by the following header:

offset	mnemonic	content	description	length	format	unit
0000	ROMS	0x55AA	device ROM signature, always 0x55AA	2	const	-
0002	DBID	0xNN	data packet id, see next section	1	const	-
0003	DLNG	0xLLLL	data packet length, reversed byte order	2	ubyte	bytes
0005	CHKS	0xCC	data packet checksum, 8Bit count, 2's complement	1	ubyte	-

The way the next step is executed will be determined by "DBID":

JILI2:

The controller specific registry is stored in the adapter EEPROM. Currently these IDs resp. graphic controllers are defined:

packet ID	description	length (d)
0x01	ATI Rage Mobility M/M1 specific registry	var.
0x02	NSC Geode GX1 specific registry	15 bytes
0x03	VIA VT8603 specific registry	70 bytes
0x04	VIA VT8606 specific registry	66 bytes
0x05	Genesis-Microchip gmZAN1 specific registry	var.
0x06	SMI Lynx EM+ specific registry	var.
0x07	ATI Mobility Radeon M6 specific registry	var.

If correctly detected, the specific registry will be copied from the EEPROM to the BIOS area. Multiple specific registry packets can be merged into the EEPROM in order to support different graphic controllers. The packets have to be placed in their correct ID order.

JILI3:

Controller specific register data are stored in a reserved block of the system BIOS FlashEEPROM, called JILI Data Area (JDA). The register data sets are selected by either "FPID" or "PAID", a 32bit index which is stored in the adapter EEPROM. This data packet is defined below:

packet ID	description	length (d)
0x80	Display Descriptor ID "DDID"	16 / 37 bytes

Display Descriptor format: (mandatory block)

rel.offset	mnemonic	description	length	format	unit	
0000	FPID	flatpanel ID, 32 Bit (MSB always 0)	4 byte	ubyte	-	manda-tory
0004	PAID	panel adapter ID (MSB always 0)	4 byte	ubyte	-	
0008	HSIZE	horizontal diplay size	2 byte	ubyte	pixel	
000A	VSIZE	vertical display size	2 byte	ubyte	pixel	
000C.4-7	PPC	pixel per clock	4 bit	binary	pixel	optional
000C.0-3	RBPP	red bits per pixel	4 bit	binary	pixel	
000D.4-7	GBPP	green bits per pixel	4 bit	binary	pixel	
000D.0-3	BBPP	blue bits per pixel	4 bit	binary	pixel	
000E.4-7	HTILE	horizontal tiles	4 bit	binary	tiles	
000E.0-3	VTILE	vertical tiles	4 bit	binary	tiles	
000F.5-7	ICONF	interface configuration, 0=TTL, 1=FPDI, 2=LDI	3 bit	binary	-	
000F.4	PTYPE	TFT (0) / STN (1) panel type	1 bit	binary	-	
000F.3	SCLKPOL	positive (0) / negative (1) SCLK polarity	1 bit	binary	-	
000F.2	DEPOL	positive (0) / negative (1) DE polarity	1 bit	binary	-	
000F.1	VSPOL	positive (0) / negative (1) VSync polarity	1 bit	binary	-	
000F.0	HSPOL	positive (0) / negative (1) HSync polarity	1 bit	binary	-	

Display Descriptor format: (optional block)

rel.offset	mnemonic	description	length	format	unit	
0010	MAXDCLK	max.dotclock	2 byte	ubyte	10kHz	optional
0012	reserved	-	2 byte	-	-	
0014	MINVCLK	min.vertical sync rate	1 byte	ubyte	Hz	
0015	TYPVCLK	typical vertical sync rate	1 byte	ubyte	Hz	
0016	MAXVCLK	max.vertical sync rate	1 byte	ubyte	Hz	
0017	reserved	-	1 byte	-	-	
0018	MINHTOT	min.horizontal total	2 byte	ubyte	pixel	
001A	MINVTOT	min.vertical total	2 byte	ubyte	lines	
001C	reserved	-	1 byte	-	-	
001D	MINHSW	min.horizontal sync.width	1 byte	ubyte	pixel	
001E	MINVSW	min.vertical sync.width	1 byte	ubyte	lines	
001F	reserved	-	1 byte	-	-	
0020	MINHBP	min.horizontal back porch	1 byte	ubyte	pixel	
0021	MINVBP	min.vertical back porch	1 byte	ubyte	lines	
0022	reserved	-	2 byte	-	-	
0024	JIPAID	JIPA panel id	4 bit	binary	-	

First the BIOS reads the FPID. If a valid ID is found (>0) the JDA is scanned for the matching entry. If available, it is copied to the video BIOS parameters.
If FPID is not defined (=0) or no matching entry was found in the JDA, the PAID is taken instead.
This mechanism is implemented to handle special panel settings which cannot be matched with a standard cable.

The panel parameters inside the Display Descriptor can additionaly be used to calculate the controller registry online if desired.

The Display Descriptor can be merged with the controller specific packets, too. Like mentioned before it has to be put in the ID order, which is the last position currently.

The end of the data packets inside the adapter EEPROM has to be marked by a special ID:

content	description	length (d)
0x00	"EOR": end of ROM signature, always 0x00	1

It is recommended to put a file / revision tag behind the EOR label. Though the BIOS will not handle these data at all, the JILI tools may use them. It should look like this:

[filename (without extension)] / [revision] / [date+initials]

For example: sa202/rev1.0/011015AK
sa202 = filename SA202.JCF
rev1.0 = Revision 1.0
011015AK = 15.10.2001, created by Andreas Kaudel (AK)

3.3.2 Filenames

The configuration file names are built by the below mechanism:

resolution	*interface mode*	*data packet index*	*file index*
Q=320x240	A = 1x18Bit LVDS	01 = ATI Rage Mobility M/M1	
H=640x240	B = 1x24Bit LVDS FPDI	02 = NSC mgx1	
V=640x480	C = 2x18Bit LVDS	03 = VIA VT8603 Twister	
T=854x480	D = 2x24Bit LVDS FPDI	04 = VIA VT8606 Twister-T	
S=800x600	E = 1x18Bit RGB	05 = Genesis-Microchip gmZAN1	
W=1024x600	F = 1x24Bit LVDS LDI	06 = SMI Lynx EM+	
X=1024x768	G = 2x24Bit LVDS LDI	07 = ATI Mobility Radeon M6	
M=1280x768		80 = Display Descriptor	
Y=1600x1024			
E=1280x1024			
P=1400x1050			
U=1600x1200			

For example: VA0101 means: 640x480,1x18Bit LVDS interface, ATI Rage Mobility M/M1

The file index is a simple counter to distinguish between identical panel types with different setting.

4. Document Information

Date	Filename	Author	Changes
18.08.2000	jilid101.doc	A.Kaudel, JUMPtec AG	initial release
30.08.2000	jilid102.doc	A.Kaudel, JUMPtec AG	table 3.2 corrected
07.10.2000	jilid103.doc	A.Kaudel, JUMPtec AG	table 3.3 corrected
14.11.2000	jilid104.doc	A.Kaudel, JUMPtec AG	EEPROM devices changed to 16kbit dev's and to 3.3V in chapter 3.3
15.08.2001	jilim110.doc	A.Kaudel, Dr.Berghaus	changed document name to "jili standard definition" added table "3.1 Interface Configurations" added section "3.3.2 Panel Configuration Files"
18.10.2001	jilim111.htm	A.Kaudel, Dr.Berghaus	HTML formatted added EEPROM reference type added section "3.4 Brightness Control" added section "4.3 Cable Types"
23.01.2002	jilim112.doc	A.Kaudel, Dr.Berghaus	PDF formatted revised table "3.1 Interface Configurations" revised section "3.3.2 Panel Configuration Files"
11.11.2002	jilim113.doc	A.Kaudel, Kontron HH	added "SCLK" in table 3.1.1
07.04.2003	jilim120.doc	A.Kaudel, Kontron HH	completely revised document: changed to Kontron layout added JILI3 mechanism added LDI modes added JILI40 connector FFC reference type corrected added section "contrast control" added filename/revision tag table "filenames" updated