

<b>Related Products</b>	<p>coolMONSTER (LEU2)</p> <p>littleMONSTER2 (LEU2)</p> <p>coolMONSTER/S (LEU3)</p> <p>coolMONSTER/C3 (LEU6)</p> <p>coolMONSTER/P3 (LEU6)</p> <p>coolMONSTER/VE (LEUE)</p> <p>coolMONSTER/VC (LEUE)</p>
<b>Subject</b>	PISA Slot CPU-Boards and problems with PCI add-on cards
<b>Document Name</b>	PISABackplanes_E112.doc
<b>Usage</b>	Common

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## 1. REVISION HISTORY

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<b>Date</b>	<b>Document Name</b>	<b>Subjects added, changed, deleted</b>	<b>Changed by</b>
10-May-02	JAP0062.DOC	Initial release	H. Bruhn
10-May-02	JAP0062.DOC	Add PCI interrupt routing picture	M.Ciolacu
10-May-02	JAP0062.DOC	Add PCI specification 2.2 compliance	G. Vogl
24-May-02	JAP0062.DOC	Add PISA Specification 1.8 information	H. Bruhn
27-May-02	JAP0062.DOC	English proofreading	D. Gunter
10-Dec-02	PISABackplanes_E111.DOC	Reformatted	H. Bruhn
23-Mar-04	PISABackplanes_E112.DOC	Added information about the BIOS-switch solution	H.Bruhn

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## **3. GENERAL INFORMATION AND PROBLEMS**

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**Kontron Embedded Modules GmbH** was the initiator of the industrial bus standard PISA, which is nowadays used all over the world by several single board computer manufacturers. The official PISA specification is available from the **Kontron Embedded Modules GmbH** web pages. When this document was written, the latest version 1.7, released on June 4, 1997, was still the valid base document. There is also a non official release of the PISA specification 1.8 mentioned sometimes. This version holds additional information about the possibility to drive an optional EEPROM placed on the PISA backplane. However this EEPROM is not required on the backplane for the correct function of a PISA system. If compatibility to PISA specification 1.8 is mentioned then this is very good for possible future add-on functionality. However, compatibility to 1.7 spec should nevertheless be guaranteed by a PISA board supplier.

Even though this specification has not changed throughout the last 8 years it looks like some backplanes on the market didn't manage, until now, to follow this official standard. Some others are probably following different standards. We are facing more and more requests from our customers concerning this item, therefore we have written this application note.

If you are using a **Kontron Embedded Modules GmbH** Slot-CPU board in combination with a 3<sup>rd</sup> party PISA-backplane which offers PCI-extension slots, and you are facing problems with PCI extension cards plugged into these slots, these problems may result from an incompatibility of the backplane with the PISA specification. Basically it is the signal routing on the backplane which is different to the specified routing of the PISA's PCI-bus. The details of the technical background will be discussed below.

Nevertheless, it is always recommended to ask the backplane distributor or manufacturer for the information of PISA 1.7 compatibility. Don't use backplanes without PISA compliance.

## 4. PCI-BUS INTERRUPT ROUTING

### 4.1. Introduction

The PCI-bus section of the PISA-bus offers 4 PCI interrupts. On the chipset itself these interrupts are normally called PIRQ0 to PIRQ3, while on the PISA connector these signals are referred to as INT A to INT D. Because the PCI-bus is a plug-and-play system, it is necessary to make sure that a special interrupt routing is done on the backplane. This interrupt routing will ensure that a PCI extension card plugged into one PCI slot will automatically use a different PCI interrupt than a card plugged into another slot. This routing makes sure that the PCI interrupts are distributed in this way.

The system BIOS is configured according to that routing and manages the allocation of the "ISA" interrupts (IRQs) for the corresponding PCI interrupt.

If a backplane that is not following the specified routing is used, several problems may occur. For example: extension cards not recognized, IRQ resources not allocated, PCI-extension card recognized but not working, etc.

### 4.2. Interrupt Routing for PISA backplanes

The PISA specification has a chapter describing the necessary interrupt routing. Here is the table found in the PISA specification 1.7:

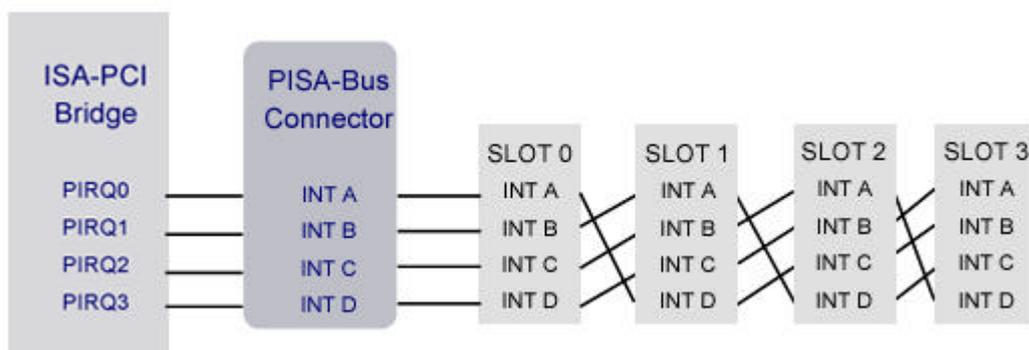
Following interrupt routing on the backplane is recommended for proper bios support:

Backplane Slot	PISA INT A	PISA INT B	PISA INT C	PISA INT D
Slot 1 (AD19)	INT A	INT B	INT C	INT D
Slot 2 (AD20)	INT D	INT A	INT B	INT C
Slot 3 (AD21)	INT C	INT D	INT A	INT B
Slot 4 (AD22)	INT B	INT C	INT D	INT A

e.g. INT B signal of PCI-Slot 3 (IDSEL AD21) has to be routed to signal INT D of the PISA board

This routing is in compliance with PCI specification 2.2 (see chapter 2.2.6, implementation note: interrupt routing).

To give a better understanding of how the routing must look, the following drawing makes the necessary connections visible:



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## **5. BACKPLANES KNOWN TO HAVE NONE PISA ROUTING**

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So far **Kontron Embedded Modules GmbH** is aware that there are at least several backplanes designed by the company ICP that are not PISA specification 1.7 compliant. ICP says that their backplanes and boards are PCISA. We suspect that none of their PCISA products is following the PISA specification and it is not their intention to offer PISA standard products. At this moment we don't know if there are more incompatibilities other than the PCI-interrupt routing.

There may be other companies offering backplanes that are not PISA compliant, even if they are expected to be so. Many companies seem to mix up PISA and PCISA. We don't know if distributors and manufacturers of backplanes give any information, about this possible mix up, to their customers requesting a PISA backplane.

We are very sorry that some **Kontron Embedded Modules GmbH** customers are assuming all products that look like a PISA-board are compatible. This assumption is unfortunately wrong.

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## **6. BIOS SWITCH SOLUTION**

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Kontron Embedded Modules GmbH found a solution to solve at least a few of the incompatibility problems described above. This solution is a BIOS Switch integrated in the system BIOS of some of our PISA-CPU boards. Unfortunately this setup option cannot be integrated into all PISA-CPU board's BIOSes due to space limitations of the onboard BIOS flash ROM.

However, on some PISA-CPU boards of Kontron Embedded Modules GmbH you can set the "PCISA PIRQ Routing" to enabled in the PCI Configuration Submenu of the Advanced Menu (see the product manuals). This enables the PISA-CPU board to function in a backplane with PCISA interrupt routing.

So, whenever you use a PISA compatible backplane leave this switch set to disabled. If you expect your backplane to follow the PCISA interrupt routing, you have to enable this switch.

Nevertheless, if your board still doesn't function correctly with add-on PCI cards, please choose a different backplane where the manufacturer guarantees PISA 1.7 compatibility.

Please note that Kontron Embedded Modules GmbH is not responsible for this incompatibility, produced by companies offering boards and backplanes that are not following PISA 1.7 specification.