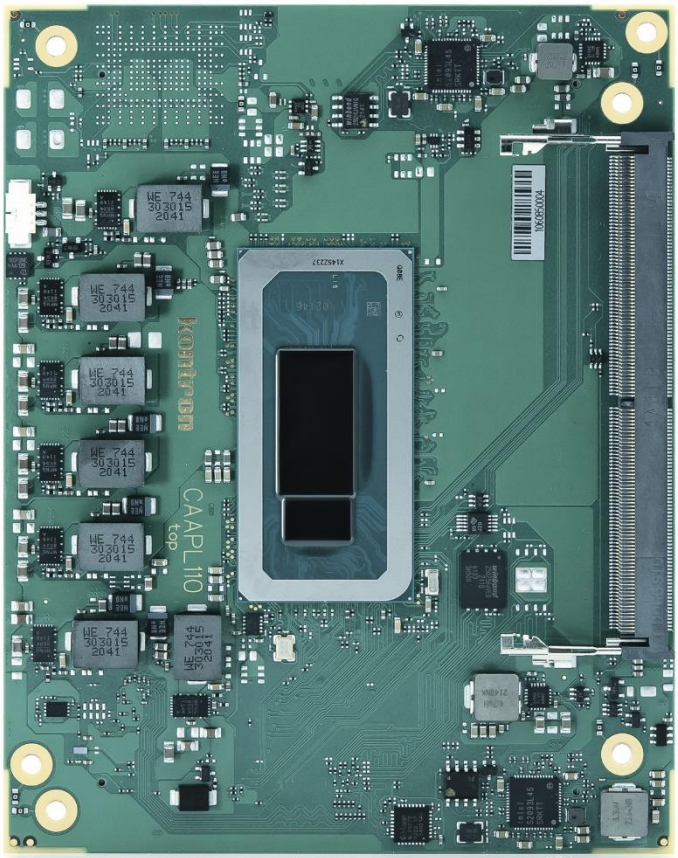
USER GUIDE



COMh-caRP

User Guide Rev. 0.3 Preliminary

kontron

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1. General Information

1.1 Disclaimer

Kontron would like to point out that the information contained in this user guide may be subject to alteration, particularly as a result of the constant upgrading of Kontron products. This document does not entail any guarantee on the part of Kontron with respect to technical processes described in the user guide or any product characteristics set out in the user guide. Kontron assumes no responsibility or liability for the use of the described product(s), conveys no license or title under any patent, copyright or mask work rights to these products and makes no representations or warranties that these products are free from patent, copyright or mask work right infringement unless otherwise specified. Applications that are described in this user guide are for illustration purposes only. Kontron makes no representation or warranty that such application will be suitable for the specified use without further testing or modification. Kontron expressly informs the user that this user guide only contains a general description of processes and instructions which may not be applicable in every individual case. In cases of doubt, please contact Kontron.

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You understand and agree that your use of Kontron devices as a component in High Risk Applications is entirely at your risk. To minimize the risks associated with your products and applications, you should provide adequate design and operating safeguards. You are solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning your products. You are responsible to ensure that your systems (and any Kontron hardware or software components incorporated in your systems) meet all applicable requirements. Unless otherwise stated in the product documentation, the Kontron device is not provided with error-tolerance capabilities and cannot therefore be deemed as being engineered, manufactured or setup to be compliant for implementation or for resale as device in High Risk Applications. All application and safety related information in this document (including application descriptions, suggested safety measures, suggested Kontron products, and other materials) is provided for reference only.

Handling and operation of the product is permitted only for trained personnel within a work place that is access controlled. Follow the “General Safety Instructions” supplied with the product.

You find the most recent version of the “General Safety Instructions“ online in the download area of this product in our Customer Section.

This product is not suited for storage or operation in corrosive environments, in particular under exposure to sulfur and chlorine and their compounds. For information on how to harden electronics and mechanics against these stress conditions, contact Kontron Support.

1.3 Terms and Conditions

Kontron warrants products in accordance with defined regional warranty periods. For more information about warranty compliance and conformity, and the warranty period in your region, visit https://www.kontron.com/terms-and-conditions.

Kontron sells products worldwide and declares regional General Terms & Conditions of Sale, and Purchase Order Terms & Conditions. Visit https://www.kontron.com/terms-and-conditions.

For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

1.4 Customer Support

Find Kontron contacts by visiting: https://www.kontron.com/en/support-and-services.

1.5 Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products. For more details on Kontron’s service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit https://www.kontron.com/en/support-and-services.

1.6 Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron Support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

1.7 Symbols

The following symbols may be used in this user guide of COMh-caRP

simple Box

Info-Box

Important-Box

Alert-Box

Tip-Box

Help-Box

Todo-Box

Download-Box

1.8 For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

1.9 High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product. Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

1.10 Special Handling and Unpacking Instruction

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

1.11 Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

Danger of explosion if the battery is replaced incorrectly.

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer’s instructions.

1.12 General Instructions on Usage

In order to maintain Kontron’s product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account. In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product, then re-pack it in the same manner as it was delivered. Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

1.13 Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit https://www.kontron.com/en/quality-management.

1.13.1 Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

1.13.2 WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with Kontron.

Kontron follows the WEEE directive.

You are encouraged to return our products for proper disposal.

2. Introduction

This user guide describes the COM-HPC® Client Size A Computer-On-Module COMh-caRP made by Kontron and focuses on describing the module's special features. Kontron recommends users to study this user guide before powering on the module.

2.1 Product Naming Clarification

COM-HPC® defines a Computer-On-Module (COM), with all the components necessary for a bootable host computer, packaged as a super component. The product name for Kontron COM-HPC® Computer-On-Modules consists of:

Standard short form	Type	Module size	Processor family identifier	Available temperature variants
COMh-	c=client s=server	a = Size A (95mm x 120mm) b = Size B (120mm x 120mm) c = Size C (160mm x 120mm) d = Size D (160mm x 160mm) e = Size E (200mm x 160mm)	ID = IceLake D AP = AlderLake P AS = AlderLake S etc.	(none=) Commercial Extended (E1) Industrial (E2) Screened industrial (E2S)

Table 1: COM-HPC® Product Naming Clarification

2.2 Product description

The COM-HPC® client module with a 12th Gen Intel® Core™ processor and a size of 95x120mm is perfect for high-performance computing in resource-intensive areas such as networking, automation and measurement. The COMh-caRP features an optimized power-performance ratio with a power consumption of 15 to 45W TDP (Thermal Design Power); in multithreading up to 20 threads can be processed with 14 cores. The module also comes with up to 64GB of DDR5 memory and up to 2.5 Gbit Ethernet. As storage medium, an NVME SSD up to one terabyte can be optionally integrated onboard. The COM-HPC® module also supports USB 4 (display and PCIe 5.0 via USB).

Key features are:

- Up to 64 GByte DDR5 memory
- Up to 2.5Gb Ethernet
- USB 4.0 (Thunderbolt)
- Optional NVMe SSD onboard

2.3 COM-HPC® Documentation

The COM-HPC® specification defines the COM-HPC® module form factor, pinout and signals. For more COM-HPC® specification information, visit the PCI Industrial Computer Manufacturers Group (PICMG®) website.

2.4 COM-HPC® Client Functionality

All Kontron COM-HPC® Client modules contain two 400-pin connector, each of which has 4 rows called A to D on the primary connector and row E to H on the secondary connector. The COM-HPC® Client Computer-on-Module features the following maximum amount of interfaces according to the PICMG module pinout type.

Interface	Client	COMh-caRP
PCIe_REFCLK	2x	2x
PCIe_REFCLK_IN	2x	-
PCIe	49x	24x
NBASE-T	2x	2x
ETH_KR	2x 10/25Gb	-
ETH_KR_CEI	1x	-
USB 2.0	8x	8x
USB 3.2 Gen2x2	2x	2x
USB 4.0	2x	2x
USB C PD I²C	1x	1x
DDI	3x	2x
eDP/DSI	1x	1x
Soundwire/DMIC	1x	1x
I2S	1x	1x
SATA	2x	2x (can be switched to more PCIe)
eSPI	1x	1x
BOOT_SPI	1x	1x
GP_SPI	1x	1x
SMB	1x	1x
I²C	2x	2x
UART	2x	2x
GPIO	12x	12x

Table 2: COM-HPC® Client and COMh-caRP functionality

2.5 COM-HPC® Benefits

COM-HPC® defines a Computer-On-Module (COM), with all the components necessary for a bootable

host computer, packaged as a highly integrated computer. All Kontron COM-HPC® modules are very compact and feature a standardized form factor and a standardized connector layout that carry a specified set of signals. Each COM module is based on the COM-HPC® specification. This standardization allows designers to create a single-system carrier board that can accept present and future COM-HPC® modules. The carrier board designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application, on a carrier board optimally designed to fit a system's packaging. A single carrier board design can use a range of COM-HPC® modules with different sizes and pinouts. This flexibility differentiates products at various price and performance points and provides a built-in upgrade path when designing future-proof systems. The modularity of a COM-HPC® solution also ensures against obsolescence when computer technology evolves. A properly designed COM-HPC® carrier board can work with several successive generations of COM-HPC® modules. A COM-HPC® carrier board design has many advantages of a customized computer-board design and, additionally, delivers better obsolescence protection, heavily reduced engineering effort, and faster time to market.

3. Product specification

3.1 Module Variants

3.1.1 Commercial Grade Modules (0°C to +60°C)

Commercial grade modules (0°C to +60°C) are NOT available as a standard product number. Either use COMh-caAP for commercial grade products or contact your local sales representative to find out more about available commercial temperature variants on a custom base.

3.1.2 Extended temperature Grade Modules (E1, -25°C to 75°C)

Extended temperature grade modules (E1, -25°C to 75°C) are NOT available as a standard product number. Contact your local sales representative to find out more about available extended temperature variants on a custom base.

3.1.3 Industrial Temperature Grade Modules (E2, -40°C to +85°C)

Part Number	Product Name	CPU	Use Case
HCA02-0000-80-7	COMh-caRP E2 i7-13800HRE	i7-13800HRE	industrial
HCA02-0000-60-5	COMh-caRP E2 i5-13600HRE	i5-13600HRE	industrial
HCA02-0000-30-3	COMh-caRP E2 i3-13300HRE	i3-13300HRE	industrial
HCA02-0000-70-7	COMh-caRP E2 i7-1370PRE	i7-1370PRE	industrial
HCA02-0000-50-5	COMh-caRP E2 i5-1350PRE	i5-1350PRE	industrial

Part Number	Product Name	CPU	Use Case
HCA02-0000-20-3	CCOMh-caRP E2 i3-1320PRE	i3-1320PRE	industrial

Table 3: Product Number for Extended temperature (E2, -40°C to +85°C)

3.2 Accessories

Accessories are product specific, COM-HPC® specific or general COMe accessories. For more information, contact your local Kontron Sales Representative or Kontron Inside Sales.

3.2.1 Cooling

Any LGA 1700 cooler can be used for the CPU. In this case please use our X-Bracket for cooler mounting. Alternativly to the available CPU coolers our standard heat spreader can be used, which is available in a threaded and non-threaded (through hole) version.

Kontron PN	Product Name	Description
HCA0A-0000-99-0	COMh-caAP Heat Spreader threaded	Standard COM-HPC Heat Spreader for COMh-caAP with threads
HCA0A-0000-99-1	COMh-caAP Heat Spreader through hole	Standard COM-HPC Heat Spreader for COMh-caAP through hole

Table 4: Cooling Equipment for COMh-caAP/COMh-caRP available from Kontron

3.2.2 Evaluation Carrier

Kontron PN	Product Name	Description
HCT01-0000-10-0	COM-HPC Client Carrier 10mm	COM-HPC Client Carrier with 10mm Connector Height

Table 5: Evaluation Carrier from Kontron

3.2.3 SO-DIMM Memory

Kontron provided NON-ECC memory modules.

Kontron PN	Product Name	Size	ECC	Op. Temperature
97040-0848-CAAP	DDR5-4800 SODIMM 8GB_CCAS	8GB	noECC	0°C to +60°C
97040-1648-CAAP	DDR5-4800 SODIMM 16GB_CCAS	16GB	noECC	0°C to +60°C
97040-3248-CAAP	DDR5-4800 SODIMM 32GB_CCAS	32GB	noECC	0°C to +60°C

Table 6: Memory for COMh-caRP available from Kontron

3.3 Functional Specification

3.3.1 Technical Data

Function	Definition
Compliance	COM HPC Client, Size A
Dimension (H X W)	120mm x 95 mm
Processors	Board comes Intel® 13th generation RaptorLake H/P/U Core® I processors
Chipset	Intel® 600/700 Series Chipset Family - On-Package Platform Controller Hub
Main Memory	2x DDR5 SODIMM dual channel up to 64 GByte non ECC
Graphics Controller	Intel® Iris XeGraphics architecture with up to 96 EUs, 4 Independent Displays (up to 8K)
Displays	DDI1: DP++ DDI2: DP++ DDI3: DP++ eDP
Ethernet Controller	2x Intel® I226
Ethernet	Up to 2x 2.5 Gb Ethernet with TSN support
Storage	2x SATA 6 Gb/s (optional)
Flash On-board	Up to 1 TByte NVMe SSD (on request)
PCI Express	1x 8 PCIe Gen 5.0 (Raptor Lake H-Series, 35-45 W) 2x 4 PCIe Gen 4.0 → 1×4 shared with onboard NVMe 8x PCIe Gen3.0 Optional 1x PCIe for BMC
USB	2x USB 4.0/ Thunderbolt ™; 2x USB 3.2 8x USB 2.0
Serial	2x serial interface (RX/TX only)
Other Features	(G) SPI, SMB, Fast I²C, Staged Watchdog, RTC
Special Features	Trusted Platform Module (TPM) 2.0
Features on Request	vPRO (AMT/TXT/AES Support), up to 3x PCIe x1 additional w/o Ethernet & SATA, NVMe SSD, Fail Save via 2nd SPI Flash
Power Management	ACPI 6.0
Power Supply	8.0 V – 20 V Wide Range, Single Supply Power
BIOS	AMI UEFI
Operating Systems	Windows®10, Linux
Temperature	Commercial temperature: 0 °C to +60 °C operating, -30 °C to +85 °C non-operating Optional E1: -25 °C to +75 °C operating, -30 °C to +85 °C non-operating E2: NA
Humidity	93 % relative Humidity at 40 °C, non-condensing (according to IEC 60068-2-78)

Table 7: Technical Data

3.3.2 Block Diagram

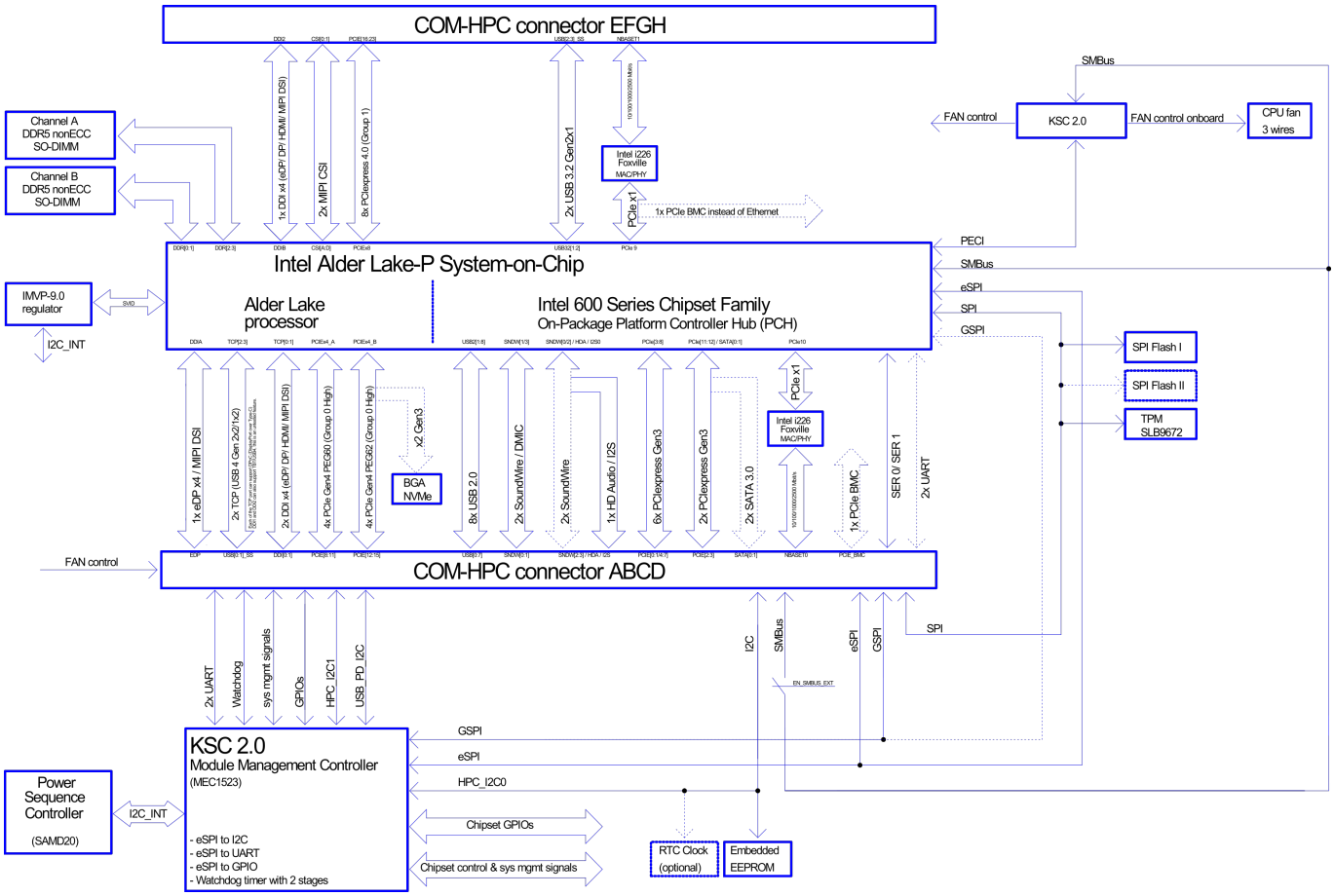

Figure 1: COMh-caRP Blockdiagram

3.3.3 Front Side

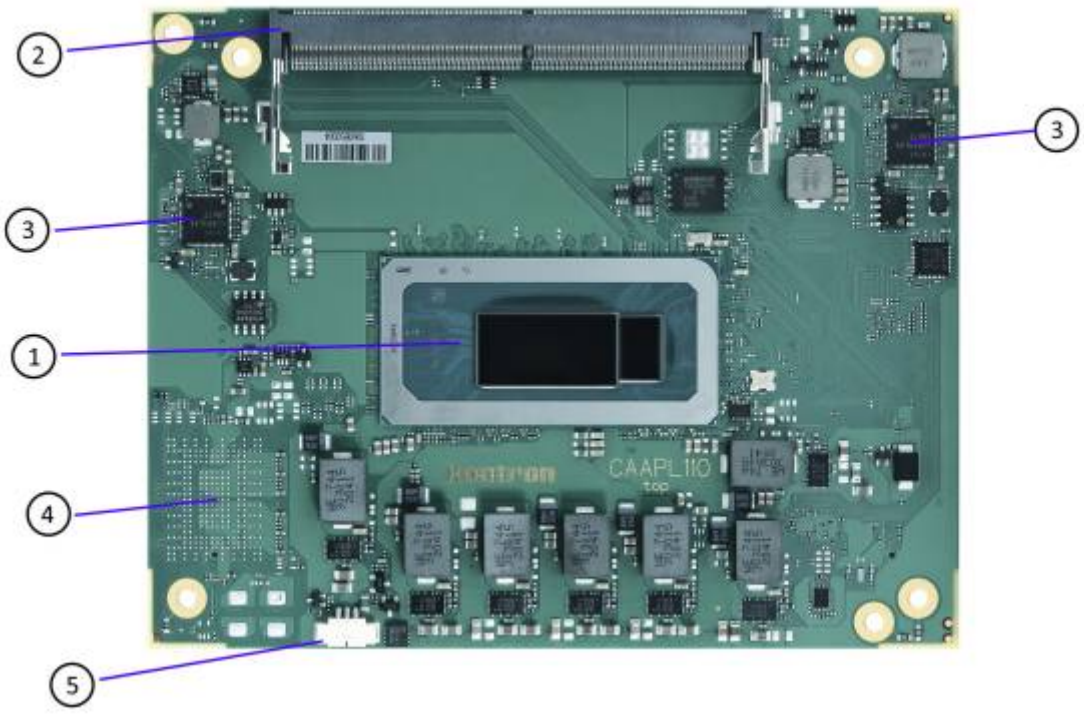

Figure 2: COMh-caRP Front Side

1. CPU and PCH
2. memory socket
3. 2x Ethernet PHY
4. optional NVME
5. 3-pin fan connector

3.3.4 Back Side

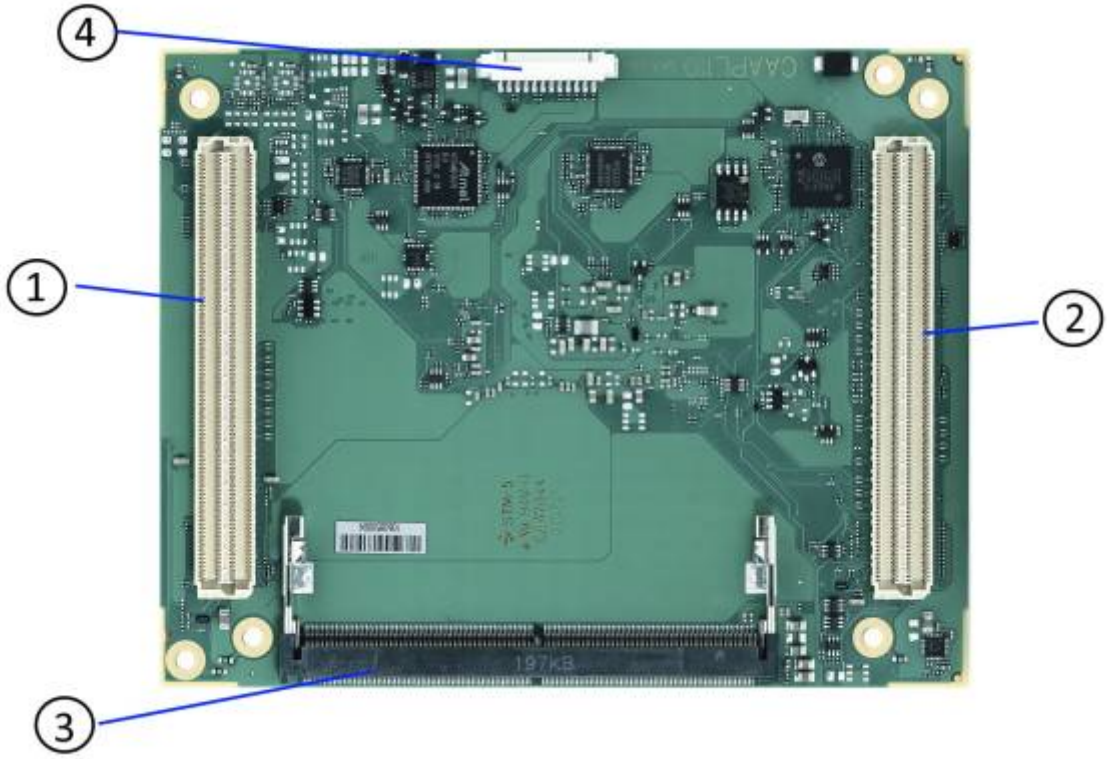

Figure 3: COMh-caRP Back Side

1. COM-HPC® Connector J1
2. COM-HPC® Connector J2
3. DDR5 SO-DIMM memory socket
4. Programming connector for embedded controller

3.3.5 Processor (CPU)

The 13th Gen Intel® Core™ mobile processors combine power efficiency, performance, flexibility, and industrial-grade features to drive success for demanding AI, graphics, and rugged edge use cases. This new generation offers a performance hybrid architecture with up to 14 cores and flexible processor base power from 15W to 45W.
13th Gen Intel Core mobile processors also offer enhanced Intel® Iris® X^e Graphics for fast, power-efficient parallel AI processing and immersive visual experiences. And with industrial-grade features and ruggedized SKUs, this lineup will enable advanced intelligence and real-time performance in the most-challenging environments.

Key features are:

- Intel® 7 process technology
- Up to 14 cores, up to 20 threads in IoT SKUs
- Up to 24 MB Intel® Smart Cache
- Processor base power range of 15W to 45W
- Intel® Iris® X^e Graphics with up to 96 execution units (EUs)
- Support for up to four concurrent displays at up to 4K resolution or one display at 8K resolution
- Pipelock video synchronization for Windows, graphics and display virtualization
- Intel® Deep Learning Boost (Intel® DL Boost) with VNNI instructions
- Up to DDR5-4800; LP5x-6400
- Up to 8 lanes PCIe 4.0 + 8 lanes PCIe 5.0 (H-series) off the CPU, up to 12 lanes PCIe 3.0 off the PCH
- Intel vPro® platform eligible on select SKUs
- Long-life availability
- Windows 10 IoT Enterprise 2021 LTSC, Yocto Project Linux, UEFI, Slim Bootloader
- Thunderbolt™ 4 or USB 4
- Integrated 1GbE port, 2.5GbE discrete LAN
- Support for Intel® TCC/TSN
- IBECC memory
- Extended temperature (-40°C to 100°C Tjmax)

Processor Number	**Processor Cores**	**Number of P-cores**	**Number of E-cores**	**Number of Threads**	**Intel® Smart Cache (L3)**	**P-Core Base Freq (GHz)**	**E-Core Base Freq (GHz)**	**Max P-Core Turbo Freq (GHz)**	**Max E-Core Turbo Freq (GHz)**	**Processor Graphics**	**Number of Execution Units (EUs)**	**Intel vPro® Platform**
Intel® Core™ i7-13800HRE processor	14	6	8	20	24MB	2.5 (@45W) 1.8 (@35W)	1.8	Up to 5.0	Up to 4.0	Intel® Iris® X^e Graphics	96	Yes
Intel® Core™ i5-13600HRE processor	12	4	8	16	18MB	2.7 (@45W) 1.9 (@35W)	1.9	Up to 4.8	Up to 3.6	Intel® Iris® X^e Graphics	80	Yes
Intel® Core™ i3-13300HRE processor	8	4	4	12	12MB	2.1 (@45W) 1.2 (@35W)	1.5	Up to 4.6	Up to 3.4	Intel® UHD Graphics	48	No

Table 8: Processor lineup - 13th Gen Intel® Core™ processors (H-series 45W)

Processor Number	Processor Cores	Number of P-cores	Number of E-cores	Number of Threads	Intel® Smart Cache (L3)	P-Core Base Freq (GHz)	E-Core Base Freq (GHz)	Max P-Core Turbo Freq (GHz)	Max E-Core Turbo Freq (GHz)	Processor Graphics	Number of Execution Units (EUs)	Intel vPro® Platform
Intel® Core™ i7-1370PRE processor	14	6	8	20	24MB	1.9 (@28W) 1.3 (@20W)	1.2	Up to 4.8	Up to 3.7	Intel® Iris® Xe Graphics	96	Yes
Intel® Core™ i5-1350PRE processor	12	4	8	16	12MB	1.8 (@28W) 1.2 (@20W)	1.3	Up to 4.6	Up to 3.4	Intel® Iris® Xe Graphics	80	Yes
Intel® Core™ i3-1320PRE processor	8	4	4	12	12MB	1.7 (@28W) 1.2 (@20W)	1.2	Up to 4.5	Up to 3.3	Intel® UHD Graphics	48	No

Table 9: Processor lineup - 13th Gen Intel® Core™ processors (P-series 28W)

Processor Number	Processor Cores	Number of P-cores	Number of E-cores	Number of Threads	Intel® Smart Cache (L3)	P-Core Base Freq (GHz)	E-Core Base Freq (GHz)	Max P-Core Turbo Freq (GHz)	Max E-Core Turbo Freq (GHz)	Processor Graphics	Number of Execution Units (EUs)	Intel vPro® Platform
Intel® Core™ i7-1365URE processor	10	2	8	12	12MB	1.7 (@15W) 1.2 (@12W)	1.2	Up to 4.9	Up to 3.7	Intel® Iris® Xe Graphics	96	Yes
Intel® Core™ i5-1345URE processor	10	2	8	12	12MB	1.4 (@15W) 1.0 (@12W)	1.1	Up to 4.6	Up to 3.4	Intel® Iris® Xe Graphics	80	Yes
Intel® Core™ i3-1315URE processor	6	2	4	8	10MB	1.2 (@15W) 0.8 (@12W)	0.9	Up to 4.5	Up to 3.3	Intel® UHD Graphics	64	No

Table 10: Processor lineup - 13th Gen Intel® Core™ processors (U-series 15W)

3.3.6 System Memory

The COMh-caRP supports up to 2 x 32 GByte of SODIMM DDR5-4800 non-ECC memory. One SO-DIMM socket is on the top side, on on the bottom side available.

Socket	SO-DIMM DDR5-4800
Memory Type	DDR5-4800 non-ECC
Channels	Dual-channel
Max Memory	Up to 64GByte
Memory Speed	4800 MTs (max)

Table 11: System Memory

One SODIMM memory socket is located on the top side of the module with 8 mm height. The socket may be populated with a DDR5 SODIMM module mounted horizontally. There is another SODIMM memory socket mounted horizontally on the bottom side of the module with 4 mm height.

In general, memory modules have a much lower longevity than embedded motherboards, and therefore the EOL of the memory modules may occur several times during the lifetime of the motherboard. Kontron guarantees to maintain memory modules by replacing EOL memory modules with another qualified similar module. As a minimum, it is recommended to use Kontron memory modules for prototype system(s) in order to prove the stability of the system and as a reference. For volume production, if required, test and qualify other types of RAM. In order to qualify RAM it is recommend to configure three systems running a RAM Stress Test program in a heat chamber at 60°C, for a minimum of 24 hours.

3.3.7 High-Speed Interface Overview

The different variants of the chipset populated on the COMh-caRP offered High-Speed IOs and the following table will give an overview of it.

HSIO Lane#	USB 3.2	PCIe	GbE	SATA	Description
0	USB0_SS0	-	-	-	-
1	USB1_SS0	-	-	-	-
2	-	PCIe 0	-	-	-
3	-	PCIe 1	-	-	-
4	-	PCIe 4	-	-	-
5	-	PCIe 5	-	-	-
6	-	PCIe 6	-	-	-
7	-	PCIe 7	-	-	-
8	-	-	GbE0	-	-
9	-	(optional PCIe BMC)	GbE1	-	-
10	-	(optional PCIe 2)	-	default SATA 0	-
11	-	(optional PCIe 3)	-	default SATA 1	-

Table 12: HSIO Mapping

3.4 Interfaces

3.4.1 PCIe

COM-HPC allows for up to 49 PCIe lanes on the Client Module pin-out, and for up to 65 PCIe lanes on the Server Module. The PCIe lanes are divided into 5 Groups:

- Group 0 Low: PCIe lanes 0:7 and also an additional lane for BMC use
- Group 0 High: PCIe lanes 8:15
- Group 1: PCIe lanes 16:31
- Group 2: PCIe lanes 32:47
- Group 3: PCIe lanes 48:63 (Server Module only)

COMh Group	COMh connector	HSIO Port	Supported Lane Config		
0 Low	PCIe00	USB32_3/PCIe #3	x1	x2	-
	PCIe01	USB32_4/PCIe #4	x1		
	PCIe02	PCIe #11	x1	x2	
	PCIe03	PCIe #12	x1		
	PCIe04	PCIe #5	x1	x2	x4
	PCIe05	PCIe #6	x1		
	PCIe06	PCIe #7	x1	x2	
	PCIe07	PCIe #8	x1		

Table 13: General Purpose PCI Express 3.0 ports

PCIe2 and PCIe3 only available if no SATA is used.

COMh Group	COMh connector	ADL P	Supported Lane Config
0 High	PCIe08	PCIEX4_A_TX/RX_±[0]	x4
	PCIe09	PCIEX4_A_TX/RX_±[1]	
	PCIe10	PCIEX4_A_TX/RX_±[2]	
	PCIe11	PCIEX4_A_TX/RX_±[3]	
	PCIe12 no NVME	PCIEX4_B_TX/RX_±[0]	x4
	PCIe13 no NVME	PCIEX4_B_TX/RX_±[1]	
	PCIe14 no NVME	PCIEX4_B_TX/RX_±[2]	
	PCIe15 no NVME	PCIEX4_B_TX/RX_±[3]	

COMh Group	COMh connector	ADL P	Supported Lane Config
1	PCIe16	PCIEX8_A_TX/RX_±[0]	x8
	PCIe17	PCIEX8_A_TX/RX_±[1]	
	PCIe18	PCIEX8_A_TX/RX_±[2]	
	PCIe19	PCIEX8_A_TX/RX_±[3]	
	PCIe20	PCIEX8_A_TX/RX_±[4]	
	PCIe21	PCIEX8_A_TX/RX_±[5]	
	PCIe22	PCIEX8_A_TX/RX_±[6]	
	PCIe23	PCIEX8_A_TX/RX_±[7]	

Table 14: PCI Express Graphics Gen 5

The PCIEX8 lanes in Group 1 are only available on H-Series SKUs.

Processor PCIEX4_B_* lanes can either be connected to COMh PCIe lanes [12:15] or to the optional onboard NVME Flash.

3.4.2 USB

The COM-HPC Client Module supports up to eight USB 2.0 ports and up to four USB 3.2 Gen 2×2 or USB4 ports. A COM-HPC USB 3.2 Gen 2×2 port may alternatively be used as a USB 3.2 Gen 1 or Gen 2 port as well.
The COM-HPC Server Module supports up to eight USB 2.0 ports, up to two USB 3.2 Gen 1 or Gen 2 ports and up to two USB 3.2 Gen 2×2 ports or USB4 ports. A USB 3.2 Gen 2×2 may be used as a USB 3.2 Gen 1 or Gen 2 port as well.
To realize a COM-HPC USB 3.2 Gen 1, Gen 2, Gen 2×2 or USB4 port, one of the four available USB 2.0 ports from the USB[0:3] pool must be used along with the SuperSpeed pins.

COMh-caRP support up to 8x USB 2.0, 2 USB 4.0 and 2x USB 3.2 Gen 2

To support USB4 on USB0 SS or USB1 SS USB2 ports can not be swapped. USB0 SS has to use USB2 port 0 and USB1 SS has to use USB2 port1. Configuration has to be done in BIOS during build time.

For USB 4.0 following signals are used

COMh connector	ADL P	Description
USB0_SSTX[0:1]±	TCP2_TX[0:1]±	4 Gen 2×2/3×2 (20/40 Gb/s)
USB0_SSRX[0:1]±	TCP2_TXRX[0:1]±	4 Gen 2×2/3×2 (20/40 Gb/s)
USB1_SSTX[0:1]±	TCP3_TX[0:1]±	4 Gen 2×2/3×2 (20/40 Gb/s)
USB1_SSRX[0:1]±	TCP3_TXRX[0:1]±	4 Gen 2×2/3×2 (20/40 Gb/s)
USB0_LS[TX:RX]	TBT_LSX2_[RX:TX]D	sideband TX/RX interface

COMh connector	ADL P	Description
USB1_LS[TX:RX]	TBT_LSX3_[RX:TX]D	sideband TX/RX interface
USB0_AUX±	TCP2_AUX_[P:N]	DisplayPort Aux channel for USB4 DP modes
USB1_AUX±	TCP3_AUX_[P:N]	DisplayPort Aux channel for USB4 DP modes
SML[0:1]_DAT	SML0[CLK:DATA]	SM Link to support Carrier USB4 Re-Timers
SML[0:1]_CLK	SML1[CLK:DATA]	SM Link to support Carrier USB PD Controller
PMCALERT#	GPP_B11/PMCALERT#	Active low Alert signal associated with SML1
USB_RT_ENA	GPP_D3	Power Enable for carrier based USB Re-Timers
USB_PD_I2C_DAT	-	I2C data line between EC and carrier
USB_PD_I2C_CLK	-	I2C clock line between EC and carrier
USB_PD_ALERT#	-	Active low Alert signal from USB PD controller

Table 15: USB 4.0 signals

For USB 3.2 ports following signals are used:

COMh connector	HSIO	Port Description
USB_SS2	USB32_1 3.2	Gen2 x1 (5/10 Gb/s)
USB_SS3	USB32_2 3.2	Gen2 x1 (5/10 Gb/s)

Table 16: USB 3.2 signals

COM-HPC connector	ADL P	Description
USB0	USB2 1	In corresponding with USB_SS0
USB1	USB2 2	In corresponding with USB_SS1
USB2	USB2 3	In corresponding with USB_SS2
USB3	USB2 4	In corresponding with USB_SS3
USB4	USB2 5	-
USB5	USB2 6	-
USB6	USB2 7	-
USB7	USB2 8	-
-	USB2 9	Not used
-	USB2 10	Not used

Table 17: USB 2.0 ports

3.4.5 Graphics Interfaces

COM-HPC Client boards support following graphic interfaces:

Interface	Description
eDP	embedded DisplayPort
DP0	DisplayPort 0
DP1	DisplayPort 1
DP2	DisplayPort 2

Table 18: COM-HPC defined display interfaces

If more than one active display port is connected, then the processor frequency may be lower than base frequency in thermally limited scenarios.

COMh-caRP supports the full range of COM-HPC addressed graphic interfaces. Additionally there is also graphical use of both USB4 interfaces possible.

COMh Port	ADL Port	Remarks
eDP/DSI	DDIA	eDP is default, DSI only with custom version possible
DDI2 (DP++)	DDIB	-
DDI0 (DP++)	TCP0	-
DDI1 (DP++)	TCP1	-
USB4 0	TCP2	-
USB4 1	TCP3	-

Table 19: Display Interfaces on COMh-caRP

3.4.3 SATA

Two SATA links for support of SATA-150 (revision 1.0, 1.5Gb/s), SATA-300 (revision 2.0, 3Gb/s), and SATA-600 (revision 3.0, 6Gb/s) devices are defined, for the Client Module and the Server Module.

3.4.6 Audio Interfaces

COM-HPC Client boards can support following audio interfaces:

- Soundwire
- HD Audio

COMh-caRP use SoundWire DMIC and HDAudio/I2S Interface connect to COMh Connectors. Additionally audio signals are routed to the DP ports. Therefore an extra audio interface is not necessary, if there is audio output only necessary at the displays.

COMh	ADL/RPL P	Description
SNDW_DMIC_DAT0	GPP_S7/SNDW3_DATA/DMIC_DATAA1	Bi-directional PCM audio data
SNDW_DMIC_CLK0	GPP_S6/SNDW3_CLK/DMIC_CLK_A1	Clock for Soundwire transactions
SNDW_DMIC_DAT1	GPP_S3/SNDW1_DATA/DMIC_DATAA0	Bi-directional PCM audio data
SNDW_DMIC_CLK1	GPP_S2/SNDW1_DATA/DMIC_CLK_A0	Clock for Soundwire transactions

Table 20: Soundwire Interface on COMh-caRP

COMh	ADL/RPL P SNDW	ADL/RPL P HDA	ADL/RPL P I2S
I2S_CLK/SNDW_CLK2/HDA_B CLK	SNDW0_CLK	GPP_R0/HDA_BCLK/I2S0_SCLK	
I2S_DIN/SNDW_DAT2/HDA_SDI	SNDW0_DATA	GPP_R3/HDA_SDI0/I2S0_RXD	
I2S_DOUT/SNDW_DAT3/HDA_SDO	SNDW2_CLK	GPP_R2/HDA_SDO/I2S0_TXD	
I2S_LRCLK/SNDW_CLK3/HDA_SYNC	SNDW2_DATA	GPP_R1/HDA_SYNC/I2S0_SFRM	
I2S_MCLK/HDA_RST#	-	GPP_R4/HDA_RST#	I2S_MCLK1_OUT*

*configurable via BIOS option

Table 21: optional Soundwire, HDA and I2S Interface on COMh-caRP

3.4.7 UART

Two 3.3V logic level asynchronous serial ports, designated UART0 and UART1 are defined by COM-HPC. Each port has TX and RX signals for data use and RTS# and CTS# signals for optional handshake / flow control use. For logic level use, the TX and RX signals are active high and the RTS# and CTS# signals are active low. Some data sheets omit the trailing '#' signal but the logic level handshake signals are active low nonetheless. The idle state, or 'mark' state, of the logic level TX line is high, or 3.3V in the COM-HPC case.
These ports may be used directly as logic level asynchronous serial connections between COM-HPC Module and Carrier based devices, or between COM-HPC Module and Carrier based mezzanine devices such as certain Mini-PCIe or M.2 cards. Care has to be taken that the logic I/O levels match up.

The UART interface on COMh-caRP is by default driven from the embedded controller. It can be reconnected on a custom version to the PCH's UART.

COMh	EC (Default)	PCH (Optional)
UART0_TX	UART0_TX	GPP_H11/UART0_TXD
UART0_RX	UART0_RX	GPP_H10/UART0_RXD
UART0_RTS#	UART0_RTS#	GPP_H13/UART0_CTS#
UART0_CTS#	UART0_CTS#	GPP_H12/UART0_RTS#
UART1_TX	UART1_TX	GPP_D18/UART1_TXD
UART1_RX	UART1_RX	GPP_D17/UART1_RXD
UART1_RTS#	UART1_RTS#	-
UART1_CTS#	UART1_CTS#	-

Table 22: UART interface on COMh-caRP

3.4.8 General Purpose SPI interface

COM-HPC Client and Server modules can support a General Purpose SPI interface (GP_SPI) to connect multiple peripherals.

The COMh GP_SPI interface on COMh-caRP is handle by the embedded controller. There is an option to handle it by PCH as well.

EC	PCH (Optional)	COMh
EC_GP_SPI_CLK	PCH_GP_SPI_CLK	GP_SPI_CLK
EC_GP_SPI_MOSI	PCH_GP_SPI_MOSI	GP_SPI_MOSI
EC_GP_SPI_MISO	PCH_GP_SPI_MISO	GP_SPI_MISO
EC_GP_SPI_CS0#	PCH_GP_SPI_CS0#	GP_SPI_CS0#
EC_GP_SPI_CS1#	PCH_GP_SPI_CS1#	GP_SPI_CS1#
EC_GP_SPI_CS2#	-	GP_SPI_CS2#
EC_GP_SPI_CS3#	-	GP_SPI_CS3#
EC_GP_SPI_ALERT#	-	GP_SPI_ALERT#

Table 23: GP-SPI on COMh-caRP

3.4.9 Boot SPI

The Boot SPI interface is used to support loading all or parts of the system BIOS from a Module or Carrier based SPI (Serial Peripheral Interface) or SQI (Serial Quad Interface) flash device. The SPI or SQI flash device can be up to 64 MB (512 Mb). Two flash devices may be used on the Module, allowing up to 128 MB of boot code storage on the Module. Alternatively there may be a flash device on the Carrier and / or on the Module, for a combined total of up to 128 MB. In most situations, only one flash device, either on the Module or on the Carrier, is used.

Alder Lake/Raptor Lake SPI0 is routed to COMh connector. This interfaces supports serial flash (for BIOS firmware) and TPM being attached to it only.

COMh	Signal PCH Pin	Description
BOOT_SPI_CS#	SPI0_CS0#	Chip select for Carrier Board SPI
BOOT_SPI_IO0	SPI0_MOSI	Bidirectional data path for Carrier SPI flash
BOOT_SPI_IO1	SPI0_MISO	Bidirectional data path for Carrier SPI flash
BOOT_SPI_IO2	SPI0_IO2	Bidirectional data path for Carrier SPI flash
BOOT_SPI_IO3	SPI0_IO3	Bidirectional data path for Carrier SPI flash
BOOT_SPI_CLK	SPI0_CLK	Clock from Module chipset to Carrier SPI
VCC_BOOT_SPI	-	connected to V_3V3_S5
BSEL0	-	Boot select pins. These pins distinguish between a SPI or eSPI BIOS boot and between an on-Module or off-Module BIOS. Passed through KSC
BSEL1	-	
BSEL2	-	

Table 24: Boot SPI interface on COMh-caRP

COMh-caRP supports on-module and external carrier boot from SPI. COMh signals BSEL[1:3] can be used to select the desired boot source (see table below)

BSEL			eSPI_CS1#	eSPI_CS0#	SPI_CS1#	SPI_CS0#	Boot option	Description
0	1	2						
1	1	1	Carrier	Module	Module	Module	MAFS	BIOS on SPI0 or SPI1 on Module
1	1	0	Carrier	Module	Module	Carrier	MAFS	BIOS on SPI0 on Carrier or on SPI1 on Module
1	0	1	Carrier	Module	Carrier	Module	MAFS	BIOS on SPI0 on Module or on SPI1 on Carrier
1	0	0	-	-	-	-	-	Not used
0	1	1	Module	Carrier	Module	Module	MAFS	BIOS on SPI0 or SPI1 on Module
0	1	0	Module	Carrier	Module	Module	SAFS	BIOS on Carrier SAFS
0	0	1	Module	Carrier	Module	Module	SAFS	BIOS on Carrier SAFS
0	0	0	-	-	-	-	-	Not used

Table 25: BIOS Boot options on COMh-caRP

eSPI + SAFS configurations are not yet supported on COMh-caRP.

Following Flash Devices are supported by the BIOS:

- W25Q256JVEIQ
- S25FL256LAGNFI010
- MX25L25645GZ2I
- MT25QL256ABA1EW9-0SIT

3.4.10 eSPI

COM-HPC supports an eSPI port for general purpose I/O. The eSPI interface (like LPC before it) can be useful for general purpose devices such as Carrier Super I/O devices, Carrier CPLDs or FPGAs, hardware monitoring devices, and others. It is also possible to boot the BIOS over eSPI. The eSPI bus runs from a 1.8V supply. COM-HPC does not support LPC.

Booting from eSPI is not yet supported on COMh-caRP. Using eSPI devices on the carrier will require a customized BIOS version.

3.4.11 I2C

The internal I2C bus transfers data between components on the same module and the external I2C bus transfers data between I2C devices connected on the bus. The Fast I2C bus transfers data with rates up to 400 kHz. To change the I2C bus speed, in the BIOS setup menu select:

Advanced>Miscellaneous>I2C Speed> 400 kHz to 1 kHz

The default speed is 200 kHz.

3.4.12 GPIO

The COMh-caRP offers GPIO pins on the dedicated pins of COM-HPC®. The type of termination resistor used sets the direction of the GPIO; where GPI terminations are pull-up resistors, and GPO terminations are pull-down resistors.
Due to the fact that both the pull-up and pull-down termination resistors are weak, it is possible to override the termination resistors using external pull-ups, pull-downs or IOs. Overriding the termination resistors means that the GPIO pins can be considered as bi-directional since there are no restrictions whether you use the available GPIO pins in the in-direction or out-direction.

3.4.13 SMB

The System Management Bus (SMB) is a simple 2-wire bus for low-speed system management communication. The PCH or the SOC controls the SMB. The module’s SMB connects typically to the memory and the hardware controller.

3.5 Features

3.5.1 ACPI Power States

ACPI enables the system to power down, save power when not required (suspend) and wake up when required (resume).
ACPI controls the power states S0-S5, where S0 has the highest priority and S5 the lowest priority.

S0	Working state
S1	Sleep (typically not supported anymore)
S2	Deep Sleep (typically not supported anymore)
S3	Suspend-to-RAM
S4	Suspend-to-disk / Hibernate
S5	Soft-off state

Table 26: ACPI Power States Function

Not all ACPI defined power states are available.
The COMh-caRP supports ACPI 6.0 and the power states only.

Systems that support the low-power idle state do not use power states S3 and S4.

To power on from states S3, S4 and S5 use

- Power Button
- WakeOnLAN (S3, S4)

The OS must support wake up from an USB device and the carrier board must power the USB port with the standby voltage.

3.5.2 Embedded Controller - Hardware Monitor

The embedded controller (EC) provides a broad set of functionality:
- monitoring the module’s processor temperature, power supply voltages (VCC /5 VSB), battery voltage V_BAT
- monitoring and configuring the on-board and external fans
- acting as hub or super-IO for low speed interfaces such as UART, I2C/SMB, GSPI, GPIO
- supporting watchdog functions

The EC is accessible through the API in the Board Support Package.

3.5.3 TPM

Trusted Platform Module is a BOM Option with the Infineon SLB9672 connected to SPI.

3.5.4 Watchdog

The watchdog timer interupt (WD_OUT) is a hardware or software timer implemented by the module to the carrier board if there is a fault condition in the main program; the watchdog triggers a system reset or other corrective actions after a specific time, with the aim to bring the system back from a non-responsive to normal state.

The COMh-caRP supports an independently programmable watchdog that works with two stages that can be used stage by stage.

No action	Stage is off and will be skipped
Reset	Restarts the module and starts a new POST and operating system
Delay → No action	Might be necessary when an operating system must be started and the time for the first trigger pulse must be extended. Only available in the first stage!

WD_OUT only	Triggers WD_OUT pin on the carrier board connector only
Reset + WD_OUT	
Delay + WD_OUT → No action	

Table 27: Dual Staged Watchdog Timer - Time-Out Events

Watchdog Time-out

The COMh-caRP has 2 signals interfering with the watchdog.
WD_STROBE# is an input to trigger the watchdog timer. Periodic strobing prevents the watchdog, if enabled, from timing out.
WD_OUT is an output indicating that a watchdog time-out event has occurred, when the setting activates this signal.

COM-HPC	EC	Description
WD_OUT	GPIO036	Passed through Embedded Controller. Output indicating that a watchdog time-out event has occurred.
WD_STROBE#	GPIO035	Passed through Embedded Controller. Strobe input to watchdog timer.

Table 28: Watchdog signal on COM-HPC connector

3.5.5 Real-Time Clock (RTC)

The RTC keeps track of the current time accurately. The RTC's low power consumption enables the RTC to continue operation and keep time using a lower secondary source of power while the primary source of power is switched off or unavailable.
The COMh-caRP supports typical RTC values of 3 V and less than 10 µA. When powered by the main power supply on-module regulators generate the RTC voltage, to reduce RTC current draw. The RTC's battery voltage range is 2.8 V to 3.47 V.

It is not recommended to run a system without a RTC battery on the carrier board. Even if the RTC battery is not required to keep the actual time and date when main power is off, a missing RTC battery will cause other side effects such as longer boot times. Intel processor environments are generally designed to rely on RTC battery voltage.

3.5.6 NVME

On some COM-HPC modules a PCIe NVMe NAND Flash SSD (with a capacity up to 1TB) can be populated optionally.

On COMh-caRP a PCIe NVMe NAND Flash SSD (with a capacity up to 1TB) can be populated optionally, connected to the PCIEX4_B[0:3] lanes instead of COMh PCIe[12:16] lanes.

There are different types of NVMe SSDs available from different vendors.
For further information on offered resp. released types and their particular feature set, contact Kontron Support.

3.5.7 Features on Request

- NVME can be equipped
- 2nd SPI BIOS flash on-module for failover (not implemented on Standard Modules)
- Rapid Shutdown circuit (not implemented on Standard Modules)

3.6 Electrical Specification

The module powers on by connecting to a carrier board via the COM-HPC interface connectors. The COM-HPC interface connector pins on the module limit the amount of power received.

Before connecting the module's interface connector to the carrier board's corresponding connector, ensure that the carrier board is switched off and disconnected from the main power supply. Failure to disconnect the main power supply could result in personal injury and damage to the module and/or carrier board.

Observe that only trained personnel aware of the associated dangers connect the module, within an access controlled ESD-safe workplace

3.6.1 Power Supply Specification

The power specification of the module supports a supply voltage of 12 V. Other supported voltages are 5 V standby and 3.3 V RTC battery input

Supply Voltage (VCC)	12 V ± 5% COMh-caRP: Widerange Input 8V - 20V
Standby Voltage (VCC_5V_SBY)	5 V ± 5% - Note: Standby voltage is not mandatory for operation
RTC Voltage (VCC_RTC)	2.8 V to 3.47 V

Table 29: Electrical Specification

Only connect to an external power supply delivering the specified input rating and complying with the requirements of Safety Extra Low Voltage (SELV) and Limited Power Source (LPS) of UL/IEC 60950-1 or (PS2) of UL/IEC 62368-1.

To protect external power lines of peripheral devices, make sure that the wires have the right diameter to withstand the maximum available current and the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN 62368-1.

If any of the supply voltages drops below the allowed operating level longer than the specified hold-up time, all the supply voltages should be shut down and left OFF for a

time long enough to allow the internal board voltages to discharge sufficiently.
If the OFF time is not observed, parts of the board or attached peripherals may work incorrectly or even suffer a reduction of MTBF. The minimum OFF time depends on the implemented PSU model and other electrical factors and must be measured individually for each case.

Power Supply Voltage Rise Time

The input voltage rise time is 0.1 ms to 20 ms from input voltage ≤10% to nominal input voltage. To comply with the ATX specification there must be a smooth and continuous ramp of each DC input voltage from 10 % to 90 % of the DC input voltage final set point.

Power Supply Voltage Ripple

The maximum power supply voltage ripple and noise is 200 mV peak-to-peak measured over a frequency bandwidth of 0 MHz to 20 MHz. The voltage ripple, must not cause the input voltage range to be exceeded.

Power Supply Inrush Current

The maximum inrush current at 5 V standby is 2 A. From states G3 (module is mechanically completely off, with no power consumption) or S5 (module appears to be completely off) to state S0 (module is fully usable) the maximum inrush current meets the SFX Design Guide.

3.6.2 Power Management

The Advanced Configuration and Power Interface (ACPI) 6.0 hardware specification supports features such as power button and suspend states. The power management options are available within the BIOS set up menu: **Advanced>ACPI Settings>**

Suspend States

If power is removed, 5V can be applied to the V_5V_SBY pins to support the ACPI suspend-states:

- Suspend to RAM (S3)
- Suspend to Disk (S4)
- Soft-off (S5)

If power is removed, the wake-up event (S0) requires 12V VCC to power on the module for normal operation.

Power Supply Control Signals

Power supply control settings are set in the BIOS and enable the module to shut down, reset and wake from standby.

COM-HPC Signal	Pin	Description
Power Button (PWRBTN#)	B02	A PWRBTN# falling edge signal creates power button event (50 ms ≤ t < 4 s, typical 400 ms) at low level). Power button events can be used to bring a system out of S5 soft-off and other suspend states, as well as powering the system down. Pressing the power button for at least four seconds turns off power to the module Power Button Override.
Power Good (VIN_PWR_OK)	C06	Indicates that all power supplies to the module are stable within specified ranges. PWR_OK signal goes active and module internal power supplies are enabled. PWR_OK can be driven low to prevent module from powering up until the carrier is ready and releases the signal. PWR_OK should not be deactivated after the module enters S0 unless there is a power fail condition.
Reset Button (RSTBTN#)	C02	Reset button input. The RSTBTN# may be level sensitive (active low) or may be triggered by the falling edge of the signal. There are some situations in which it is desirable for a sustained low state of the RSTBTN# to keep the CPU Module unit in a reset condition. This situation comes up with large Carrier or module based FPGAs that need more time to be loaded and configured than the CPU boot time allows. Therefore, COM-HPC Module designs should either keep the CPU Module in a reset state while RSTBTN# is low, or they should pause the boot process in an early state while RSTBTN# is low. This can be done by the Module BIOS monitoring the RSTBTN# line through an I/O port. The BIOS should be paused in an early point, before PCIe and USB enumerations take place. Additionally, the Module PLTRST# signal (below) should not be released (driven or pulled high) while the RSTBTN# is low. For situations when RSTBTN# is not able to reestablish control of the system, VIN_PWR_OK or a power cycle may be used.
Platform Reset (PLTRST#)	A12	Platform Reset: output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. PLTRST# should remain asserted (low) while the RSTBTN# is low.
Suspend to RAM (SUS_S3#)	B08	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board should be used to enable the non-standby power on a typical ATX supply. Even in single input supply system implementations (AT mode, no standby input), the SUS_S3# Module output should be used disable any Carrier voltage regulators when SUS_S3# is low, to prevent bleed leakage from Carrier circuits into the Module.
Suspend to Disk (SUS_S4_S5#)	C08	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.
Suspend Clock (SUS_CLK)	A87	32.768 kHz +/- 100 ppm clock used by Carrier peripherals such as M.2 cards in their low power modes.
PCIe Wake UP (WAKE0#)	D10	PCI Express wake up signal.

COM-HPC Signal	Pin	Description
GP Wake UP (WAKE1#)	D11	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.
Battery Low (BATLOW#)	A11	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.
Lid detection (LID#)	B45	LID switch. COM-HPC/Client only: Low active signal used by the ACPI operating system for a LID switch.
Sleep button (SLEEP#)	B46	Sleep button. COM-HPC/Client only: Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.
Tamper Signal (TAMPER#)	B06	Tamper or Intrusion detection line on VCC_RTC power well. Carrier hardware pulls this low on a Tamper event.
No power (AC_PRESENT)	D34	Driven hard low on Carrier if system AC power is not present.
Resume Reset (RSMRST_OUT#)	B86	This is a buffered copy of the internal Module RSMRST# (Resume Reset, active low) signal. The internal Module RSMRST# signal is an input to the chipset or SOC and when it transitions from low to high it indicates that the suspend well power rails are stable. USB devices on the Carrier that are to be active in S5 / S3 / S0 should not have their 5V supply applied before RSMRST_OUT# goes high. RSMRST_OUT# shall be a 3.3V CMOS Module output, active in all power states.

Table 30: Power Supply Control Signals

3.7 Thermal Management

3.7.1 Heatspreader Plate Assembly

A heatspreader plate assembly is available from Kontron for the COMh-caRP. The heatspreader plate assembly is NOT a heat sink. The heatspreader plate transfers heat as quickly as possible from the processor using a copper core positioned directly above the processor and a Thermal Interface Material (TIM). The heatspreader plate is factory prpared with a TIM screen printed on the contacts and may be fasten to the module without additional user actions.
The heatspreader plate works as a COM-HPC standard thermal interface and must be used with a heat sink or external cooling devices to mainten the heatspreader plate at proper operating temperatures. Unter worst-case conditions, the cooling mechanism must maintain an ambient air and heatspreader plate temperature on any spot of the heatspreader's surface according the module's specification:

- 60°C for commercial temperature grade modules
- 75°C for extended temperature grade modules (E1)
- 85°C for industrial temperature grade modules (E2)

3.7.2 Active/Passive Cooling Solutions

Both active and passive thermal management approaches can be used with the heatspreader plate. The optimum cooling solution depends on the aaplication and environmental conditions. Kontron's active or passive cooling solutions are designed to cover the power and thermal dissipation for a commercial temperature range used in housing with a suitable airflow.

3.7.3 Operating with Kontron Heatspreader Plate (HSP) Assembly

The operating temperature requirements are:

- Maximum ambient temperature with ambient being the air surrounding the module
- Maximum measurable temperature on any part on the heatspreader's surface

Temperature Grade	Requirements
Commercial Grade	at 60°C HSP temperature on MCP @100% load; needs to run at nominal frequency
Extended Grade(E1)	at 75°C HSP temperature the MCP @ 75% load; is allowed to start throttling for thermal protection
Industrial Grade (E2)	at 85°C HSP temperature the MCP @ 50% load; is allowed to start throttling for thermal protection

Table 31: Heatspreader Temperature Specification

3.7.4 Operating without Kontron Heatspreader Plate (HSP) Assembly

The operating temperature is the maximum measurable temperature on any spot of the module's surface.

3.7.5 Temperature Sensors

The modules's processor is capable of reading its internal temperature. The on-module Hardware Monitor (HWM), located in the board management controller KSC20, uses an on-chip temperature sensor to measure the modules's temperature on the board.

Figure 4: Module Temperature Sensor

1. Temperature Sensor in Board Management Controller

3.7.6 On-Module Fan Connector

The module's fan connector powers, controls and monitors an external fan. To connect a standard 3-pin connector fan to the module, use Kontron's fan cable, KAB-HSP 200 mm (96079-0000-00-0).

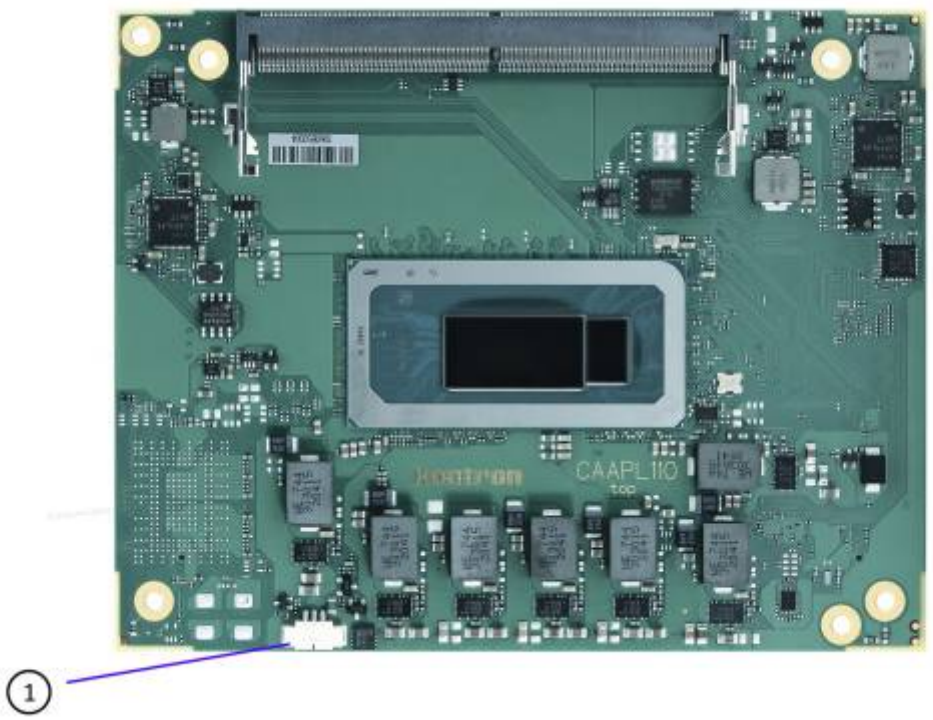

Figure 5: On-module fan connector

Pin	Signal	Description	Type
1	Fan_Tach_IN#	Fan input voltage from COMe connector	Input
2	V_FAN	12 V ±10% (max.) across module input range	PWR
3	GND	Power GND	PWR

Table 32: Fan Connector (3-Pin) Pin Assignment

Always check the fan specification according to the limitations of the supply current and supply voltage.

3.8 Mechanical Specification

The COMh-caRP is compatible with the COM-HPC® mechanical specification.

3.8.1 Module Dimensions

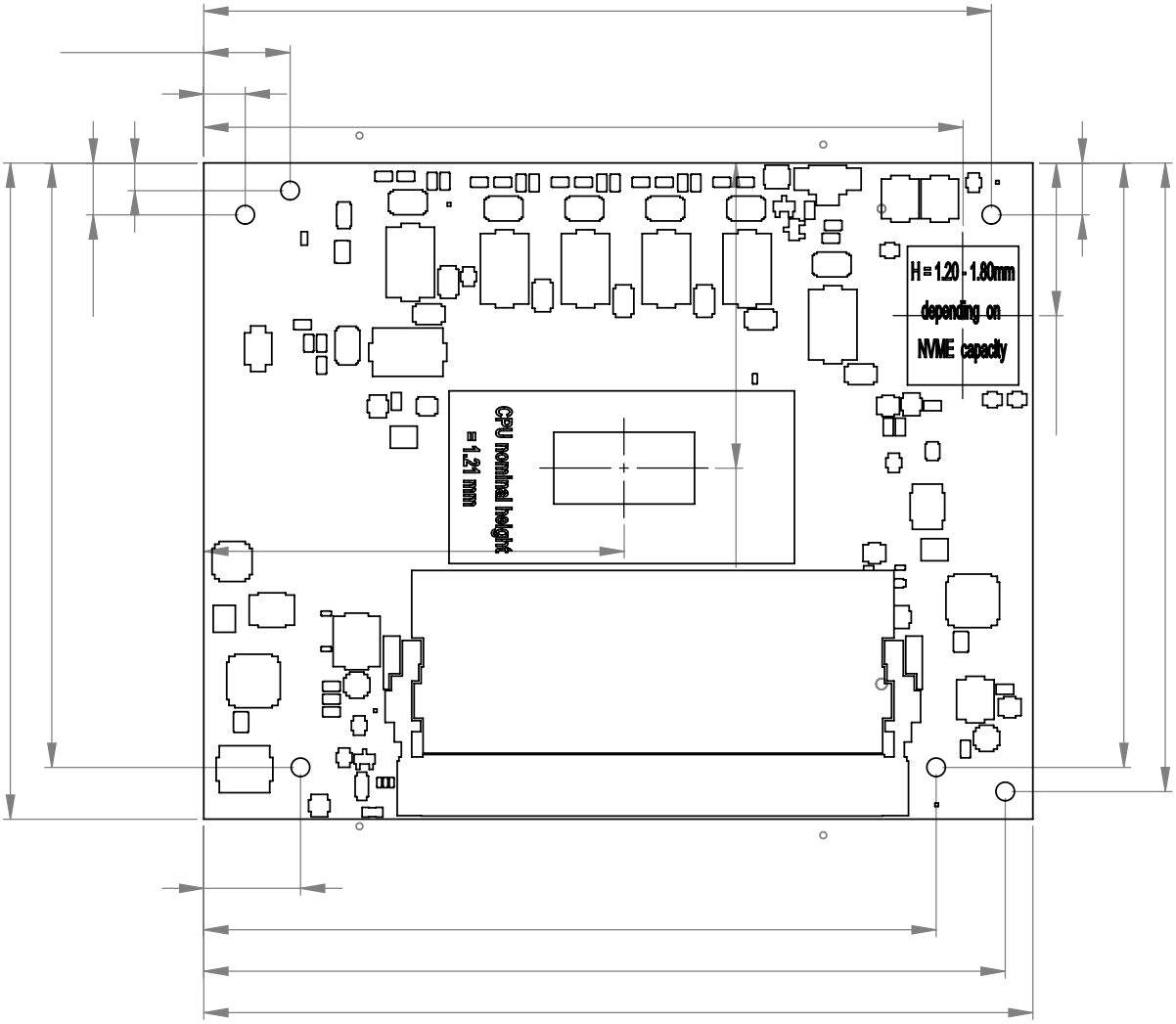

Figure 6: Module Dimensions

3.8.2 Module Height

The COM-HPC specification defines a module height of approximatly 15mm, when measured from the bottom of the module's PCB board to the top of the heatspreader. The overall height of the module and carrier board depends on

- which carrier board connectors are used (5mm and 10mm height are available)
- which cooling solution is used. The height of the cooling solution is not specified in the COM-HPC specification

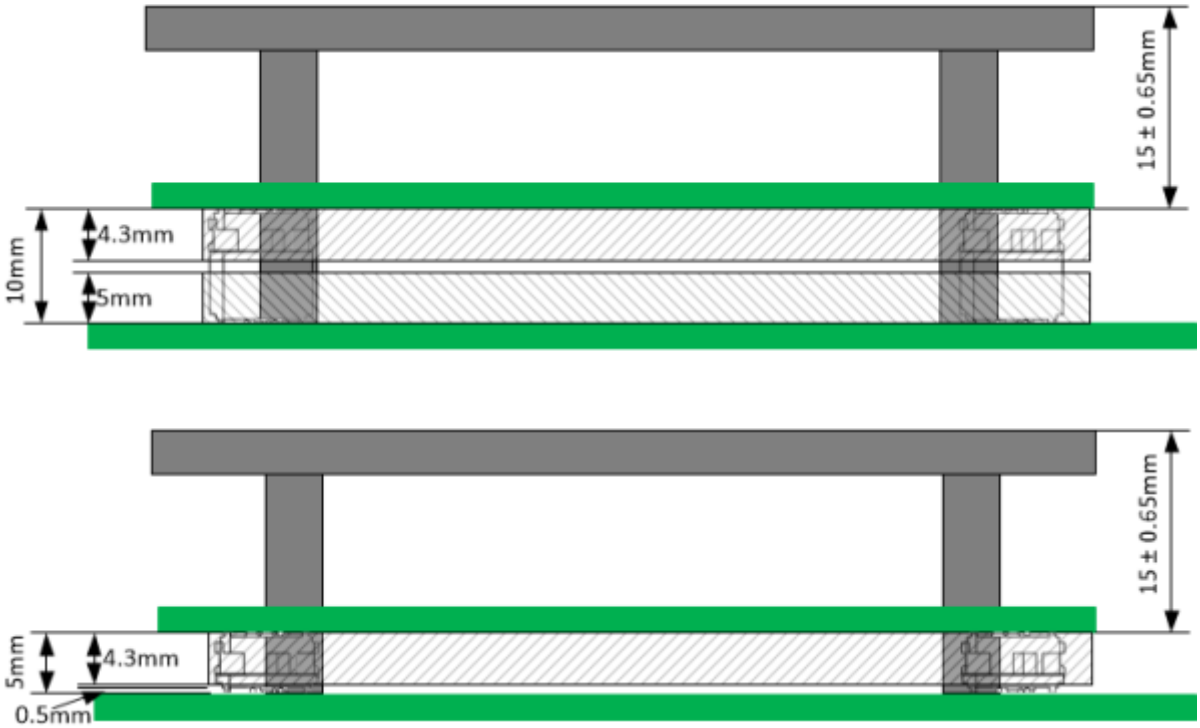

Figure 7: Module and Carrier Height with 10mm and 5mm connector height

3.8.3 Heatspreader Plate Assembly Dimension

Please check our Customer Section for Heatspreader 3D models and drawings.

3.9 Environmental Specification

The COMh-caRP support commercial temperature grades with on option of extended temperature grades (E1). The E1 is only available for customized versions only.

Environmental		**Description**
Commercial Grade	Operating	0°C to +60°C (32°F to 140°F)
	Non-operating	-30°C to +85°C (-22°F to 185°F)
Extended Grade (E1)	Operating	-25°C to +75°C (-13°F to 167°F)
	Non-operating	-30°C to +85°C (-22°F to 185°F)
Relative Humidity		93 % @40°C, non-condensing
Shock (according to IEC / EN 60068-2-27)		Non-operating shock test (half-sinusoidal, 11ms, 15g)
Vibration (according to IEC / EN 60068-2-6)		Non-operating vibration (sinusoidal, 10 Hz to 2000 Hz, +/- 0.15 mm, 2 g)

Table 33: Environmental Specification

3.10 Compliance

The COMh-caRP complies with the following or the latest status thereof. If modified, the prerequisites for specific approvals may no longer apply. For more information, contact Kontron Support.

Europe - CE Mark	
Directives	**2014/30/EU**: Electromagnetic Compatibility **2014/35/EU**: Low Voltage **2011/65/EU**: RoHS II **2001/95/EC**: General Product Safety
EMC	**EN 55032 Class B**: Electromagnetic compatibility of multimedia equipment - Emission Requirements Class A **EN 61000-6-2**: Electromagnetic compatibility (EMC) Part 6-2: Generic standards - Immunity standard for industrial environments
Safety	**EN 62368-1**: Audio/video, information and communication technology equipment - Part 1: Safety requirements

Table 34: Compliance CE Mark

USA/Canada	
Safety	**UL 62368-1 & CSA C22.2 No. 62368-1 (Component Recognition)**: Audio/video, information and communication technology equipment - Part 1: Safety requirements Recognized by Underwriters Laboratories Inc. Representative samples of this component have been evaluated by UL and meet applicable UL requirements. **UL listings**: AZOT2.E147705 AZOT8.E147705
UK CA Mark	
EMC	**BS EN 55032 Class B**: Electromagnetic compatibility of multimedia equipment - Emission Requirements Class A **BS EN 61000-6-2**: Electromagnetic compatibility (EMC) Part 6-2: Generic standards - Immunity standard for industrial environments
Safety	**BS EN 62368-1**: Audio/video, information and communication technology equipment - Part 1: Safety requirements
CB scheme (For International Certifications)	
Safety	**IEC 62368-1**: Audio/video, information and communication technology equipment - Part 1: Safety requirements

Table 35: Country Compliance

If the product is modified, the prerequisites for specific approvals may no longer apply.

Kontron is not responsible for any radio television interference caused by unauthorized modifications of the delivered product or the substitution or attachment of connecting cables and equipment other than those specified by Kontron. The correction of interference caused by unauthorized modification, substitution or attachment is the

user’s responsibility.

3.11 MTBF

The MTBF (Mean Time Before Failure) values were calculated using a combination of the manufacturer’s test data (if available) and the Telcordia (Bellcore) issue 2 calculation for the remaining parts.
The Telcordia calculation used is “” in a ground benign, controlled environment. This particular method takes into account varying temperature and stress data and the system is assumed to have not been burned-in. Other environmental stresses (such as extreme altitude, vibration, salt-water exposure) lower MTBF values.

	MTBF Value @40°C	Part Number
MTBF (hours)		

Table 36: MTBF

The MTBF estimated value above assumes no fan, but a passive heat sinking arrangement. Estimated RTC battery life (as opposed to battery failures) is not accounted for and needs to be considered separately. Battery life depends on both temperature and operating conditions. When the module is connected to external power, the only battery drain is from leakage paths.

4. COM-HPC Interface Connector

The COMh-caRP is a COM-HPC® Client module containing two 400-pin connectors J1 and J2; each with 4 rows called rows and all rows are named A to D on the primary connector J1 and E to H on the secondary connector J2.

Figure 8: COM-HPC Interface Connectors

1. COM-HPC interface connector (J1)
2. COM-HPC interface connector (J2)

4.1 Connecting COM-HPC Interface Connector to Carrier Board

The COM-HPC interface connectors (J1, J2) are inserted into the corresponding connectors on the carrier board and secured using the mounting points and standoffs. The height of the standoffs depends on the height of the carrier board’s connector.

The module is powered on by connecting to the carrier board using the interface connector. Before connecting the module’s interface connector to the carrier board’s corresponding connector, ensure that the carrier board is switch off and disconnected from the main power supply. Failure to disconnect the main power supply could result in personal injury and damage to the module and/or carrier board. Observe that only trained personnel aware of the associated dangers connect the module, within an access controlled ESD-safe workplace.

To protect external power lines of peripheral devices, make sure that the wires have the right diameter to withstand the maximum available current. The enclosure of the peripheral device fulfills the fire-protection requirements of IEC/EN 62368.

4.2 J1 and J2 signals

The type of an interface pin consists of the pin type and the buffer type.

Pin Types	Description
I	Input to the Module
O	Output from the Module
I/O	Bi-directional input / output signal
OD	Open drain output
REF	Analog reference voltage output – low voltage (GND min, 3.3V max)

Table 37: Pin Types

Buffer Types	Description
CMOS	Logic input or output. Input thresholds and output levels shall be at or over 80% of supply rail for the high side and at or under 20% of the relevant supply rail for the low side.
LV_DIFF	Low voltage differential signals – may include DP, TMDS, DP_AUX, MIPI D-PHY and HCSL (High Speed Current Steering Logic) used for PCIe clock pairs. Exact details for these variants differ, but the all of these signals are well under 3.3V and the LV_DIFF type label serves well to describe them as a group.
KR	Ethernet 25GBASE-KR or 10GBASE-KR compatible signal.
KX	Ethernet 1000BASE-KX compatible signal.
DP	Display Port compatible signal. Used for DDI interfaces.
MDI	Media Dependent Interface, used for NBASE-T signaling.
NFET	N channel FET output, drain pin, Module can pull low to GND or float.
PCIE	PCI Express compatible differential signals. Includes signaling up to PCIe Gen 5.
PDS	Pull-down strap. Module either pulls these lines to GND or leaves them open.
SATA	SATA compatible differential signals.
USB	USB 2.0 compliant differential signals.
USB_SS	USB Super Speed compliant signals; includes USB 3.0, USB 3.1, USB 3.2 and USB4.

Table 38: Buffer Types

Other Notation	Description
PD	Pull-Down
PU	Pull-Up
2K2	2.2 Kohm resistor (and so on for other values)

Table 39: Other Notation

4.3 Connector J1

4.3.1 Pins A1 - A100

Pin	Signal	Description	Type	Termination	Comment
A1	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
A2	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
A3	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
A4	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
A5	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
A6	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
A7	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
A8	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
A9	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
A10	GND	Power Ground	PWR GND	—	—
A11	BATLOW#	Battery Low	I-3.3	PU 10k 3.3V (S5)	assertion will prevent wake from S3-S5 state
A12	PLTRST#	Platform Reset	O-3.3	—	—
A13	GND	Power Ground	PWR GND	—	—
A14	USB7-	USB 2.0 Data Pair Port 7 -	DP-I/O	PD 14.25k to 24.8k in PCH	—
A15	USB7+	USB 2.0 Data Pair Port 7 +	DP-I/O	PD 14.25k to 24.8k in PCH	—
A16	GND	Power Ground	PWR GND	—	—
A17	USB6-	USB 2.0 Data Pair Port 6 -	DP-I/O	PD 14.25k to 24.8k in PCH	—
A18	USB6+	USB 2.0 Data Pair Port 6 +	DP-I/O	PD 14.25k to 24.8k in PCH	—
A19	GND	Power Ground	PWR GND	—	—
A20	DDI1_SDA_AUX-	DDI1 SDA AUX -	I/O-3.3	—	—
A21	DDI1_SCL_AUX+	DDI1 SCL AUX+	I/O-3.3	—	—
A22	GND	Power Ground	PWR GND	—	—
A23	DDI1_PAIR0-	DDI1 Pair 0 -	DP-O	—	—
A24	DDI1_PAIR0+	DDI1 Pair 0 +	DP-O	—	—
A25	GND	Power Ground	PWR GND	—	—
A26	DDI1_PAIR1-	DDI1 Pair 1 -	DP-O	—	—
A27	DDI1_PAIR1+	DDI1 Pair 1 +	DP-O	—	—

Pin	Signal	Description	Type	Termination	Comment
A28	GND	Power Ground	PWR GND	—	—
A29	DDI1_PAIR2-	DDI1 Pair 2 -	DP-O	—	—
A30	DDI1_PAIR2+	DDI1 Pair 2 +	DP-O	—	—
A31	GND	Power Ground	PWR GND	—	—
A32	DDI1_PAIR3-	DDI1 Pair 3 -	DP-O	—	—
A33	DDI1_PAIR3+	DDI1 Pair 3 +	DP-O	—	—
A34	GND	Power Ground	PWR GND	—	—
A35	eDP_AUX-	eDP AUX -	I/O PCIE LV_DIFF	—	—
A36	eDP_AUX+	eDP AUX +	I/O PCIE LV_DIFF	—	—
A37	GND	Power Ground	PWR GND	—	—
A38	eDP_TX0-	eDP Pair 0 -	O LV_DIFF	—	—
A39	eDP_TX0+	eDP Pair 0 +	O LV_DIFF	—	—
A40	GND	Power Ground	PWR GND	—	—
A41	eDP_TX1-	eDP Pair 0 -	O LV_DIFF	—	—
A42	eDP_TX1+	eDP Pair 0 +	O LV_DIFF	—	—
A43	GND	Power Ground	PWR GND	—	—
A44	eDP_TX2-	eDP Pair 0 -	O LV_DIFF	—	—
A45	eDP_TX2+	eDP Pair 0 +	O LV_DIFF	—	—
A46	GND	Power Ground	PWR GND	—	—
A47	eDP_TX3-	eDP Pair 0 -	O LV_DIFF	—	—
A48	eDP_TX3+	eDP Pair 0 +	O LV_DIFF	—	—
A49	GND	Power Ground	PWR GND	—	—
A50	eSPI_IO0	eSPI Master Data I/O 0	I/O-1.8	—	—
A51	eSPI_IO1	eSPI Master Data I/O 1	I/O-1.8	—	—
A52	eSPI_IO2	eSPI Master Data I/O 2	I/O-1.8	—	—
A53	eSPI_IO3	eSPI Master Data I/O 3	I/O-1.8	—	—
A54	eSPI_CLK	eSPI Master Clock Output	O-1.8	—	—
A55	GND	Power Ground	PWR GND	—	—
A56	PCIe_CLKREQ0_LO#	PCI Express clock request signal	I/O-3.3	PU 10k (S5)	—
A57	PCIe_CLKREQ0_HI#	PCI Express clock request signal	I/O-3.3	PU 10k (S5)	—
A58	GND	Power Ground	PWR GND	—	—
A59	PCIe_BMC_TX-	PCI Express Diff Transmit - for Carrier BMC	O PCIe	—	NA on standard variants
A60	PCIe_BMC_TX+	PCI Express Diff Transmit + for Carrier BMC	O PCIe	—	NA on standard variants
A61	GND	Power Ground	PWR GND	—	—
A62	PCIe08_TX-	PCI Express Lane 8 Transmit - Group 0 High	O PCIe	—	—
A63	PCIe08_TX+	PCI Express Lane 8 Transmit + Group 0 High	O PCIe	—	—
A64	GND	Power Ground	PWR GND	—	—

Pin	Signal	Description	Type	Termination	Comment
A65	PCIe09_TX-	PCI Express Lane 9 Transmit - Group 0 High	O PCIe	—	—
A66	PCIe09_TX+	PCI Express Lane 9 Transmit + Group 0 High	O PCIe	—	—
A67	GND	Power Ground	PWR GND	—	—
A68	PCIe10_TX-	PCI Express Lane 10 Transmit - Group 0 High	O PCIe	—	—
A69	PCIe10_TX+	PCI Express Lane 10 Transmit + Group 0 High	O PCIe	—	—
A70	GND	Power Ground	PWR GND	—	—
A71	PCIe11_TX-	PCI Express Lane 11 Transmit - Group 0 High	O PCIe	—	—
A72	PCIe11_TX+	PCI Express Lane 11 Transmit + Group 0 High	O PCIe	—	—
A73	GND	Power Ground	PWR GND	—	—
A74	PCIe12_TX-	PCI Express Lane 12 Transmit - Group 0 High	O PCIe	—	—
A75	PCIe12_TX+	PCI Express Lane 12 Transmit + Group 0 High	O PCIe	—	—
A76	GND	Power Ground	PWR GND	—	—
A77	PCIe13_TX-	PCI Express Lane 13 Transmit - Group 0 High	O PCIe	—	—
A78	PCIe13_TX+	PCI Express Lane 13 Transmit + Group 0 High	O PCIe	—	—
A79	GND	Power Ground	PWR GND	—	—
A80	PCIe14_TX-	PCI Express Lane 14 Transmit - Group 0 High	O PCIe	—	—
A81	PCIe14_TX+	PCI Express Lane 14 Transmit + Group 0 High	O PCIe	—	—
A82	GND	Power Ground	PWR GND	—	—
A83	PCIe15_TX-	PCI Express Lane 15 Transmit - Group 0 High	O PCIe	—	—
A84	PCIe15_TX+	PCI Express Lane 15 Transmit + Group 0 High	O PCIe	—	—
A85	GND	Power Ground	PWR GND	—	—
A86	VCC_RTC	Real-Time Clock Circuit Power Input	PWR 3V	—	voltage range 2.3-5.5V
A87	SUS_CLK	Clock used by Carrier peripherals	O-3.3	—	32 kHz
A88	GPIO_00	General purpose input/output 0	I/O-3.3	PU 100k 3.3V (S5)	—
A89	GPIO_01	General purpose input/output 1	I/O-3.3	PU 100k 3.3V (S5)	—
A90	GPIO_02	General purpose input/output 2	I/O-3.3	PU 100k 3.3V (S5)	—
A91	GPIO_03	General purpose input/output 3	I/O-3.3	PU 100k 3.3V (S5)	—

Pin	Signal	Description	Type	Termination	Comment
A92	GPIO_04	General purpose input/output 4	I/O-3.3	PU 100k 3.3V (S5)	—
A93	GPIO_05	General purpose input/output 5	I/O-3.3	PU 100k 3.3V (S5)	—
A94	GPIO_06	General purpose input/output 6	I/O-3.3	PU 100k 3.3V (S5)	—
A95	GPIO_07	General purpose input/output 7	I/O-3.3	PU 100k 3.3V (S5)	—
A96	GPIO_08	General purpose input/output 8	I/O-3.3	PU 100k 3.3V (S5)	—
A97	GPIO_09	General purpose input/output 9	I/O-3.3	PU 100k 3.3V (S5)	—
A98	GPIO_10	General purpose input/output 10	I/O-3.3	PU 100k 3.3V (S5)	—
A99	GPIO_11	General purpose input/output 11	I/O-3.3	PU 100k 3.3V (S5)	—
A100	TYPE0	Pin-out Type Indication	PDS	—	—

Table 40: Connector J1 Pins A1 - A100

4.3.2 Pins B1 - B100

Pin	Signal	Description	Type	Termination	Comment
B1	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
B2	PWRBTN#	Power Button	I-3.3	PU 10k 3.3V (S5)	—
B3	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
B4	THERMTRIP#	Thermal Trip	O-3.3	—	Thermal Trip Event, transition to S5 indicator
B5	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
B6	TAMPER#	Tamper or Intrusion detection line	I-3.3	PU 1M 3.3V (RTC_G3)	—
B7	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
B8	SUS_S3#	Suspend To RAM (or deeper) Indicator	O-3.3	PD 100K	—
B9	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
B10	WD_STROBE#	Watchdog timer strobe input	I-3.3	PU 10k 3.3V (S0)	—
B11	WD_OUT	Watchdog timer indication	O-3.3	PD 10K	—

Pin	Signal	Description	Type	Termination	Comment
B12	GND	Power Ground	PWR GND	—	—
B13	USB5-	USB 2.0 Data Pair Port 5 -	I/O-3.3	—	—
B14	USB5+	USB 2.0 Data Pair Port 5 +	I/O-3.3	—	—
B15	GND	Power Ground	PWR GND	—	—
B16	USB4-	USB 2.0 Data Pair Port 4 -	I/O-3.3	—	—
B17	USB4+	USB 2.0 Data Pair Port 4 +	I/O-3.3	—	—
B18	GND	Power Ground	PWR GND	—	—
B19	I2S_LRCLK/SNDW_CLK3/HDA_SYNC	I2S L/R Clock. Alternative use as Soundwire 3 clock or HDA sample synchronization signal	O-1.8	—	—
B20	I2S_DOUT/SNDW_DAT3/ HDA_SDO	I2S Data Out. Input in I2S mode Alternative use as bi-directional Soundwire 3 data lane or HDA serial TDM data output	I/O-1.8	—	—
B21	I2S_MCLK/HDA_RST#	I2S Master Clock. Alternative use as HDA reset output	O-1.8	—	—
B22	I2S_DIN/SNDW_DAT2/HDA_SDI	I2S Data In. Input in I2S mode. Alternative use as bi-directional Soundwire 2 data lane or HDA serial TDM data input	I/O-1.8	—	—
B23	I2S_CLK/SNDW_CLK2/HDA_BCLK	I2S Clock. Alternative use as Soundwire 2 clock or HDA serial data clock	O-1.8	—	—
B24	VCC_5V_SBY	5V Standby (4.75V - 5.25V)	PWR 5V (S5)	—	—
B25	USB67_OC#	USB over-current sense 6 & 7	I-3.3	PU 10k 3.3V (S5)	—
B26	USB45_OC#	USB over-current sense 4 & 5	I-3.3	PU 10k 3.3V (S5)	—
B27	USB23_OC#	USB over-current sense 2 & 3	I-3.3	PU 10k 3.3V (S5)	—
B28	USB01_OC#	USB over-current sense 0 & 1	I-3.3	PU 10k 3.3V (S5)	—

Pin	Signal	Description	Type	Termination	Comment
B29	SML1_CLK	SML 1 Clock Line	I/O-3.3	PU	—
B30	SML1_DAT	SML 1 Data Line	I/O-3.3	PU	—
B31	PMCALERT#	Active low Alert signal (SML 1)	I-3.3	PU 10k 3.3V (S5)	—
B32	SML0_CLK	SML 0 Clock Line	I/O-3.3	PU	—
B33	SML0_DAT	SML 0 Data Line	I/O-3.3	PU	—
B34	USB_PD_ALERT#	Active low Alert signal (USB)	I-3.3	PU	—
B35	USB_PD_I2C_CLK	I2C clock line	I/O-3.3	PU	—
B36	USB_PD_I2C_DAT	I2C data line	I/O-3.3	PU	—
B37	USB_RT_ENA	Power Enable for USB Retimers	O-3.3	—	—
B38	USB1_LSRX	USB 4 Receive channel 1	I-3.3	PD	—
B39	USB1_LSTX	USB 4 Transmit channel 1	O-3.3	PD	—
B40	USB0_LSRX	USB 4 Receive channel 0	I-3.3	PD	—
B41	USB0_LSTX	USB 4 Transmit channel 0	O-3.3	PD	—
B42	GND	Power Ground	PWR GND	—	—
B43	USB0_AUX-	USB4 DP Aux channel 0 -	LV_Diff	—	—
B44	USB0_AUX+	USB4 DP Aux channel 0 +	LV_Diff	—	—
B45	LID#	LID switch	I-3.3	PU	—
B46	SLEEP#	Sleep button	I-3.3	PU	—
B47	VCC_BOOT_SPI	Power supply for Carrier Board SPI	PWR 1.8/3.3	—	—
B48	BOOT_SPI_CS#	Clock from Module chipset to Carrier SPI	O	—	—
B49	BSEL0	Boot Select Pin 0	I	PU 10k 3.3V (S5)	—
B50	BSEL1	Boot Select Pin 1	I	PU 10k 3.3V (S5)	—
B51	BSEL2	Boot Select Pin 2	I	PU 10k 3.3V (S5)	—
B52	eSPI_ALERT0#	eSPI Alert 0	I-1.8	PU	—
B53	eSPI_ALERT1#	eSPI Alert 1	NA	PU	—
B54	eSPI_CS0#	eSPI Master Chip Select 0	O-1.8	PU	—
B55	eSPI_CS1#	eSPI Master Chip Select 1	NA	PU	—
B56	eSPI_RST#	eSPI Reset	O-1.8	—	—
B57	GND	Power Ground	PWR GND	—	—

Pin	Signal	Description	Type	Termination	Comment
B58	PCIe_BMC_RX-	PCI Express Diff Receive - for Carrier BMC	I PCIe	—	NA on standard variants
B59	PCIe_BMC_RX+	PCI Express Diff Receive + for Carrier BMC	I PCIe	—	NA on standard variants
B60	GND	Power Ground	PWR GND	—	—
B61	PCIe08_RX-	PCI Express Lane 8 Receive - Group 0 High	I PCIe	—	—
B62	PCIe08_RX+	PCI Express Lane 8 Receive + Group 0 High	I PCIe	—	—
B63	GND	Power Ground	PWR GND	—	—
B64	PCIe09_RX-	PCI Express Lane 9 Receive - Group 0 High	I PCIe	—	—
B65	PCIe09_RX+	PCI Express Lane 9 Receive + Group 0 High	I PCIe	—	—
B66	GND	Power Ground	PWR GND	—	—
B67	PCIe10_RX-	PCI Express Lane 10 Receive - Group 0 High	I PCIe	—	—
B68	PCIe10_RX+	PCI Express Lane 10 Receive + Group 0 High	I PCIe	—	—
B69	GND	Power Ground	PWR GND	—	—
B70	PCIe11_RX-	PCI Express Lane 11 Receive - Group 0 High	I PCIe	—	—
B71	PCIe11_RX+	PCI Express Lane 11 Receive + Group 0 High	I PCIe	—	—
B72	GND	Power Ground	PWR GND	—	—
B73	PCIe12_RX-	PCI Express Lane 12 Receive - Group 0 High	I PCIe	—	—
B74	PCIe12_RX+	PCI Express Lane 12 Receive + Group 0 High	I PCIe	—	—
B75	GND	Power Ground	PWR GND	—	—
B76	PCIe13_RX-	PCI Express Lane 13 Receive - Group 0 High	I PCIe	—	—

Pin	Signal	Description	Type	Termination	Comment
B77	PCIe13_RX+	PCI Express Lane 13 Receive + Group 0 High	I PCIe	—	—
B78	GND	Power Ground	PWR GND	—	—
B79	PCIe14_RX-	PCI Express Lane 14 Receive - Group 0 High	I PCIe	—	—
B80	PCIe14_RX+	PCI Express Lane 14 Receive + Group 0 High	I PCIe	—	—
B81	GND	Power Ground	PWR GND	—	—
B82	PCIe15_RX-	PCI Express Lane 15 Receive - Group 0 High	I PCIe	—	—
B83	PCIe15_RX+	PCI Express Lane 15 Receive + Group 0 High	I PCIe	—	—
B84	GND	Power Ground	PWR GND	—	—
B85	TEST#	Test mode	I OD-3.3	PU	leave unconnected on carrier
B86	RSMRST_OUT#	Resume Reset	O-3.3	—	Buffered copy of internal Module RSMRST#
B87	UART1_TX	UART Transmit Port 1	O-3.3	—	—
B88	UART1_RX	UART Receive Port 1	I-3.3	PU	—
B89	UART1_RTS#	UART Request to Send Port 1	O-3.3	—	—
B90	UART1_CTS#	UART Clear to Send Port 1	I-3.3	PU	—
B91	IPMB_CLK	Clock I/O for IPMB Port	I/O OD-3.3	PU 47k	—
B92	IPMB_DAT	Data I/O for IPMB Port	I/O OD-3.3	PU 47k	—
B93	GP_SPI_MOSI	SPI Master Out Slave In	O-3.3	—	—
B94	GP_SPI_MISO	SPI Master IN Slave OUT	I-3.3	PU	—
B95	GP_SPI_CS0#	SPI Chip Select	O-3.3	—	—
B96	GP_SPI_CS1#	SPI Chip Select	O-3.3	—	—
B97	GP_SPI_CS2#	SPI Chip Select	O-3.3	—	—
B98	GP_SPI_CS3#	SPI Chip Select	O-3.3	—	—
B99	GP_SPI_CLK	SPI Clock	O-3.3	—	—
B100	GP_SPI_ALERT#	SPI Alert (interrupt)	I-3.3	PU	—

Table 41: Connector J1 Pins B1 - B100

4.3.3 Pins C1 - C100

Pin	Signal	Description	Type	Termination	Comment
C1	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
C2	RSTBTN#	Reset button input	I-3.3	PU	—
C3	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
C4	CARRIER_HOT#	Temp sensor for over-temp	I-3.3	PU	—
C5	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
C6	VIN_PWROK	Power OK from Main supply	I-3.3	PU 10k 3.3V (S5)	—
C7	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
C8	SUS_S4_S5#	Suspend To Disk (S4) or Soft Off (S5) Indicator	O-3.3	PD 100K	—
C9	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
C10	GND	Power Ground	PWR GND	—	—
C11	FAN_PWMOUT	Fan speed control	O-3.3	—	
C12	FAN_TACHIN	Fan tachometer	I-3.3	PU	
C13	GND	Power Ground	PWR GND	—	—
C14	USB3-	USB 2.0 Data Pair Port 3 -	I/O-3.3	—	—
C15	USB3+	USB 2.0 Data Pair Port 3 +	I/O-3.3	—	—
C16	GND	Power Ground	PWR GND	—	—
C17	USB2-	USB 2.0 Data Pair Port 2 -	I/O-3.3	—	—
C18	USB2+	USB 2.0 Data Pair Port 2 +	I/O-3.3	—	—
C19	GND	Power Ground	PWR GND	—	—
C20	SNDW_DMIC_CLK1	Clock for Soundwire transaction	I/O-1.8	—	—
C21	SNDW_DMIC_DAT1	PCM Audio data	O-1.8	—	—
C22	GND	Power Ground	PWR GND	—	—
C23	SNDW_DMIC_CLK0	Clock for Soundwire transaction	I/O-1.8	—	—
C24	SNDW_DMIC_DAT0	PCM Audio data	O-1.8	—	—
C25	GND	Power Ground	PWR GND	—	—
C26	DDI0_DDC_AUX_SEL	DDI0 AUX function select	I-3.3	—	—
C27	DDI1_DDC_AUX_SEL	DDI1 AUX function select	I-3.3	—	—
C28	DDI0_HPD	DDI0 Hot Plug Detect	I-3.3	PD 100k	—
C29	DDI1_HPD	DDI1 Hot Plug Detect	I-3.3	PD 100k	—
C30	eDP_HPD	eDP Hot Plug Detect	I-3.3	PD 100k	—
C31	eDP_VDD_EN	eDP Power Enable	O-3.3	—	—
C32	eDP_BKLT_EN	eDP Backlight Enable	O-3.3	—	—
C33	eDP_BKLTCTL	eDP Backlight Brightness Control	O-3.3	—	—
C34	GND	Power Ground	PWR GND	—	—
C35	USB1_AUX-	USB4 DP Aux channel 1 -	LV_Diff	—	—
C36	USB1_AUX+	USB4 DP Aux channel 1+	LV_Diff	—	—
C37	GND	Power Ground	PWR GND	—	—

Pin	Signal	Description	Type	Termination	Comment
C38	USB1_SSRX0-	USB Super Speed Pair 1 Receive 0 -	I USB SS	—	—
C39	USB1_SSRX0+	USB Super Speed Pair 1 Receive 0	I USB SS	—	—
C40	GND	Power Ground	PWR GND	—	—
C41	USB1_SSRX1-	USB Super Speed Pair 1 Receive 1 -	I USB SS	—	—
C42	USB1_SSRX1+	USB Super Speed Pair 1 Receive 1 +	I USB SS	—	—
C43	GND	Power Ground	PWR GND	—	—
C44	USB0_SSRX0-	USB Super Speed Pair 0 Receive 0 -	I USB SS	—	—
C45	USB0_SSRX0+	USB Super Speed Pair 0 Receive 0 +	I USB SS	—	—
C46	GND	Power Ground	PWR GND	—	—
C47	USB0_SSRX1-	USB Super Speed Port 0 Receive 1 -	I USB SS	—	—
C48	USB0_SSRX1+	USB Super Speed Port 0 Receive 1 +	I USB SS	—	—
C49	GND	Power Ground	PWR GND	—	—
C50	BOOT_SPI_IO0	SPI Data 0	I/O	—	—
C51	BOOT_SPI_IO1	SPI Data 1	I/O	—	—
C52	BOOT_SPI_IO2	SPI Data 2	I/O	—	—
C53	BOOT_SPI_IO3	SPI Data 3	I/O	—	—
C54	BOOT_SPI_CLK	Clock Module to Carrier SPI	O	—	—
C55	GND	Power Ground	PWR GND	—	—
C56	PCIe_REFCLK0_HI-	Reference clock PCIe Group 0 High -	O LV_DIFF	—	—
C57	PCIe_REFCLK0_HI+	Reference clock PCIe Group 0 High +	O LV_DIFF	—	—
C58	GND	Power Ground	PWR GND	—	—
C59	PCIe_REFCLK0_LO-	Reference clock PCIe Group 0 Low -	O LV_DIFF	—	—
C60	PCIe_REFCLK0_LO+	Reference clock PCIe Group 0 Low +	O LV_DIFF	—	—
C61	GND	Power Ground	PWR GND	—	—
C62	PCIe00_RX-	PCI Express Lane 0 Receive - Group 0 Low	I PCIe	—	—
C63	PCIe00_RX+	PCI Express Lane 0 Receive + Group 0 Low	I PCIe	—	—
C64	GND	Power Ground	PWR GND	—	—
C65	PCIe01_RX-	PCI Express Lane 1 Receive - Group 0 Low	I PCIe	—	—
C66	PCIe01_RX+	PCI Express Lane 1 Receive + Group 0 Low	I PCIe	—	—
C67	GND	Power Ground	PWR GND	—	—

Pin	Signal	Description	Type	Termination	Comment
C68	PCIe02_RX-	PCI Express Lane 2 Receive - Group 0 Low	I PCIe	—	NA on standard variants
C69	PCIe02_RX+	PCI Express Lane 2 Receive + Group 0 Low	I PCIe	—	NA on standard variants
C70	GND	Power Ground	PWR GND	—	—
C71	PCIe03_RX-	PCI Express Lane 3 Receive - Group 0 Low	I PCIe	—	NA on standard variants
C72	PCIe03_RX+	PCI Express Lane 3 Receive + Group 0 Low	I PCIe	—	NA on standard variants
C73	GND	Power Ground	PWR GND	—	—
C74	PCIe04_RX-	PCI Express Lane 4 Receive - Group 0 Low	I PCIe	—	—
C75	PCIe04_RX+	PCI Express Lane 4 Receive + Group 0 Low	I PCIe	—	—
C76	GND	Power Ground	PWR GND	—	—
C77	PCIe05_RX-	PCI Express Lane 5 Receive - Group 0 Low	I PCIe	—	—
C78	PCIe05_RX+	PCI Express Lane 5 Receive + Group 0 Low	I PCIe	—	—
C79	GND	Power Ground	PWR GND	—	—
C80	PCIe06_RX-	PCI Express Lane 6 Receive - Group 0 Low	I PCIe	—	—
C81	PCIe06_RX+	PCI Express Lane 6 Receive + Group 0 Low	I PCIe	—	—
C82	GND	Power Ground	PWR GND	—	—
C83	PCIe07_RX-	PCI Express Lane 7 Receive - Group 0 Low	I PCIe	—	—
C84	PCIe07_RX+	PCI Express Lane 7 Receive + Group 0 Low	I PCIe	—	—
C85	GND	Power Ground	PWR GND	—	—
C86	SMB_CLK	SMB Clock	I/O OD-3.3	PU	—
C87	SMB_DAT	SMB Data	I/O OD-3.3	PU	—
C88	SMB_ALERT#	SMB Alert	I-3.3	PU	—
C89	UART0_TX	UART Transmit Port 0	O-3.3	—	—
C90	UART0_RX	UART Receive Port 0	I-3.3	PU	—
C91	UART0_RTS#	UART Request to Send Port 0	O-3.3	—	—
C92	UART0_CTS#	UART Clear to Send Port 0	I-3.3	PU	—
C93	I2C0_CLK	I2C Clock Port 0	I/O OD-3.3	PU 2k2	—
C94	I2C0_DAT	I2C Data Port 0	I/O OD-3.3	PU 2k2	—
C95	I2C0_ALERT#	I2C Alert	I-3.3	PU 2k2	—
C96	I2C1_CLK	I2C Clock Port 1	I/O OD-3.3	PU 2k2	—
C97	I2C1_DAT	I2C Data Port 1	I/O OD-3.3	PU 2k2	—
C98	NBASET0_SDP	NBASE-T Ethernet Port 0 SDP	I/O-3.3	—	—

Pin	Signal	Description	Type	Termination	Comment
C99	NBASET0_CTREF	NBASE-T Ethernet Port 0 Reference voltage	0-3.3	1µF capacitor	—
C100	TYPE1	Pin-out Type indication	—	Tie to GND	—

Table 42: Connector J1 Pins C1 - C100

4.3.4 Pins D1 - D100

Pin	Signal	Description	Type	Termination	Comment
D1	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
D2	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
D3	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
D4	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
D5	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
D6	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
D7	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
D8	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
D9	VCC	Main Input Voltage (8.0V-20V)	PWR 8.0-20V	—	—
D10	WAKE0#	PCI Express Wake Event	I/O-3.3	PU	—
D11	WAKE1#	General Purpose Wake Event	I-3.3	PU	—
D12	GND	Power Ground	PWR GND	—	—
D13	USB1-	USB 2.0 Data Pair Port 1 -	I/O-3.3	—	—
D14	USB1+	USB 2.0 Data Pair Port 1 +	I/O-3.3	—	—
D15	GND	Power Ground	PWR GND	—	—
D16	USB0-	USB 2.0 Data Pair Port 0 -	I/O-3.3	—	—
D17	USB0+	USB 2.0 Data Pair Port 0 +	I/O-3.3	—	—
D18	GND	Power Ground	PWR GND	—	—
D19	DDI0_SDA_AUX-	DDI0 SDA AUX -	I/O-3.3	PU 100k	
D20	DDI0_SCL_AUX+	DDI0 SCL AUX+	I/O-3.3	PD 100k	
D21	GND	Power Ground	PWR GND	—	—
D22	DDI0_PAIR0-	DDI0 Pair 0 -	DP-O	—	—
D23	DDI0_PAIR0+	DDI0 Pair 0 +	DP-O	—	—
D24	GND	Power Ground	PWR GND	—	—
D25	DDI0_PAIR1-	DDI0 Pair 1 -	DP-O	—	—
D26	DDI0_PAIR1+	DDI0 Pair 1 +	DP-O	—	—
D27	GND	Power Ground	PWR GND	—	—
D28	DDI0_PAIR2-	DDI0 Pair 2 -	DP-O	—	—
D29	DDI0_PAIR2+	DDI0 Pair 2 +	DP-O	—	—
D30	GND	Power Ground	PWR GND	—	—
D31	DDI0_PAIR3-	DDI0 Pair 3 -	DP-O	—	—
D32	DDI0_PAIR3+	DDI0 Pair 3 +	DP-O	—	—
D33	GND	Power Ground	PWR GND	—	—
D34	AC_PRESENT	AC power	I-3.3	PU	
D35	RSVD	Reserved Pin	—	—	—

Pin	Signal	Description	Type	Termination	Comment
D36	GND	Power Ground	PWR GND	—	—
D37	USB1_SSTX0-	USB Super Speed Pair 1 Transmit 0 -	O USB SS	—	—
D38	USB1_SSTX0+	USB Super Speed Pair 1 Transmit 0 +	O USB SS	—	—
D39	GND	Power Ground	PWR GND	—	—
D40	USB1_SSTX1-	USB Super Speed Pair 1 Transmit 1 -	O USB SS	—	—
D41	USB1_SSTX1+	USB Super Speed Pair 1 Transmit 1 +	O USB SS	—	—
D42	GND	Power Ground	PWR GND	—	—
D43	USB0_SSTX0-	USB Super Speed Pair 0 Transmit 0 -	O USB SS	—	—
D44	USB0_SSTX0+	USB Super Speed Pair 0 Transmit 0 +	O USB SS	—	—
D45	GND	Power Ground	PWR GND	—	—
D46	USB0_SSTX1-	USB Super Speed Pair 0 Transmit 1 -	O USB SS	—	—
D47	USB0_SSTX1+	USB Super Speed Pair 0 Transmit 1 +	O USB SS	—	—
D48	GND	Power Ground	PWR GND	—	—
D49	SATA0_RX-	SATA 0 Receive Pair -	I SATA	—	—
D50	SATA0_RX+	SATA 0 Receive Pair +	I SATA	—	—
D51	GND	Power Ground	PWR GND	—	—
D52	SATA0_TX-	SATA 0 Transmit Pair -	O SATA	—	—
D53	SATA0_TX+	SATA 0 Transmit Pair +	O SATA	—	—
D54	GND	Power Ground	PWR GND	—	—
D55	SATA1_RX-	SATA 1 Receive Pair -	I SATA	—	—
D56	SATA1_RX+	SATA 1 Receive Pair +	I SATA	—	—
D57	GND	Power Ground	PWR GND	—	—
D58	SATA1_TX-	SATA 1 Transmit Pair -	O SATA	—	—
D59	SATA1_TX+	SATA 1 Transmit Pair +	O SATA	—	—
D60	GND	Power Ground	PWR GND	—	—
D61	PCIe00_TX-	PCI Express Lane 0 Transmit - Group 0 Low	O PCIe	—	—
D62	PCIe00_TX+	PCI Express Lane 0 Transmit + Group 0 Low	O PCIe	—	—
D63	GND	Power Ground	PWR GND	—	—
D64	PCIe01_TX-	PCI Express Lane 1 Transmit - Group 0 Low	O PCIe	—	—
D65	PCIe01_TX+	PCI Express Lane 1 Transmit + Group 0 Low	O PCIe	—	—
D66	GND	Power Ground	PWR GND	—	—
D67	PCIe02_TX-	PCI Express Lane 2 Transmit - Group 0 Low	O PCIe	—	NA on standard variants

Pin	Signal	Description	Type	Termination	Comment
D68	PCIe02_TX+	PCI Express Lane 2 Transmit + Group 0 Low	O PCIe	—	NA on standard variants
D69	GND	Power Ground	PWR GND	—	—
D70	PCIe03_TX-	PCI Express Lane 3 Transmit - Group 0 Low	O PCIe	—	NA on standard variants
D71	PCIe03_TX+	PCI Express Lane 3 Transmit + Group 0 Low	O PCIe	—	NA on standard variants
D72	GND	Power Ground	PWR GND	—	—
D73	PCIe04_TX-	PCI Express Lane 4 Transmit - Group 0 Low	O PCIe	—	—
D74	PCIe04_TX+	PCI Express Lane 4 Transmit + Group 0 Low	O PCIe	—	—
D75	GND	Power Ground	PWR GND	—	—
D76	PCIe05_TX-	PCI Express Lane 5 Transmit - Group 0 Low	O PCIe	—	—
D77	PCIe05_TX+	PCI Express Lane 5 Transmit + Group 0 Low	O PCIe	—	—
D78	GND	Power Ground	PWR GND	—	—
D79	PCIe06_TX-	PCI Express Lane 6 Transmit - Group 0 Low	O PCIe	—	—
D80	PCIe06_TX+	PCI Express Lane 6 Transmit + Group 0 Low	O PCIe	—	—
D81	GND	Power Ground	PWR GND	—	—
D82	PCIe07_TX-	PCI Express Lane 7 Transmit - Group 0 Low	O PCIe	—	—
D83	PCIe07_TX+	PCI Express Lane 7 Transmit + Group 0 Low	O PCIe	—	—
D84	GND	Power Ground	PWR GND	—	—
D85	NBASET0_MDI0-	NBASE-T Ethernet Port 0 MDI Pair 0 -	I/O-3.3	—	—
D86	NBASET0_MDI0+	NBASE-T Ethernet Port 0 MDI Pair 0 -	I/O-3.3	—	—
D87	GND	Power Ground	PWR GND	—	—
D88	NBASET0_MDI1-	NBASE-T Ethernet Port 0 MDI Pair 1 -	I/O-3.3	—	—
D89	NBASET0_MDI1+	NBASE-T Ethernet Port 0 MDI Pair 1 -	I/O-3.3	—	—
D90	GND	Power Ground	PWR GND	—	—
D91	NBASET0_MDI2-	NBASE-T Ethernet Port 0 MDI Pair 2 -	I/O-3.3	—	—
D92	NBASET0_MDI2+	NBASE-T Ethernet Port 0 MDI Pair 2 -	I/O-3.3	—	—
D93	GND	Power Ground	PWR GND	—	—
D94	NBASET0_MDI3-	NBASE-T Ethernet Port 0 MDI Pair 3 -	I/O-3.3	—	—

Pin	Signal	Description	Type	Termination	Comment
D95	NBASET0_MDI3+	NBASE-T Ethernet Port 0 MDI Pair 3 -	I/O-3.3	—	—
D96	GND	Power Ground	PWR GND	—	—
D97	NBASET0_LINK_MAX#	NBASE-T Ethernet Port 0 MAX speed Link indicator	O-3.3	—	—
D98	NBASET0_LINK_MID#	NBASE-T Ethernet Port 0 MID speed Link indicator	O-3.3	—	—
D99	NBASET0_LINK_ACT#	NBASE-T Ethernet Port 0 controller activity indicator	O-3.3	—	—
D100	TYPE2	Pin-out Type indication	—	Tied to GND	—

Table 43: Connector J1 Pins D1 - D100

4.4 Connector J2

4.4.1 Pins E1 - E100

Pin	Signal	Description	Type	Termination	Comment
E1	RAPID_SHUTDOWN	Trigger for Rapid Shutdown	I-5.0	PD 100k	—
E2	GND	Power Ground	PWR GND	—	—
E3	DDI2_SDA_AUX-	DDI2 SDA AUX -	I/O-3.3	PU 100k	—
E4	DDI2_SCL_AUX+	DDI2 SCL AUX+	I/O-3.3	PD 100k	—
E5	GND	Power Ground	PWR GND	—	—
E6	DDI2_PAIR0-	DDI2 Pair 0 -	DP-O	—	—
E7	DDI2_PAIR0+	DDI2 Pair 0 +	DP-O	—	—
E8	GND	Power Ground	PWR GND	—	—
E9	DDI2_PAIR1-	DDI2 Pair 1 -	DP-O	—	—
E10	DDI2_PAIR1+	DDI2 Pair 1 +	DP-O	—	—
E11	GND	Power Ground	PWR GND	—	—
E12	DDI2_PAIR2-	DDI2 Pair 2 -	DP-O	—	—
E13	DDI2_PAIR2+	DDI2 Pair 2 +	DP-O	—	—
E14	GND	Power Ground	PWR GND	—	—
E15	DDI2_PAIR3-	DDI2 Pair 3 -	DP-O	—	—
E16	DDI2_PAIR3+	DDI2 Pair 3 +	DP-O	—	—
E17	GND	Power Ground	PWR GND	—	—
E18	DDI2_DDC_AUX_SEL	DDI2 AUX function select	I-3.3	—	—
E19	DDI2_HPD	DDI2 Hot Plug Detect	I-3.3	PD 100k	—
E20	GND	Power Ground	PWR GND	—	—
E21	PCIe32_TX-	PCI Express Lane 32 Transmit - Group 2	NA	—	—
E22	PCIe32_TX+	PCI Express Lane 32 Transmit + Group 2	NA	—	—
E23	GND	Power Ground	PWR GND	—	—

Pin	Signal	Description	Type	Termination	Comment
E24	PCIe33_TX-	PCI Express Lane 33 Transmit - Group 2	NA	—	—
E25	PCIe33_TX+	PCI Express Lane 33 Transmit + Group 2	NA	—	—
E26	GND	Power Ground	PWR GND	—	—
E27	PCIe34_TX-	PCI Express Lane 34 Transmit - Group 2	NA	—	—
E28	PCIe34_TX+	PCI Express Lane 34 Transmit + Group 2	NA	—	—
E29	GND	Power Ground	PWR GND	—	—
E30	PCIe35_TX-	PCI Express Lane 35 Transmit - Group 2	NA	—	—
E31	PCIe35_TX+	PCI Express Lane 35 Transmit + Group 2	NA	—	—
E32	GND	Power Ground	PWR GND	—	—
E33	PCIe36_TX-	PCI Express Lane 36 Transmit - Group 2	NA	—	—
E34	PCIe36_TX+	PCI Express Lane 36 Transmit + Group 2	NA	—	—
E35	GND	Power Ground	PWR GND	—	—
E36	PCIe37_TX-	PCI Express Lane 37 Transmit - Group 2	NA	—	—
E37	PCIe37_TX+	PCI Express Lane 37 Transmit + Group 2	NA	—	—
E38	GND	Power Ground	PWR GND	—	—
E39	PCIe38_TX-	PCI Express Lane 38 Transmit - Group 2	NA	—	—
E40	PCIe38_TX+	PCI Express Lane 38 Transmit + Group 2	NA	—	—
E41	GND	Power Ground	PWR GND	—	—
E42	PCIe39_TX-	PCI Express Lane 39 Transmit - Group 2	NA	—	—
E43	PCIe39_TX+	PCI Express Lane 39 Transmit + Group 2	NA	—	—
E44	GND	Power Ground	PWR GND	—	—
E45	PCIe16_TX-	PCI Express Lane 16 Transmit - Group 1	O PCIe	—	—
E46	PCIe16_TX+	PCI Express Lane 16 Transmit + Group 1	O PCIe	—	—
E47	GND	Power Ground	PWR GND	—	—
E48	PCIe17_TX-	PCI Express Lane 17 Transmit - Group 1	O PCIe	—	—
E49	PCIe17_TX+	PCI Express Lane 17 Transmit + Group 1	O PCIe	—	—
E50	GND	Power Ground	PWR GND	—	—
E51	PCIe18_TX-	PCI Express Lane 18 Transmit - Group 1	O PCIe	—	—
E52	PCIe18_TX+	PCI Express Lane 18 Transmit + Group 1	O PCIe	—	—

Pin	Signal	Description	Type	Termination	Comment
E53	GND	Power Ground	PWR GND	—	—
E54	PCIe19_TX-	PCI Express Lane 19 Transmit - Group 1	O PCIe	—	—
E55	PCIe19_TX+	PCI Express Lane 19 Transmit + Group 1	O PCIe	—	—
E56	GND	Power Ground	PWR GND	—	—
E57	PCIe20_TX-	PCI Express Lane 20 Transmit - Group 1	O PCIe	—	—
E58	PCIe20_TX+	PCI Express Lane 20 Transmit + Group 1	O PCIe	—	—
E59	GND	Power Ground	PWR GND	—	—
E60	PCIe21_TX-	PCI Express Lane 21 Transmit - Group 1	O PCIe	—	—
E61	PCIe21_TX+	PCI Express Lane 21 Transmit + Group 1	O PCIe	—	—
E62	GND	Power Ground	PWR GND	—	—
E63	PCIe22_TX-	PCI Express Lane 22 Transmit - Group 1	O PCIe	—	—
E64	PCIe22_TX+	PCI Express Lane 22 Transmit + Group 1	O PCIe	—	—
E65	GND	Power Ground	PWR GND	—	—
E66	PCIe23_TX-	PCI Express Lane 23 Transmit - Group 1	O PCIe	—	—
E67	PCIe23_TX+	PCI Express Lane 23 Transmit + Group 1	O PCIe	—	—
E68	GND	Power Ground	PWR GND	—	—
E69	RSVD	Reserved Pin	—	—	—
E70	RSVD	Reserved Pin	—	—	—
E71	RSVD	Reserved Pin	—	—	—
E72	RSVD	Reserved Pin	—	—	—
E73	RSVD	Reserved Pin	—	—	—
E74	RSVD	Reserved Pin	—	—	—
E75	RSVD	Reserved Pin	—	—	—
E76	RSVD	Reserved Pin	—	—	—
E77	RSVD	Reserved Pin	—	—	—
E78	NBASET1_CTREF	NBASE-T Ethernet Port 1 Reference voltage	0-3.3	1µF capacitor	—
E79	NBASET1_SDP	NBASE-T Ethernet Port 1 SDP	I/O-3.3	—	—
E80	NBASET1_LINK_MID#	NBASE-T Ethernet Port 1 MID speed Link indicator	O-3.3	—	—
E81	NBASET1_LINK_ACT#	NBASE-T Ethernet Port 1 controller activity indicator	O-3.3	—	—
E82	NBASET1_LINK_MAX#	NBASE-T Ethernet Port 1 MAX speed Link indicator	O-3.3	—	—
E83	GND	Power Ground	PWR GND	—	—
E84	RSVD			—	—
E85	RSVD			—	—
E86	GND	Power Ground	PWR GND	—	—

Pin	Signal	Description	Type	Termination	Comment
E87	ETH0_RX-	Ethernet KR Receive Port 0 -	NA	—	—
E88	ETH0_RX+	Ethernet KR Receive Port 0 +	NA	—	—
E89	GND	Power Ground	PWR GND	—	—
E90	ETH1_RX-	Ethernet KR Receive Port 1 -	NA	—	—
E91	ETH1_RX+	Ethernet KR Receive Port 1 +	NA	—	—
E92	GND	Power Ground	PWR GND	—	—
E93	PCIe_REFCLK1-	Reference clock PCIe Group 1 -	O LV_DIFF	—	—
E94	PCIe_REFCLK1+	Reference clock PCIe Group 1 +	O LV_DIFF	—	—
E95	GND	Power Ground	PWR GND	—	—
E96	PCIe_CLKREQ1#	PCIe Ref clock Group 1 request	I/O OD-3.3	PU 10k	—
E97	PCIe_CLKREQ2#	PCIe Ref clock Group 2 request	NA	PU 10k	—
E98	PCIe_CLKREQ_OUT0#	PCIe Ref clock off-module device request	NA	PU 10k	—
E99	PCIe_CLKREQ_OUT1#	PCIe Ref clock off-module device request	I/O OD-3.3	PU 10k	—
E100	PCIe_PERST_IN0#	Reset signals into Module to reset Module PCIe Targets	I-3.3	—	—

Table 44: Connector J2 Pins E1 - E100

4.4.2 Pins F1 - F100

Pin	Signal	Description	Type	Termination	Comment
F1	FUSA_STATUS0	FuSa two bit indication	NA	—	—
F2	FUSA_STATUS1	FuSa two bit indication	NA	—	—
F3	FUSA_ALERT#	Error occurrence on module	NA	—	—
F4	FUSA_SPI_CS#	FuSa Chip select	NA	—	—
F5	FUSA_SPI_CLK	FuSa Clock signal	NA	—	—
F6	FUSA_SPI_MISO	FuSa Master in Slave out	NA	—	—
F7	FUSA_SPI_MOSI	FuSa Master out Slave in	NA	—	—
F8	FUSA_SPI_ALERT	FuSa SPI data available	NA	—	—
F9	FUSA_VOLTAGE_ERR#	FuSa Over-/Undervoltage/current	NA	—	—
F10	PROCHOT#	Temperature excursion event	NA	—	—
F11	CATERR#	Catastrophic error event	NA	—	—
F12	RSVD	Reserved Pin	—	—	—
F13	RSVD	Reserved Pin	—	—	—
F14	RSVD	Reserved Pin	—	—	—
F15	RSVD	Reserved Pin	—	—	—
F16	RSVD	Reserved Pin	—	—	—
F17	RSVD	Reserved Pin	—	—	—
F18	RSVD	Reserved Pin	—	—	—
F19	GND	Power Ground	PWR GND	—	—
F20	PCIe32_RX-	PCI Express Lane 32 Receive - Group 2	NA	—	—

Pin	Signal	Description	Type	Termination	Comment
F21	PCIe32_RX+	PCI Express Lane 32 Receive + Group 2	NA	—	—
F22	GND	Power Ground	PWR GND	—	—
F23	PCIe33_RX-	PCI Express Lane 33 Receive - Group 2	NA	—	—
F24	PCIe33_RX+	PCI Express Lane 33 Receive + Group 2	NA	—	—
F25	GND	Power Ground	PWR GND	—	—
F26	PCIe34_RX-	PCI Express Lane 34 Receive - Group 2	NA	—	—
F27	PCIe34_RX+	PCI Express Lane 34 Receive + Group 2	NA	—	—
F28	GND	Power Ground	PWR GND	—	—
F29	PCIe35_RX-	PCI Express Lane 35 Receive - Group 2	NA	—	—
F30	PCIe35_RX+	PCI Express Lane 35 Receive + Group 2	NA	—	—
F31	GND	Power Ground	PWR GND	—	—
F32	PCIe36_RX-	PCI Express Lane 36 Receive - Group 2	NA	—	—
F33	PCIe36_RX+	PCI Express Lane 36 Receive + Group 2	NA	—	—
F34	GND	Power Ground	PWR GND	—	—
F35	PCIe37_RX-	PCI Express Lane 37 Receive - Group 2	NA	—	—
F36	PCIe37_RX+	PCI Express Lane 37 Receive + Group 2	NA	—	—
F37	GND	Power Ground	PWR GND	—	—
F38	PCIe38_RX-	PCI Express Lane 38 Receive - Group 2	NA	—	—
F39	PCIe38_RX+	PCI Express Lane 38 Receive + Group 2	NA	—	—
F40	GND	Power Ground	PWR GND	—	—
F41	PCIe39_RX-	PCI Express Lane 39 Receive - Group 2	NA	—	—
F42	PCIe39_RX+	PCI Express Lane 39 Receive + Group 2	NA	—	—
F43	GND	Power Ground	PWR GND	—	—
F44	PCIe16_RX-	PCI Express Lane 16 Receive - Group 1	I PCIe	—	—
F45	PCIe16_RX+	PCI Express Lane 16 Receive + Group 1	I PCIe	—	—

Pin	Signal	Description	Type	Termination	Comment
F46	GND	Power Ground	PWR GND	—	—
F47	PCIe17_RX-	PCI Express Lane 17 Receive - Group 1	I PCIe	—	—
F48	PCIe17_RX+	PCI Express Lane 17 Receive + Group 1	I PCIe	—	—
F49	GND	Power Ground	PWR GND	—	—
F50	PCIe18_RX-	PCI Express Lane 18 Receive - Group 1	I PCIe	—	—
F51	PCIe18_RX+	PCI Express Lane 18 Receive + Group 1	I PCIe	—	—
F52	GND	Power Ground	PWR GND	—	—
F53	PCIe19_RX-	PCI Express Lane 19 Receive - Group 1	I PCIe	—	—
F54	PCIe19_RX+	PCI Express Lane 19 Receive + Group 1	I PCIe	—	—
F55	GND	Power Ground	PWR GND	—	—
F56	PCIe20_RX-	PCI Express Lane 20 Receive - Group 1	I PCIe	—	—
F57	PCIe20_RX+	PCI Express Lane 20 Receive + Group 1	I PCIe	—	—
F58	GND	Power Ground	PWR GND	—	—
F59	PCIe21_RX-	PCI Express Lane 21 Receive - Group 1	I PCIe	—	—
F60	PCIe21_RX+	PCI Express Lane 21 Receive + Group 1	I PCIe	—	—
F61	GND	Power Ground	PWR GND	—	—
F62	PCIe22_RX-	PCI Express Lane 22 Receive - Group 1	I PCIe	—	—
F63	PCIe22_RX+	PCI Express Lane 22 Receive + Group 1	I PCIe	—	—
F64	GND	Power Ground	PWR GND	—	—
F65	PCIe23_RX-	PCI Express Lane 23 Receive - Group 1	I PCIe	—	—
F66	PCIe23_RX+	PCI Express Lane 23 Receive + Group 1	I PCIe	—	—
F67	GND	Power Ground	PWR GND	—	—
F68	RSVD	Reserved Pin	—	—	—
F69	RSVD	Reserved Pin	—	—	—
F70	GND	Power Ground	PWR GND	—	—
F71	NBASET1_MDI0-	NBASE-T Ethernet Port 1 MDI Pair 0 -	I/O-3.3	—	—

Pin	Signal	Description	Type	Termination	Comment
F72	NBASET1_MDI0+	NBASE-T Ethernet Port 1 MDI Pair 0 -	I/O-3.3	—	—
F73	GND	Power Ground	PWR GND	—	—
F74	NBASET1_MDI1-	NBASE-T Ethernet Port 1 MDI Pair 1 -	I/O-3.3	—	—
F75	NBASET1_MDI1+	NBASE-T Ethernet Port 1 MDI Pair 1 -	I/O-3.3	—	—
F76	GND	Power Ground	PWR GND	—	—
F77	NBASET1_MDI2-	NBASE-T Ethernet Port 1 MDI Pair 2 -	I/O-3.3	—	—
F78	NBASET1_MDI2+	NBASE-T Ethernet Port 1 MDI Pair 2 -	I/O-3.3	—	—
F79	GND	Power Ground	PWR GND	—	—
F80	NBASET1_MDI3-	NBASE-T Ethernet Port 1 MDI Pair 3 -	I/O-3.3	—	—
F81	NBASET1_MDI3+	NBASE-T Ethernet Port 1 MDI Pair 3 -	I/O-3.3	—	—
F82	GND	Power Ground	PWR GND	—	—
F83	RSVD	Reserved Pin	—	—	—
F84	RSVD	Reserved Pin	—	—	—
F85	GND	Power Ground	PWR GND	—	—
F86	ETH0_TX-	Ethernet KR Transmit Port 0 -	NA	—	—
F87	ETH0_TX+	Ethernet KR Transmit Port 0 +	NA	—	—
F88	GND	Power Ground	PWR GND	—	—
F89	ETH1_TX-	Ethernet KR Transmit Port 1 -	NA	—	—
F90	ETH1_TX+	Ethernet KR Transmit Port 1 +	NA	—	—
F91	GND	Power Ground	PWR GND	—	—
F92	PCIe_REFCLK2-	Reference clock PCIe Group 2 -	NA	—	—
F93	PCIe_REFCLK2+	Reference clock PCIe Group 2 +	NA	—	—
F94	GND	Power Ground	PWR GND	—	—
F95	RSVD			—	—
F96	ETH0-1_PRSNT#	Ethernet 0/1 Present	NA	—	—
F97	ETH0-1_PHY_RST#	Ethernet PHY reset signal	NA	—	—
F98	ETH0_SDP	Ethernet 0 SDP	NA	—	—
F99	ETH1_SDP	Ethernet 1 SDP	NA	—	—
F100	PCIe_PERST_IN1#	Reset signals into Module to reset Module PCIe Targets	NA	PD 100k	

Table 45: Connector J2 Pins F1 - F100

4.4.3 Pins G1 - G100

Pin	Signal	Description	Type	Termination	Comment
G1	VCC_5V_SBY	5V Standby (4.75V - 5.25V)	PWR 5V (S5)	—	—
G2	GND	Power Ground	PWR GND	—	—

Pin	Signal	Description	Type	Termination	Comment
G3	USB2_SSRX0-	USB Super Speed Pair 2 Receive 0 -	I USB SS	—	—
G4	USB2_SSRX0+	USB Super Speed Pair 2 Receive 0 +	I USB SS	—	—
G5	GND	Power Ground	PWR GND	—	—
G6	USB2_SSRX1-	USB Super Speed Pair 2 Receive 1 -	NA	—	—
G7	USB2_SSRX1+	USB Super Speed Pair 2 Receive 1 +	NA	—	—
G8	GND	Power Ground	PWR GND	—	—
G9	USB3_SSRX0-	USB Super Speed Pair 3 Receive 0 -	I USB SS	—	—
G10	USB3_SSRX0+	USB Super Speed Pair 3 Receive 0 +	I USB SS	—	—
G11	GND	Power Ground	PWR GND	—	—
G12	USB3_SSRX1-	USB Super Speed Pair 3 Receive 1 -	NA	—	—
G13	USB3_SSRX1+	USB Super Speed Pair 3 Receive 1 +	NA	—	—
G14	GND	Power Ground	PWR GND	—	—
G15	USB3_LSRX	USB 4 Receive channel 3	NA	PD	
G16	USB3_LSTX	USB 4 Transmit channel 3	NA	PD	
G17	USB2_LSRX	USB 4 Receive channel 2	NA	PD	
G18	USB2_LSTX	USB 4 Transmit channel 2	NA	PD	
G19	PEG_LANE_REV#	PEG lane reversal input strap	I-open/GND	PU 100k	
G20	GND	Power Ground	PWR GND	—	—
G21	PCIe40_RX-	PCI Express Lane 40 Receive - Group 2	NA	—	—
G22	PCIe40_RX+	PCI Express Lane 40 Receive + Group 2	NA	—	—
G23	GND	Power Ground	PWR GND	—	—
G24	PCIe41_RX-	PCI Express Lane 41 Receive - Group 2	NA	—	—
G25	PCIe41_RX+	PCI Express Lane 41 Receive + Group 2	NA	—	—
G26	GND	Power Ground	PWR GND	—	—
G27	PCIe42_RX-	PCI Express Lane 42 Receive - Group 2	NA	—	—
G28	PCIe42_RX+	PCI Express Lane 42 Receive + Group 2	NA	—	—
G29	GND	Power Ground	PWR GND	—	—
G30	PCIe43_RX-	PCI Express Lane 43 Receive - Group 2	NA	—	—
G31	PCIe43_RX+	PCI Express Lane 43 Receive + Group 2	NA	—	—
G32	GND	Power Ground	PWR GND	—	—
G33	PCIe44_RX-	PCI Express Lane 44 Receive - Group 2	NA	—	—
G34	PCIe44_RX+	PCI Express Lane 44 Receive + Group 2	NA	—	—
G35	GND	Power Ground	PWR GND	—	—
G36	PCIe45_RX-	PCI Express Lane 45 Receive - Group 2	NA	—	—
G37	PCIe45_RX+	PCI Express Lane 45 Receive + Group 2	NA	—	—

Pin	Signal	Description	Type	Termination	Comment
G38	GND	Power Ground	PWR GND	—	—
G39	PCIe46_RX-	PCI Express Lane 46 Receive - Group 2	NA	—	—
G40	PCIe46_RX+	PCI Express Lane 46 Receive + Group 2	NA	—	—
G41	GND	Power Ground	PWR GND	—	—
G42	PCIe47_RX-	PCI Express Lane 47 Receive - Group 2	NA	—	—
G43	PCIe47_RX+	PCI Express Lane 47 Receive + Group 2	NA	—	—
G44	GND	Power Ground	PWR GND	—	—
G45	PCIe24_RX-	PCI Express Lane 24 Receive - Group 1	NA	—	—
G46	PCIe24_RX+	PCI Express Lane 24 Receive + Group 1	NA	—	—
G47	GND	Power Ground	PWR GND	—	—
G48	PCIe25_RX-	PCI Express Lane 25 Receive - Group 1	NA	—	—
G49	PCIe25_RX+	PCI Express Lane 25 Receive + Group 1	NA	—	—
G50	GND	Power Ground	PWR GND	—	—
G51	PCIe26_RX-	PCI Express Lane 26 Receive - Group 1	NA	—	—
G52	PCIe26_RX+	PCI Express Lane 26 Receive + Group 1	NA	—	—
G53	GND	Power Ground	PWR GND	—	—
G54	PCIe27_RX-	PCI Express Lane 27 Receive - Group 1	NA	—	—
G55	PCIe27_RX+	PCI Express Lane 27 Receive + Group 1	NA	—	—
G56	GND	Power Ground	PWR GND	—	—
G57	PCIe28_RX-	PCI Express Lane 28 Receive - Group 1	NA	—	—
G58	PCIe28_RX+	PCI Express Lane 28 Receive + Group 1	NA	—	—
G59	GND	Power Ground	PWR GND	—	—
G60	PCIe29_RX-	PCI Express Lane 29 Receive - Group 1	NA	—	—
G61	PCIe29_RX+	PCI Express Lane 29 Receive + Group 1	NA	—	—
G62	GND	Power Ground	PWR GND	—	—
G63	PCIe30_RX-	PCI Express Lane 30 Receive - Group 1	NA	—	—
G64	PCIe30_RX+	PCI Express Lane 30 Receive + Group 1	NA	—	—
G65	GND	Power Ground	PWR GND	—	—
G66	PCIe31_RX-	PCI Express Lane 31 Receive - Group 1	NA	—	—

Pin	Signal	Description	Type	Termination	Comment
G67	PCIe31_RX+	PCI Express Lane 31 Receive + Group 1	NA	—	—
G68	GND	Power Ground	PWR GND	—	—
G69	RSVD			—	—
G70	RSVD			—	—
G71	GND	Power Ground	PWR GND	—	—
G72	CSI0_RX0-	CSI0 Pair 0 Receive -	I-1.2	—	—
G73	CSI0_RX0+	CSI0 Pair 0 Receive +	I-1.2	—	—
G74	GND	Power Ground	PWR GND	—	—
G75	CSI0_RX1-	CSI0 Pair 1 Receive -	I-1.2	—	—
G76	CSI0_RX1+	CSI0 Pair 1 Receive +	I-1.2	—	—
G77	GND	Power Ground	PWR GND	—	—
G78	CSI0_RX2-	CSI0 Pair 2 Receive -	I-1.2	—	—
G79	CSI0_RX2+	CSI0 Pair 2 Receive +	I-1.2	—	—
G80	GND	Power Ground	PWR GND	—	—
G81	CSI0_RX3-	CSI0 Pair 3 Receive -	I-1.2	—	—
G82	CSI0_RX3+	CSI0 Pair 3 Receive +	I-1.2	—	—
G83	GND	Power Ground	PWR GND	—	—
G84	CSI0_CLK-	CSI0 Clock input -	I-1.2	—	—
G85	CSI0_CLK+	CSI0 Clock input +	I-1.2	—	—
G86	GND	Power Ground	PWR GND	—	—
G87	CSI0_I2C_CLK	CSI-2 Mode: I2C Clock line	O-1.8	PU	—
G88	CSI0_I2C_DAT	CSI-2 Mode: I2C Data line	I/O-1.8	PU	—
G89	CSI0_MCLK	CSI Master Clock for CSI0	O-1.8	—	—
G90	CSI0_RST#	CSI0 Reset signal	O-1.8	—	—
G91	CSI0_ENA	CSI0 Enable singal	O-1.8	—	—
G92	GND	Power Ground	PWR GND	—	—
G93	RSVD			—	—
G94	RSVD			—	—
G95	GND	Power Ground	PWR GND	—	—
G96	ETH0-1_I2C_CLK	ETH 0-1 I2C clock signal	NA	—	—
G97	ETH0-1_I2C_DAT	ETH 0-1 I2C data signal	NA	—	—
G98	ETH0-1_PHY_INT#	Active low interrupt signal from ETH ports 0-1	NA	—	—
G99	ETH0-1_INT#	Active low interrupt signal from IO Port expanders for ETH	NA	—	—
G100	PCIe_WAKE_OUT0#	PCIe wake request signal	NA	—	—

Table 46: Connector J2 Pins G1 - G100

4.4.4 Pins H1 - H100

Pin	Signal	Description	Type	Termination	Comment
H1	GND	Power Ground	PWR GND	—	—
H2	USB2_SSTX0-	USB Super Speed Pair 2 Transmit 0 -	O USB SS	—	—

Pin	Signal	Description	Type	Termination	Comment
H3	USB2_SSTX0+	USB Super Speed Pair 2 Transmit 0 +	O USB SS	—	—
H4	GND	Power Ground	PWR GND	—	—
H5	USB2_SSTX1-	USB Super Speed Pair 2 Transmit 1 -	NA	—	—
H6	USB2_SSTX1+	USB Super Speed Pair 2 Transmit 1 +	NA	—	—
H7	GND	Power Ground	PWR GND	—	—
H8	USB3_SSTX0-	USB Super Speed Pair 3 Transmit 0 -	O USB SS	—	—
H9	USB3_SSTX0+	USB Super Speed Pair 3 Transmit 0 +	O USB SS	—	—
H10	GND	Power Ground	PWR GND	—	—
H11	USB3_SSTX1-	USB Super Speed Pair 3 Transmit 1 -	NA	—	—
H12	USB3_SSTX1+	USB Super Speed Pair 3 Transmit 1 +	NA	—	—
H13	GND	Power Ground	PWR GND	—	—
H14	USB2_AUX-	USB4 DP Aux channel 2 -	NA	—	—
H15	USB2_AUX+	USB4 DP Aux channel 2 -	NA	—	—
H16	GND	Power Ground	PWR GND	—	—
H17	USB3_AUX-	USB4 DP Aux channel 3 -	NA	—	—
H18	USB3_AUX+	USB4 DP Aux channel 3 -	NA	—	—
H19	GND	Power Ground	PWR GND	—	—
H20	PCIe40_TX-	PCI Express Lane 40 Transmit - Group 2	NA	—	—
H21	PCIe40_TX+	PCI Express Lane 40 Transmit + Group 2	NA	—	—
H22	GND	Power Ground	PWR GND	—	—
H23	PCIe41_TX-	PCI Express Lane 41 Transmit - Group 2	NA	—	—
H24	PCIe41_TX+	PCI Express Lane 41 Transmit + Group 2	NA	—	—
H25	GND	Power Ground	PWR GND	—	—
H26	PCIe42_TX-	PCI Express Lane 42 Transmit - Group 2	NA	—	—
H27	PCIe42_TX+	PCI Express Lane 42 Transmit + Group 2	NA	—	—
H28	GND	Power Ground	PWR GND	—	—
H29	PCIe43_TX-	PCI Express Lane 43 Transmit - Group 2	NA	—	—
H30	PCIe43_TX+	PCI Express Lane 43 Transmit + Group 2	NA	—	—
H31	GND	Power Ground	PWR GND	—	—
H32	PCIe44_TX-	PCI Express Lane 44 Transmit - Group 2	NA	—	—
H33	PCIe44_TX+	PCI Express Lane 44 Transmit + Group 2	NA	—	—
H34	GND	Power Ground	PWR GND	—	—
H35	PCIe45_TX-	PCI Express Lane 45 Transmit - Group 2	NA	—	—
H36	PCIe45_TX+	PCI Express Lane 45 Transmit + Group 2	NA	—	—
H37	GND	Power Ground	PWR GND	—	—
H38	PCIe46_TX-	PCI Express Lane 46 Transmit - Group 2	NA	—	—
H39	PCIe46_TX+	PCI Express Lane 46 Transmit + Group 2	NA	—	—
H40	GND	Power Ground	PWR GND	—	—
H41	PCIe47_TX-	PCI Express Lane 47 Transmit - Group 2	NA	—	—

Pin	Signal	Description	Type	Termination	Comment
H42	PCIe47_TX+	PCI Express Lane 47 Transmit + Group 2	NA	—	—
H43	GND	Power Ground	PWR GND	—	—
H44	PCIe24_TX-	PCI Express Lane 24 Transmit - Group 1	NA	—	—
H45	PCIe24_TX+	PCI Express Lane 24 Transmit + Group 1	NA	—	—
H46	GND	Power Ground	PWR GND	—	—
H47	PCIe25_TX-	PCI Express Lane 25 Transmit - Group 1	NA	—	—
H48	PCIe25_TX+	PCI Express Lane 25 Transmit + Group 1	NA	—	—
H49	GND	Power Ground	PWR GND	—	—
H50	PCIe26_TX-	PCI Express Lane 26 Transmit - Group 1	NA	—	—
H51	PCIe26_TX+	PCI Express Lane 26 Transmit + Group 1	NA	—	—
H52	GND	Power Ground	PWR GND	—	—
H53	PCIe27_TX-	PCI Express Lane 27 Transmit - Group 1	NA	—	—
H54	PCIe27_TX+	PCI Express Lane 27 Transmit + Group 1	NA	—	—
H55	GND	Power Ground	PWR GND	—	—
H56	PCIe28_TX-	PCI Express Lane 28 Transmit - Group 1	NA	—	—
H57	PCIe28_TX+	PCI Express Lane 28 Transmit + Group 1	NA	—	—
H58	GND	Power Ground	PWR GND	—	—
H59	PCIe29_TX-	PCI Express Lane 29 Transmit - Group 1	NA	—	—
H60	PCIe29_TX+	PCI Express Lane 29 Transmit + Group 1	NA	—	—
H61	GND	Power Ground	PWR GND	—	—
H62	PCIe30_TX-	PCI Express Lane 30 Transmit - Group 1	NA	—	—
H63	PCIe30_TX+	PCI Express Lane 30 Transmit + Group 1	NA	—	—
H64	GND	Power Ground	PWR GND	—	—
H65	PCIe31_TX-	PCI Express Lane 31 Transmit - Group 1	NA	—	—
H66	PCIe31_TX+	PCI Express Lane 31 Transmit + Group 1	NA	—	—
H67	GND	Power Ground	PWR GND	—	—
H68	RSVD			—	—
H69	RSVD			—	—
H70	GND	Power Ground	PWR GND	—	—
H71	CSI1_RX0-	CSI1 Pair 0 Receive -	I-1.2	—	—
H72	CSI1_RX0+	CSI1 Pair 0 Receive +	I-1.2	—	—
H73	GND	Power Ground	PWR GND	—	—
H74	CSI1_RX1-	CSI1 Pair 1 Receive -	I-1.2	—	—
H75	CSI1_RX1+	CSI1 Pair 1 Receive +	I-1.2	—	—
H76	GND	Power Ground	PWR GND	—	—
H77	CSI1_RX2-	CSI1 Pair 2 Receive -	I-1.2	—	—
H78	CSI1_RX2+	CSI1 Pair 2 Receive +	I-1.2	—	—
H79	GND	Power Ground	PWR GND	—	—

Pin	Signal	Description	Type	Termination	Comment
H80	CSI1_RX3-	CSI1 Pair 3 Receive -	I-1.2	—	—
H81	CSI1_RX3+	CSI1 Pair 3 Receive +	I-1.2	—	—
H82	GND	Power Ground	PWR GND	—	—
H83	CSI1_CLK-	CSI1 Clock input -	I-1.2	—	—
H84	CSI1_CLK+	CSI1 Clock input +	I-1.2	—	—
H85	GND	Power Ground	PWR GND	—	—
H86	CSI1_I2C_CLK	CSI-2 Mode: I2C Clock line	O-1.8	PU	—
H87	CSI1_I2C_DAT	CSI-2 Mode: I2C Data line	I/O-1.8	PU	—
H88	CSI1_MCLK	CSI Master Clock for CSI1	O-1.8	—	—
H89	CSI1_RST#	CSI0 Reset signal	O-1.8	—	—
H90	CSI1_ENA	CSI0 Enable singal	O-1.8	—	—
H91	GND	Power Ground	PWR GND	—	—
H92	PCIe_REFCLKIN0-	PCIe reference clock input 0 -	NA	—	—
H93	PCIe_REFCLKIN0+	PCIe reference clock input 0 +	NA	—	—
H94	GND	Power Ground	PWR GND	—	—
H95	PCIe_REFCLKIN1-	PCIe reference clock input 1 -	NA	—	—
H96	PCIe_REFCLKIN1+	PCIe reference clock input 1 +	NA	—	—
H97	GND	Power Ground	PWR GND	—	—
H98	ETH0-1_MDIO_CLK	ETH 0-1 clock signal for Management Data I/O interface	NA	—	—
H99	ETH0-1_MDIO_DAT	ETH 0-1 Management Data I/O interface mode	NA	—	—
H100	PCIe_WAKE_OUT1#	PCIe wake request signal	NA		

Table 47: Connector J2 Pins H1 - H100

5. UEFI BIOS

5.1 Starting the UEFI BIOS

The COMh-caRP uses a Kontron-customized, pre-installed and configured version of AMI Aptio® V BIOS based on the Unified Extensible Firmware Interface (UEFI) specification and the Intel® Platform Innovation Framework for EFI.
The UEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the COMh-caRP.

This chapter provides an overview of the BIOS and its setup. A more detailed listing and description of all BIOS setup nodes can be found in the BIOS file package available on our Customer Section. Please register there to get access to BIOS downloads and Product Change Notifications.

The UEFI BIOS comes with a Setup program that provides quick and easy access to the individual function settings for control or modification of the default configuration. The Setup program allows access to various menus resp. sub-menus that provide the specific functions.
To start the UEFI BIOS Setup program, follow the steps below:

1. Power on the board
2. Wait until the first characters appear on the screen (POST messages or splash screen)
3. Press the <DEL> key
4. If the UEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password
5. The Setup menu appears

5.2 Navigating the UEFI BIOS

The COMh-caRP UEFI BIOS Setup program uses a hot key navigation system with a corresponding legend bar displayed on the setup screens. The following table provides a list of navigation hot keys available in the legend bar.

Hot Key	Description
<F1>	<F1> key invokes the General Help window
↔	<Minus> key selects the next lower value within a field
<+>	<Plus> key selects the next higher value within a field
<F2>	<F2> key loads previous values
<F3>	<F3> key loads optimized defaults
<F4>	<F4> key Saves and Exits
<←> or <→>	<Left/Right> arrows select major Setup menus on menu bar, for example, Main or Advanced
<↑> or <↓>	<Up/Down> arrows select fields in the current menu, for example, Setup function or sub-screen
<ESC>	<ESC> key exits a major Setup menu and enters the Exit Setup menu. Pressing the <ESC> key in a sub-menu displays the next higher menu level
<RETURN>	<RETURN> key executes a command or selects a sub-menu

Table 48: Navigation Hot Keys Available in the Legend Bar

5.3 Setup Menus

The Setup utility features a selection bar at the top of the screen that lists the menus

Figure 9: Setup Menu Selection Bar

The Setup menus available for the COMh-caRP are:

- Main
- Advanced
- Chipset
- Security
- Boot
- Save & Exit

The currently active menu is highlighted in grey, the currently active UEFI BIOS Setup item in white. Use the left and right arrow keys to select the Setup menu.
Each Setup menu provides two main frames. The left frame displays all available functions and configurable ones are displayed in blue. Functions displayed in grey provide information about the status or the operational configuration.

5.4 Getting Help

The right frame displays a help window. The help window provides an explanation of the respective function.

5.5 UEFI Shell

The Kontron UEFI BIOS features a built-in and enhanced version of the UEFI Shell. For a detailed description of the available standard shell scripting, refer to the EFI Shell User Guide. For a detailed description of the available standard shell commands, refer to the EFI Shell Command Manual. Both documents can be downloaded from the EFI and Framework Open Source Community homepage: http://sourceforge.net/projects/efi-shell/files/documents/.

Kontron UEFI BIOS does not provide all shell commands described in the EFI Shell Command Manual.

5.5.1 Entering the UEFI Shell

To enter the UEFI Shell, follow the steps below:

1. Power on the board
2. Press the <F7> key (instead of <DEL>) to display a choice of boot devices
3. Select 'UEFI: Built-in EFI shell'

```
UEFI Interactive Shell v2.2
EDK II / Kontron add-on v0.3
UEFI v2.80 (American Megatrands, 0x0005001A)
map: No mapping found.
```

1. Press the <ESC> key within 5 seconds to skip startup.nsh or any other key to continue
2. The output produced by the device-mapping table can vary depending on the board's configuration
3. If the <ESC> key is pressed before the 5 second timeout elapses, the shell prompt is shown:

```
Shell>
```

5.5.2 Exiting the UEFI Shell

To exit the UEFI Shell, follow one of the steps below:

- Use the **exit** UEFI Shell command to select the boot device, in the Boot menu, that the OS boots from
- Reset the board using the **reset** UEFI Shell command
- Press the reset button of the board or power down/up the board

5.6 UEFI Shell Scripting

5.6.1 Startup Scripting

If the <ESC> key is not pressed and the timeout has run out, then the UEFI Shell automatically tries to execute some startup scripts. The UEFI shell searches for scripts and executes them in the following order:

1. Initially searches for Kontron flash-stored startup script
2. If there is no Kontron flash-stored startup script present, then the UEFI-specified **startup.nsh** script is used. This script must be located on the root of any of the attached FAT-formatted disk drives
3. If none of the startup scripts are present or the startup script terminates then the default boot order is continued

5.6.2 Create a Startup Script

Startup scripts can be created using the UEFI Shell built-in editor **edit** or under any OS with a plain text editor of your choice.

5.6.3 Example of Startup Scripts

Execute Shell Script on other Harddrive

This example (**startup.nsh**) executes the shell script named **bootme.nsh** located in the root of the first detected disk drive (**fs0**).

```
fs0:
bootme.nsh
```

5.7 Firmware Update

Firmware updates are typically delivered as a ZIP archive. Please find the latest available BIOS-ZIP archive on Kontron's Customer Section. Further information about the firmware update procedure can be found in the included “flash_instruction.txt”-file.

Register to Kontron's Customer Section to get access to BIOS downloads, additional documentation and Product Change Notification service.

6. Technical Support

For technical support contact our Support Department:

E-Mail:	support@kontron.com
Phone:	+49 (0) 821 4086-888

Make sure you have the following information available when you call:

- Product ID Number (PN)
- Serial Number (SN)
- Module's revision
- Operating System and Kernel/Build version
- Software modifications
- Additional connected hardware/full description of hardware set up

The Serial Number can be found on the Type Label, located on the product.

Be ready to explain the nature of your problem to the service technician.

6.1 Warranty

Due to their limited service life, parts that by their nature are subject to a particularly high degree of wear (wearing parts) are excluded from the warranty beyond that provided by law.

If there is a protection label on your product, then the warranty is lost if the product is opened.

6.2 Returning Defective Material

All equipment returned to Kontron must have a Return of Material Authorization (RMA) number assigned exclusively by Kontron. Kontron cannot be held responsible for any loss or damage caused to the equipment received without an RMA number. The buyer accepts responsibility for all freight charges for the return of goods to Kontron's designated facility. Kontron will pay the return freight charges back to the buyer's location in the event that the equipment is repaired or replaced within the stipulated warranty period. Follow these steps before returning any product to Kontron:

1. Visit the RMA Information website: RMA Information - Kontron Europe and Asia

2. Download the RMA Request sheet for **Kontron Europe GmbH** and fill out the form. Take care to include a short detailed description of the observed problem or failure and to include the product identification information (Name of product, Product Number and Serial Number). If a delivery includes more than one product, fill out the above information in the RMA Request form for each product.
3. Send the completed RMA-Request form to the fax or email address given below at Kontron Europe GmbH.
   Kontron will provide an RMA-Number.

   Kontron Europe GmbH
   RMA Support
   Phone: +49 (0) 821 4086-0
   Fax: +49 (0) 821 4086-111
   Email: service@kontron.com

4. The goods for repair must be packed properly for shipping, considering shock and ESD protection.

   

   Goods returned to Kontron Europe GmbH in non-proper packaging will be considered as customer caused faults and cannot be accepted as warranty repairs.

5. Include the RMA-Number with the shipping paperwork and send the product to the delivery address provided in the RMA form or received from Kontron RMA Support.

7. Document Revision

The following table shows the revision of this document.

Revision	Author	Date	Comment
0.1	UMA	2023-06-20	initial preliminary release- derived from COMh-caAP
0.2	UMA	2023-07-19	updated ripple voltage requirement
0.3	UMA	2023-08-02	corrected PEG speed

Table 49: Document Revision Table