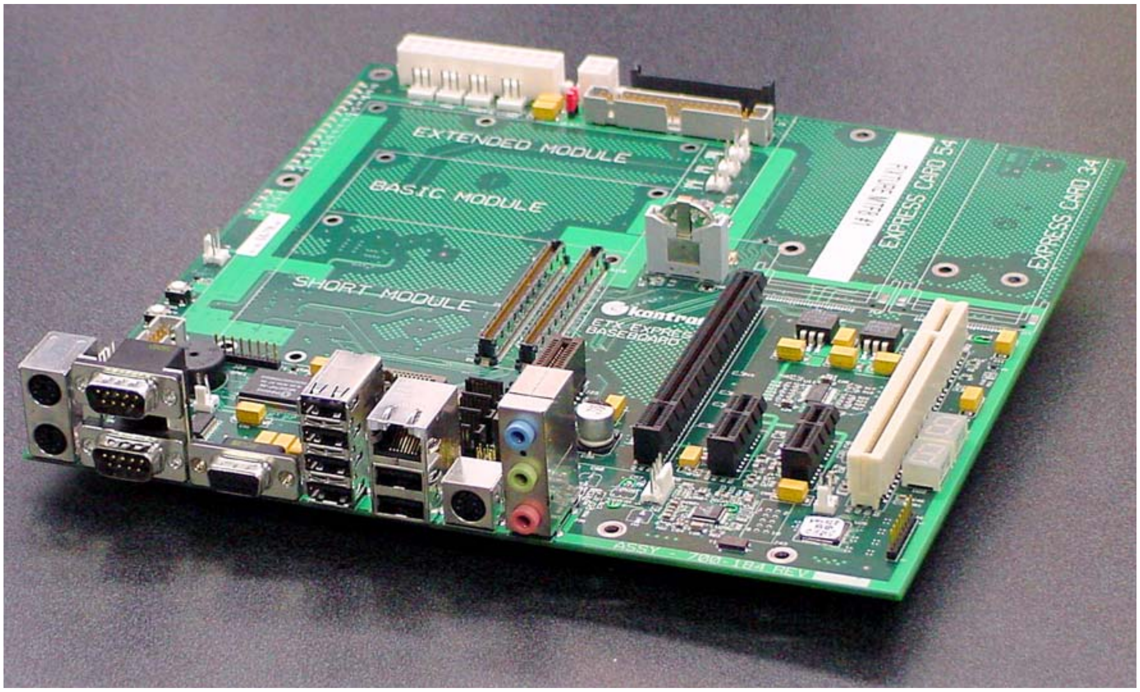

Brownsville ETXexpress Carrier Board

COM Express™ Compatible

Design Guide for ETXexpress Carrier Boards

Rev. 1.2 / April 20, 2006

kontron

Acknowledgements

The following Kontron America employees contributed to the creation of the
Design Guide for ETXexpress Carrier Boards:

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Tables

1 Introduction

1.1 COM Express™ Specification and ETXexpress Design Guide

This Design Guide for ETXexpress Carrier Boards is one of three principal references for designing ETXexpress Carrier Boards, which carry ETXexpress Modules. All Kontron ETXexpress Modules and Carrier Boards are fully compatible with the COM Express™ Specification, which Kontron played a lead role in developing.

The three references include:

- The COM Express™ Specification, which defines the two Module Form Factors (Basic and Extended), pin-outs, and signals. We suggest that you read this document first. You can find the COM Express™ Specification on the PICMG (PCI Industrial Computer Manufacturers Group) Web site: www.**picmg**.org. There is a fee for the document. All Kontron ETXexpress Modules follow the COM Express™ Specification.

- The Kontron Design Guide for ETXexpress Carrier Boards serves as a general guide for Carrier Board designs. The Design Guide focuses on maximum flexibility to accommodate a range of ETXexpress Modules. The Kontron ETXexpress Design Guide explores the requirements of the COM Express™ Specification and provides recommendations on how to design ETXexpress Carrier Boards to support features of Kontron's ETXexpress Modules.

  The ETXexpress Design Guide provides schematic examples and information on standard I/O interfaces, connections, and routing. The guide also offers ideas to maximize the design potential of ETXexpress Carrier Boards to accommodate all Kontron ETXexpress Modules.

  Kontron has created an ETXexpress Carrier Board reference design called Project Brownsville. The fully functional Carrier Board comes in a MicroATX Form Factor. Project Brownsville supports most of the Module features that are defined in the COM Express™ Specification.

- ETXexpress Module User Guides document specifications and features of an individual ETXexpress Module. You can find all user guides for ETXexpress Modules on the Kontron Web site.

1.2 Acronyms and Terms

Terms and acronyms used in this document are defined in the table below. For information on specifications, see Appendix G. For a bibliography of reference materials, see Appendix H.

Table 1-1: Terms and Definitions

Term	Definition
AC '97	Audio Coder-Decoder 1997 – an Intel-defined format to digitally encode and decode audio signals.
ADD2 Card	Advanced Digital Display (2nd Generation) Card – an Intel-defined slot card that fits in a x16 PCI Express graphics (PEG) slot but is used with SDVO signals rather than PCIe. SDVO signals are multiplexed with PEG on some chipsets and in the COM Express™ Specification. ADD2 cards convert the SDVO data stream to display formats such as TMDS, DVI, LVDS or TV encoded.
ADD2-N ADD2-R	Normal pin-out ADD2 card. Reverse pin-out ADD2 card.
ATX	"Advanced Technology eXtended" – an Intel-defined form factor for motherboards.
Base Board	An application-specific PC board that accepts an ETXexpress Module. The Base Board is alternatively referred to as a Carrier Board. Carrier Board is the preferred terminology.
Basic Form Factor	A form factor with a module size of 125mm x 95mm as defined by the PICMG. This form factor is used in space-constrained systems and typically has a single SO-DIMM memory.
BIOS	Basic Input Output System. This software runs from non-volatile memory on the Module or on the Carrier Board, initializes a system, and allocates resources before the operating system takes over.
Carrier Board	An application-specific PC board that accepts an ETXexpress Module. The Carrier Board is alternatively referred to as a Base Board. Carrier Board is the preferred terminology.
COM Express™	A form-factor standard for small modules as defined by the PICMG for mezzanine-style CPU modules that incorporate a rich set of high-speed serial interfaces such as PCIe, SATA, USB, GBE, and flat-panel LVDS. The PICMG refers to the standard as both COM.0 and COM Express™.
CRT	Cathode Ray Tube
Device Down Device Up	"Device Down" refers to a target IC "down" on the Carrier Board as opposed to being "up" on a slot card. "Device Up" refers to a target IC "up" on a slot card as opposed to being "down" on the Carrier Board.
DIMM	Dual In-line Memory Module – a memory socket format defined by JEDEC. The format is suitable for desktop and workstation computer systems.
DVI-A DVI-D	Digital Video Interface – Analog format input to digital display Digital Video Interface – Digital format input to digital display
EDID	Extended Display Identification Data – This VESA standard identifies display parameters to the host system by using a dedicated I^2C bus.
EMI	Electromagnetic Interference
ETXexpress™	The original Kontron name for modules that follow the Com Express™ Specification for small form factors as defined by PICMG. ETXexpress also is known as COM Express™. ETXexpress and COM Express™ are used interchangeably in this document.
Express Card	A hot-pluggable card has a small form factor and is used for mobile computing. Express Card is the Card Bus successor and uses USB or PCIe x1 as the I/O interface. The PCMCIA consortium maintains the Express Card standard.
Express Module	A PCIe-based, modular form-factor card promoted by the PCI-SIG for the server and workstation market.
Extended Form Factor	One of two principle sizes for COM Express™ form factors as approved by PICMG. The other form factor is called Basic. The 155mm x 110mm Extended Module is used in systems that require more memory than what smaller Basic Form Factor designs (125mm x 95mm) can provide. An Extended Form Factor Module typically accepts two full-size DIMMs.
FAE	Field Application Engineer
FFC	Flat Foil Connector
FPD	Flat Panel Display
FPGA	Field Programmable Gate Array
GBE	Gigabit Ethernet

Term	Definition
GND	Ground potential
GPI GPIO GPO	General Purpose Input General Purpose Input Output General Purpose Output
HD Audio	High Definition Audio
Hot Swap Hot Plug	Inserting or removing a device from the system without powering the system down.
IC	Integrated Circuit
I^2C	Inter Integrated Circuit – a signaling scheme that uses two wires to allow communication between integrated circuits. This reads and loads register values.
IDE	Integrated Device Electronics – IDE is synonymous with PATA and is a hard-disk standard that uses a single-ended, parallel-bus interconnect.
JEDEC	Industry-standards organization (originally, the Joint Electron Device Engineering Council). JEDEC standards cover memory modules, memory sockets, IC packaging, memory chip organizations, and more.
JIDA	Jumptec Intelligent Device Architecture. A set of BIOS extensions defined for Kontron modular computers.
JILI	Jumptec Intelligent LVDS Interface. Kontron hardware / software standard for interfacing embedded computers to flat-panel displays.
LAN	Local Area Network
LDI	LVDS Display Interface
Legacy Free	A system without a PS2 keyboard / mouse controller. The keyboard and mouse, if used, are plugged into USB ports.
LPC	Low Pin Count interface – an Intel-defined standard for attaching low-bandwidth peripherals such as serial ports, keyboard controllers, and Super I/Os to a computer system. As the name implies, few pins are involved, making LPC easy to implement.
LVDS	Low Voltage Differential Signaling. Many modern high-speed interfaces, such as PCIe and SATA, are LVDS interfaces. However, the term LVDS commonly refers to a serialized, differential interface, which is used for flat-panel interfacing. In this document and in the COM Express™ Specification, LVDS refers primarily to a flat-panel interface.
MAC	Media Access Controller – the digital-hardware control section of a LAN implementation.
MicroATX	An Intel-defined, form-factor size for motherboards: 9.6” x 9.6”.
Microstrip	A constant width PCB trace on an outer PCB layer that is a fixed height above a reference plane.
Mils	Unit of length commonly used in PCB layout work: 1/1000th of an inch
Module	A COM Express™-compliant or compatible CPU mezzanine board.
NC	No Connect
NTSC	National Television Standards Committee – refers to the composite, analog video-encoding scheme used in North America.
PAL	Phase Alternating Line. A composite, analog video-encoding scheme used in many areas of Europe.
PATA	Parallel AT Attachment device – synonymous with IDE – a hard-disk standard that uses a single-ended parallel bus interconnect.
PC-AT	Personal Computer – Advanced Technology. Trademarked term introduced in the 1980s by IBM to identify current PC technology.
PCB	Printed Circuit Board
PEG	PCI Express Graphics
PCI	Peripheral Component Interconnect – a parallel bus standard for adding peripheral components to a computer system.
PCI Express™ PCIe™	A high-speed, serialized, peer-to-peer bus standard for adding peripheral components to a computer system. PCI Express (PCIe) is electrically different from PCI, but PCI Express software protocols are backward compatible with PCI.
PCI-SIG	PCI Special Interest Group – a standards organization that maintains the PCI™ and PCI Express™ specifications.
PHY	Physical Layer interface of a LAN implementation. The Physical Layer drives physical media such as the twisted pair cable.
Plane split	A cut in a power or ground plane to isolate two regions of the plane from each other. A power plane often has several regions, including 3.3V, 2.5V, and 1.5V.
PLD	Programmable Logic Device
PICMG	PCI Industrial Computer Manufacturing Group – a non-profit industry trade group that issues and maintains technical standards to manufacturers of embedded and industrial computer boards and systems.

Term	Definition
RJ45	Registered Jack 45 – an 8-pin jack used for 10/100 and GBE LAN connections.
PLL	Phase Locked Loop
RGB	Red Green Blue – color components in a VGA or TFT flat-panel display.
RSVD	Reserved. Leave pins marked RSVD as no-connects.
SAS	Serial Attached SCSI – New-generation, high-speed SCSI hard disks that use serial communication instead of parallel communication.
SATA	Serial AT Attachment device – a high-speed, serial-interconnect standard for hard disks. SATA is electrically quite different from PATA or IDE, but SATA software protocols are backward compatible with PATA.
SDVO	Serialized Digital Video Out. An Intel-defined format to bring serialized digital video out on a high-speed differential interface. SDVO signals are electrically compatible with PCIe and are multiplexed with PCI Express x16 graphics signals on current Intel chipsets such as the 915G and the 945G. SDVO signals are routed to encoder chips from vendors such as Silicon Image.
Smart Battery	A standard describing a uniform software and hardware interface between a host computer system and a battery subsystem (the “Smart Battery”), including charger electronics. The SM Bus serves as the communication path.
SM Bus	System Management (SM) Bus. A two-wire, bidirectional bus (clock and serial data) that is used for system management such as reading parameters from a memory card and reading temperatures and voltages of system components. The SM Bus uses the same signaling scheme as an I^2C bus.
SO-DIMM	Small Outline Dual In-line Memory Module – a memory socket format defined by JEDEC. The format is suitable for small form factor mobile computer systems.
STN	Super Twisted Nematic – a passive, flat-panel display technology that allows low-power consumption displays. TFT displays are usually crisper and brighter than STN, but some situations call for the lower power consumption that STN can offer. STN displays are usually lower resolution (up to 640 x 480) monochrome displays.
Stripline	A constant width internal layer PCB trace that is sandwiched between two reference planes. If the stripline trace is equidistant between the two reference planes, it is said to be symmetric or balanced. If the stripline trace is closer to on of the planes, it is said to be asymmetric or unbalanced.
Super I/O	An integrated circuit that combines common PC I/O functions such as serial ports, floppy disk controllers, parallel ports, and PS2 keyboard and mouse. The Super I/O system interface is typically thru the LPC (Low Pin Count) bus. PCI-based Super I/Os also are available.
TFT	Thin Film Transistor – a reference to a type of flat-panel display with an active transistor at each pixel.
TMDS	Transition Minimized Differential Signaling – a low voltage differential signaling scheme for flat-panel displays that is an alternative to flat-panel LVDS. TMDS uses 8b/10b encoding to achieve DC balance and is used for DVD-D displays.
UL	Underwriter’s Laboratories – an industry trade group concerned with safety.
USB	Universal Serial Bus – A hot-pluggable serial I/O interconnect standard.
VGA	Video Graphics Array
VESA	Video Electronics Standards Association – an industry trade group that issues standards for CRT and flat-panel displays.

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2 COM Express™ Specification

The COM Express™ Specification defines requirements for highly integrated compact modules with standard I/O interfaces and connections, which allows interoperability between multisourced modules. Key capabilities defined in the COM Express™ Specification include support for:

- PCI Express Bus
- PCI Express Graphics (PEG)
- Serial ATA
- USB 2.0
- Gigabit Ethernet

The COM Express™ Specification defines two form factors:

- Basic (125mm x 95mm) Module
- Extended (155mm x 110mm) Module

The mechanical envelope for the Basic Module is defined for low-profile, space-constrained applications. Basic Modules usually use a single horizontal DDR or DDR2 SO-DIMM.

Extended Modules target applications that require more memory and high-performance CPUs and chipsets. Two full-size DIMMs fit on an Extended Module.

Five pin-out Types apply to Basic and Extended form factors:

- Module Type 1 supports a single connector with two rows of pins (220 pins total).
- Module Types 2-5 support two connectors with four rows of pins (440 pins total).

Connector placement and most mounting holes have transparency between Form Factors.

The differences among the Module Types are summarized in Table 2-1.

Table 2-1: Module Type Summary Features

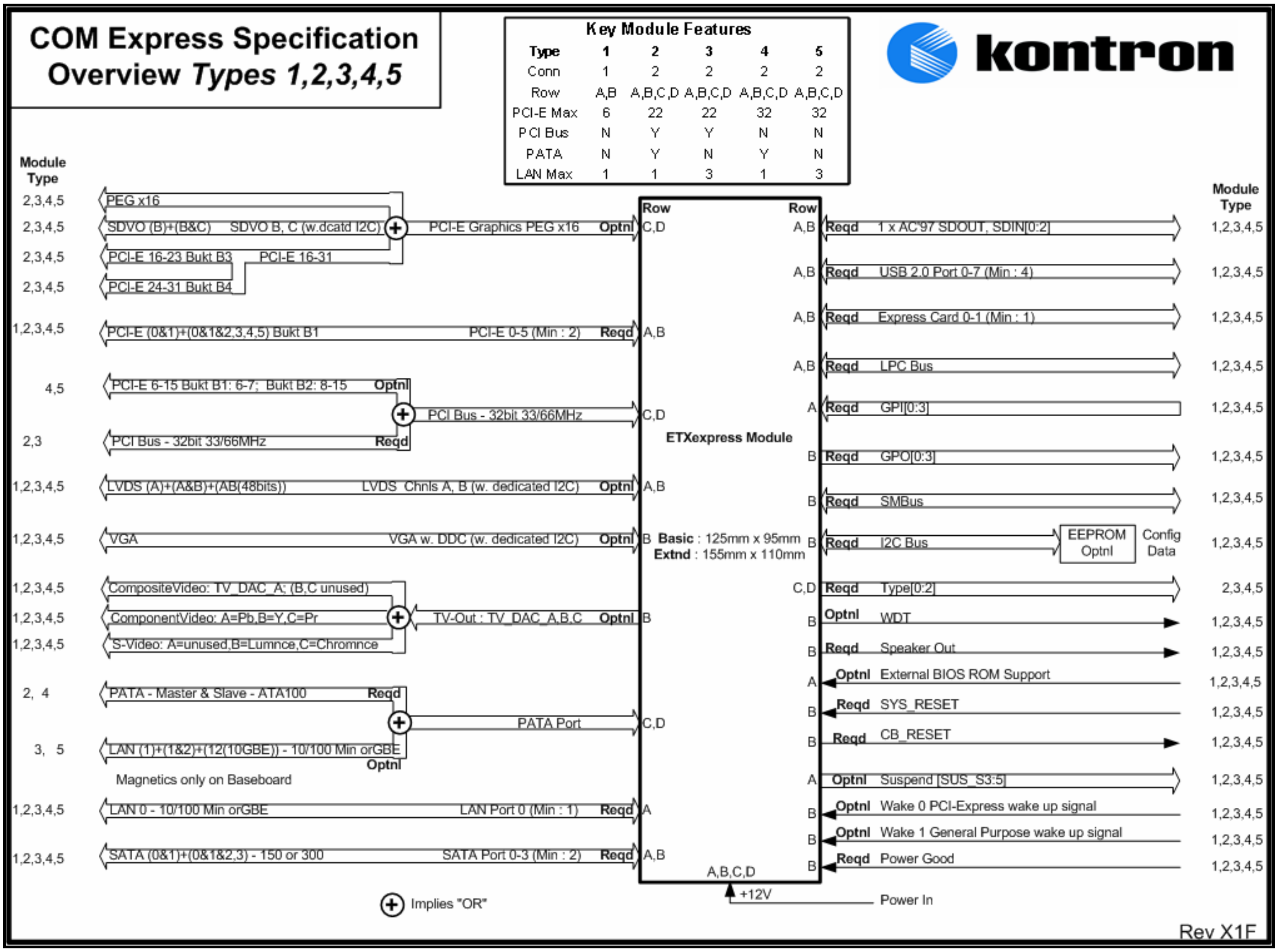
Module Type >	**1**	**2**	**3**	**4**	**5**
Connectors	1	2	2	2	2
Connector Rows	A,B	A,B,C,D	A,B,C,D	A,B,C,D	A,B,C,D
PCIe Lanes (max)	6	22	22	32	32
PCI Bus 32bits	No	Yes	Yes	No	No
PATA - IDE	No	Yes	No	Yes	No
LAN (max)	1	1	3	1	3

2.1 Synopsis

Figure 2-1 below provides a quick overview of the key functionality of ETXexpress Modules as defined in the COM Express™ Specification.

- All Module Types minimally support the following key interfaces:
  - 2 PCI Express (PCIe) Lanes (0 and 1)
  - 1 LAN Port 10/100Base-T (0)
  - 2 SATA Ports (0 and 1)
  - AC’97 Digital
  - 4 USB Ports (0 thru 3)
  - 1 Express Card Control (0)
  - LPC Bus
- Module Types 2 & 3 support the following key interface:
  - 32-bit PCI Bus
- Module Types 2 & 4 support the following key interface:
  - PATA – ATA100
- All Module Types optionally support the following key interfaces:
  - Additional PCI Express (PCIe) Lanes (2 thru 5)
  - LVDS Channels (A,B)
  - VGA
  - TV-Out (Composite, Component, or S- Video)
- Module Types 2 thru 5 optionally support the following key interface:
  - PCI Express Graphics (PEG) are configured for one of the following:
    PCIe Graphics (x16), SDVO (B,C) or PCI Express (PCIe) Lanes (16 thru 31)
- Module Types 4 & 5 optionally support the following key interface:
  - Additional PCI Express Lanes (6 thru 15)

Figure 2-1: COM Express™ Module Capabilities Block Diagram



3 ETXexpress Carrier Board Design

3.1 Schematic Design Reference Materials

Kontron has created an ETXexpress design for a Carrier Board called Project Brownsville. Brownsville is implemented in the MicroATX form factor. The Carrier Board accepts Kontron’s ETXexpress Basic and Extended Modules that have Type 1 and Type 2 pin-outs. The Carrier Board does not accept Modules that have Type 3, Type 4, and Type 5 pin-outs.

The Carrier Board’s range of features include:

- PCI Express x16 Graphics slot / SDVO slot
- Two general-purpose PCI Express (PCIe) x1 slots
- Two Express Card slots
- PCI slot
- LPC slot
- On-board Super I/O and connectors for USB, SATA, IDE, VGA, and LVDS

The full specification and a summary of features for Brownsville can be found in Appendix D.
The complete schematic diagram for the Brownsville design can be found in Appendix E. While no guarantee of correctness is made, the schematics in Appendix E come directly from a design that is in production.

Chapters 4 thru 19 illustrate specific COM Express™ interfaces through tables and schematic diagrams. Design suggestions and routing considerations accompany each diagram. Many, but not all, come from proven designs. The schematic diagrams are believed to be correct but are not guaranteed to be error-free.

3.2 Schematic Conventions

Figure 3-1 and Figure 3-2 explain the meaning of the symbols and power-naming conventions that are used in the schematics found throughout this document.

Figure 3-1: Schematic Conventions

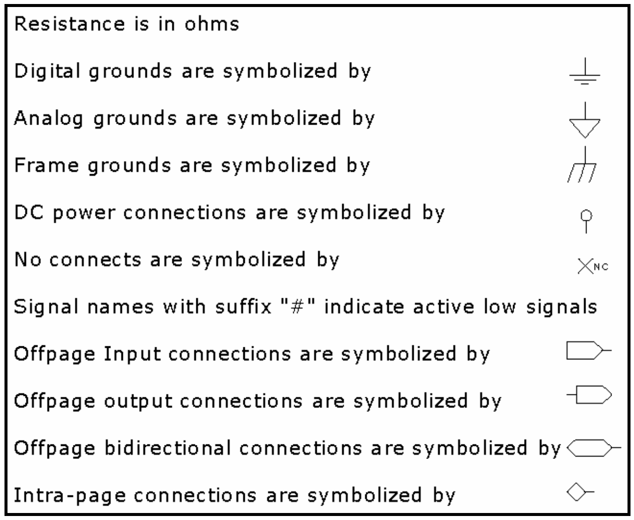


Figure 3-2: Power-naming Conventions

Vx.x_S0 - x.x represents the voltage, S0 is the full power-on state.

Vx.x_S3 - x.x represents the voltage, S3 is the low wake-latency sleep state. The memory of the system is in a low power state.

Vx.x_S4 - x.x represents the voltage, S4 is the lowest power, longest wake-latency sleep state.

Vx.x_S5 - x.x represents the voltage, S5 is the sleep state or soft off state; V5SBY is the only voltage available in this state.

V5SBY - This is the 5V standby voltage.

V12_S0 - This is the 12V that powers the base board PCIe connectors.

VCC_12V - This is 12V used to power the ETX Express module. This is derived from the additional 4-pin connector coming from ATX supplies.

3.3 PCB Design Rules

The COM Express™ Specification provides a rich set of modern, high-speed differential serial interfaces. Designing ETXexpress Carrier Boards is not difficult, but certain design rules must be followed.

The most important design rule is: **route high-speed serial interfaces as differential pairs.** The two lines in the pair must be length-matched and should have uniform, edge-to-edge spacing. They should have a minimum of layer changes. If they do change layers, both lines in the pair should change. The preferred reference plane for the high-speed pairs is a single, continuous GND plane. If the differential pair is referenced to a power plane, avoid routing the pair across a power-plane split.

Design rules for high-speed differential pairs are summarized in Appendix A.

Design rules for single-ended signals are summarized in Appendix B.

3.4 Four-Layer Stack-up

Figure 3-3: Four-Layer Stack-up

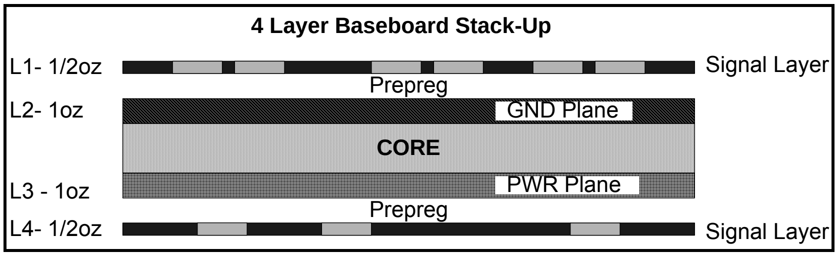


Figure 3-3 above is an example of a four layer stack-up. Layers L1 and L4 are used for signal-routing. Layers L2 and L3 are used for solid ground and power planes respectively.

Microstrips on Layers 1 and 4 reference ground and power planes on Layers 2 and 3 respectively.

In some cases, it may be advantageous to swap the GND and PWR planes. This allows Layer 4 to be GND referenced. Layer 4 is clear of parts and may be the preferred primary routing layer.

3.5 Six-Layer Stack-up

Figure 3-4: Six-Layer Stack-up

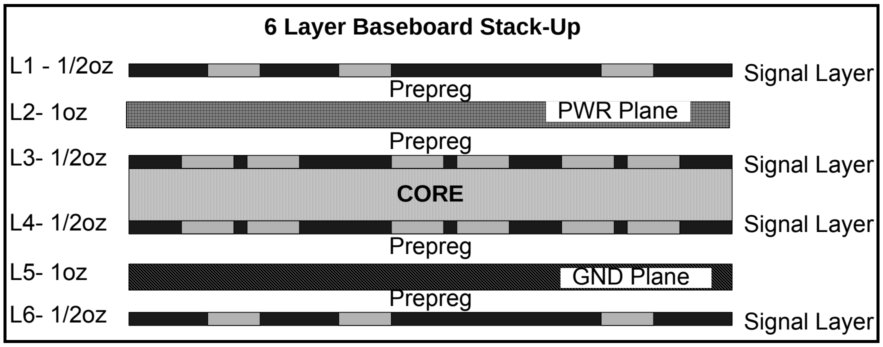


Figure 3-4 above is an example of a six layer stack-up. Layers L1, L3, L4 and L6 are used for signal-routing. Layers L2 and L5 are power and ground planes respectively.

Microstrips on Layers 1 and 6 reference solid ground and power planes on Layers 2 and 5 respectively.

Inner Layers 3 and 4 are asymmetric striplines that are referenced to planes on Layers 2 and 5.

3.6 Eight-Layer Stack-up

Figure 3-5: Eight-Layer Stack-up

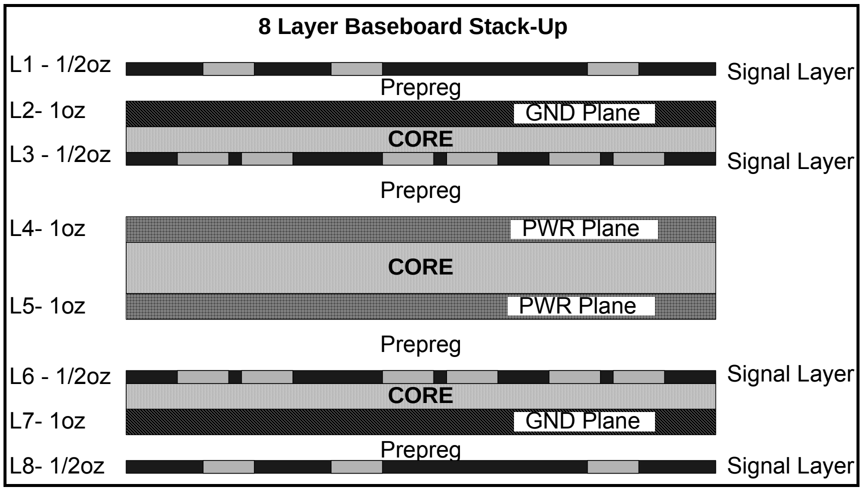


Figure 3-5 above is an example of an eight layer stack-up. Layers L1, L3, L6 and L8 are used for signal-routing. Layers L2 and L7 are solid ground planes, while L4 and L5 are used for power.

Microstrip Layers 1 and 8 reference solid ground planes on Layers 2 and 7 respectively.

Inner signal Layers 3 and 6 are asymmetric striplines that route differential signals. These signals are referenced to Layers 2 and 7 to meet the characteristics impedance target for these traces. To reduce coupling to Layers 4 and 5, specify thicker prepreg to increase layer separation.

3.7 Trace-Impedance Considerations

Most high-speed interfaces used in an ETXexpress design for a Carrier Board are differential pairs that need a well-defined and consistent differential and single-ended impedance. The differential pairs should be edge-coupled (i.e. the two lines in the pair are on the same PCB layer, at a consistent spacing to each other). Broadside coupling (in which the two lines in the pair track each other on different layers) is not recommended for mainstream commercial PCB fabrication.

There are two basic structures used for high-speed differential and single-ended signals. The first is known as a "microstrip", in which a trace or trace pair is referenced to a single ground or power plane. The outer layers of multi-layer PCBs are microstrips. A diagram of a microstrip cross section is shown in Figure 3-6 below.

The second structure is the "stripline" in which a trace or pair of traces is sandwiched between two reference planes, as shown in Figure 3-7 below. If the traces are exactly halfway between the reference planes, then the stripline is said to be symmetric or balanced. Usually the traces are a lot closer to one of the planes than the other (often because there is another, orthogonal, trace layer, which is not shown in Figure 3-7). In this case, the striplines are said to be asymmetric or un-balanced. Inner layer traces on multi-layer PCBs are usually asymmetric striplines.

Before proceeding with a Carrier Board layout, designers should decide on a PCB stack-up and on trace parameters, primarily the trace-width and differential-pair spacing. It is quite a bit harder to change the differential impedance of a trace pair after layout work is done than it is to change the impedance of a single-ended signal. That is because (with reference to Figures 3-6, 3-7, and Table 3-1 below) the geometric factors that have the biggest impact on the impedance of a single-ended trace are H1 and W1. Both H1 and W1 can be manipulated slightly by the PCB vendor. The differential impedance of a trace pair depends primarily on H1, W1 and the pair pitch. A PCB vendor can easily manipulate H1 and W1 but changing the pair pitch cannot generally be done at fabrication time. It is more important for the PCB designer and the Project Engineer to determine the routing parameters for differential pairs ahead of time.

Work with a PCB vendor on a suitable board stack-up and do your own homework using a PCB-impedance calculator. An easy to use and comprehensive calculator is available from Polar Instruments (www.polarinstruments.com). Many PCB vendors use software from Polar Instruments for their calculations. Polar Instruments offers an impedance calculator on a low-cost, per-use basis. To find this, search the Web for a "Polar Instruments subscription". Alternatively, impedance calculators are included in many PCB layout packages, although these are often incomplete when it comes to differential-pair impedances. There also are quite a few free impedance calculators available on the Web. Most are very basic, but they can be useful.

Figure 3-6: Microstrip Cross Section

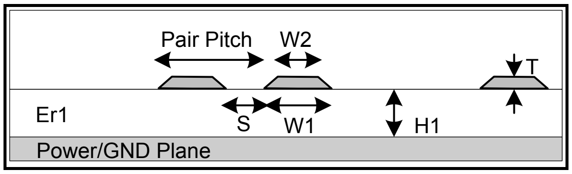


Figure 3-7: Asymmetric Stripline Cross Section

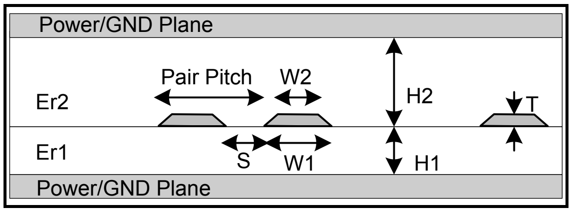


Table 3-1: Microstrip and Stripline Definitions

Symbol	Definition
Er1	Dielectric constant of material between the trace and the reference plane. Increasing Er1 results in a lower trace impedance.
Er2	Dielectric constant of the material between the 2nd reference plane (stripline case only). Usually Er1 and Er2 are the same. Increasing Er2 results in a lower trace impedance.
H1	Distance between the trace lower surface and the closer reference plane. Increasing H1 raises the trace impedance (assuming that H1 is less than H2).
H2	Distance between the trace lower surface and the more distant reference plane (stripline case only). Usually H2 is significantly greater than H1. When this is true, the lower plane shown in the figure is the primary reference plane. Increasing H2 raises the trace impedance.
Pair Pitch	The center-to-center spacing between two traces in a differential pair. Increasing the pair pitch raises the differential trace impedance.
S	The spacing or gap between two traces in a differential pair. The pair pitch is the sum of S and W1. Increasing S raises the differential trace impedance.
T	The thickness of the trace. The thickness of a ½ oz. inner layer trace is about 0.0007 inches. The thickness of a 1 oz. inner layer trace is about 0.0014 inches. Outer layer traces using a given copper weight are thicker, due to plating that is usually done on outer layers. Increasing the trace thickness lowers trace impedance.
W1, W2	W1 is the base thickness of the trace. W2 is the thickness at the top of the trace. The relation between W1 and W2 is called the “etch factor” in the PCB trade. For rough calculations, it can be assumed that W1 = W2. The etch factor is process dependent. W2 is often about 0.001 inches less than W1 for ½ oz inner layer traces For example, a 5 mil (0.005 inch) nominal trace will be 5-mil wide at the bottom and 4-mil wide at the top. Increasing the trace-width lowers trace impedance.

4 ETXexpress Module Connectors

4.1 Connector Descriptions

Descriptions, part numbers, and land patterns for ETXexpress Connectors are provided in the COM Express™ Specification. The discussion below augments the description given in the Specification.

ETXexpress Carrier Boards that implement Pin-out Types 2, 3, 4 or 5 use a pair of 220-pin, 0.5mm-pitch, surface-mount connectors for a total of 440 pins. Each connector has two rows of 110 pins. For the full 440-pin implementation, there are four rows of 110 pins each. The four rows are labeled A, B, C and D in the COM Express™ Specification. The two 220-pin connectors are referred to as the 'A-B' connector and the 'C-D' connector. Only Type 1 Modules use a single 220-pin connector, the 'A-B' connector.

The connectors are from the AMP / Tyco 0.5mm pitch 'Freeheight', or FH family. There may later be alternate suppliers, per the terms imposed on the primary connector vendor by the PICMG. ETXexpress Carrier Board connectors are available in stacking heights of 8mm and 5mm.
The Carrier Board connector is the 'Plug.' (It is a plug in the vendor's terminology; although to some users it looks more like a receptacle). The module connector is the 'Receptacle' in the vendor's terminology. The module is always built with the same connector, the 4mm receptacle ('4H' in the vendor's terminology). The system's stack height is determined by the choice of the Carrier Board connector. The options available in this pin count are 8mm ("8H Plug") and 5mm ("5H Plug").

A pair of 220-pin ETXexpress Carrier-Board connectors is available from the vendor in a bridged configuration in which the two 220-pin connectors are held together during assembly by a disposable bridge. The bridge keeps the two connectors aligned, relative to each other, during assembly. The bridge also has a pad that can be used by pick and place equipment to pick up the connector pair.

4.2 Connector Land Patterns and Alignment

It is extremely important that the designers of Carrier Boards ensure that the ETXexpress connectors have the proper land patterns and that the connectors are aligned correctly. The land pattern is diagrammed in the COM Express™ Specification. Connector alignment is ensured if the peg location holes in the PCB connector pattern are in the correct positions (as shown in the land pattern of the COM Express™ Specification) and if the holes are drilled to the proper size and tolerance by the PCB fabricator.

Land patterns for Carrier Board connectors may be available from Kontron for major PCB CAD systems. Contact your Kontron FAE.

4.3 Connector and Module CAD Symbol Recommendations

The 440-pin COM Express™ connector should be shown in the Carrier Board CAD system as a single schematic symbol and a single PCB symbol, rather than as a pair of 220-pin symbols. This ensures that the relative position of the two 220-pin connectors remains correct as PCB placement for the Carrier Board is done.

It also is very advantageous to extend this concept to include the ETXepress Module outline and the Module mounting holes in the same PCB land pattern. This allows PCB designers to easily move the entire module around to try placement options without losing the relative positions and orientations of the Module connectors, mounting holes, and Module outline.

4.4 Connector Schematics (Type 2 Pin-Out)

The following schematics show available signals for the ETXexpress connector pins for Connector Rows A, B, C and D as defined in the COM Express™ Specification for a Type 2 pin-out. The schematics show available and unused signals. ETXexpress connectors are treated in the schematic as a single, 440-pin connector, J4, with pin Rows A, B, C and D.

Figure 4-1: COM Express™ Connector Rows A-B (Pins 1-60) Schematic (Type 2 Pin-Out)

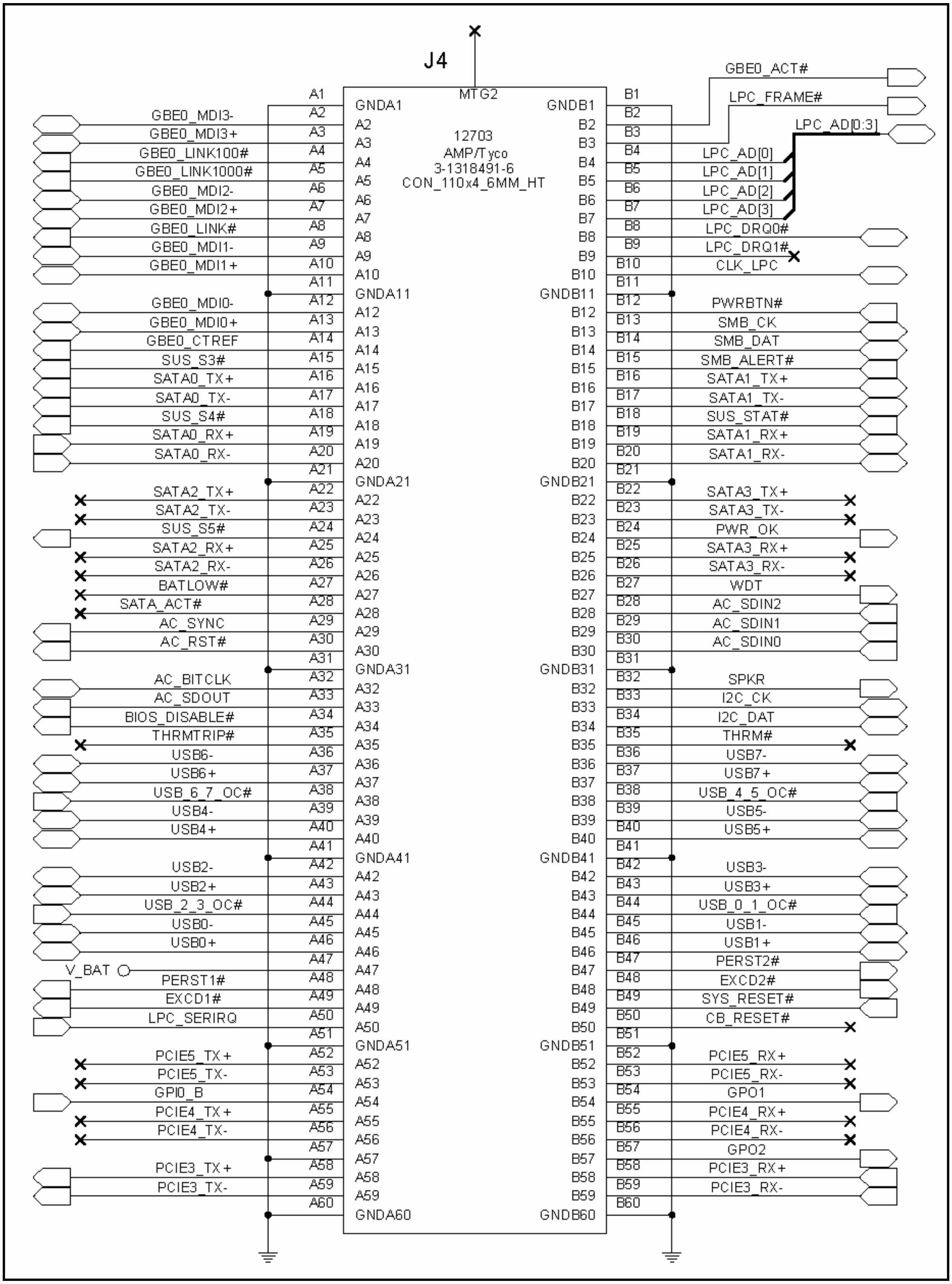


Figure 4-2: COM Express™ Connector Rows A-B (Pins 61-110) Schematic (Type 2 Pin-out)

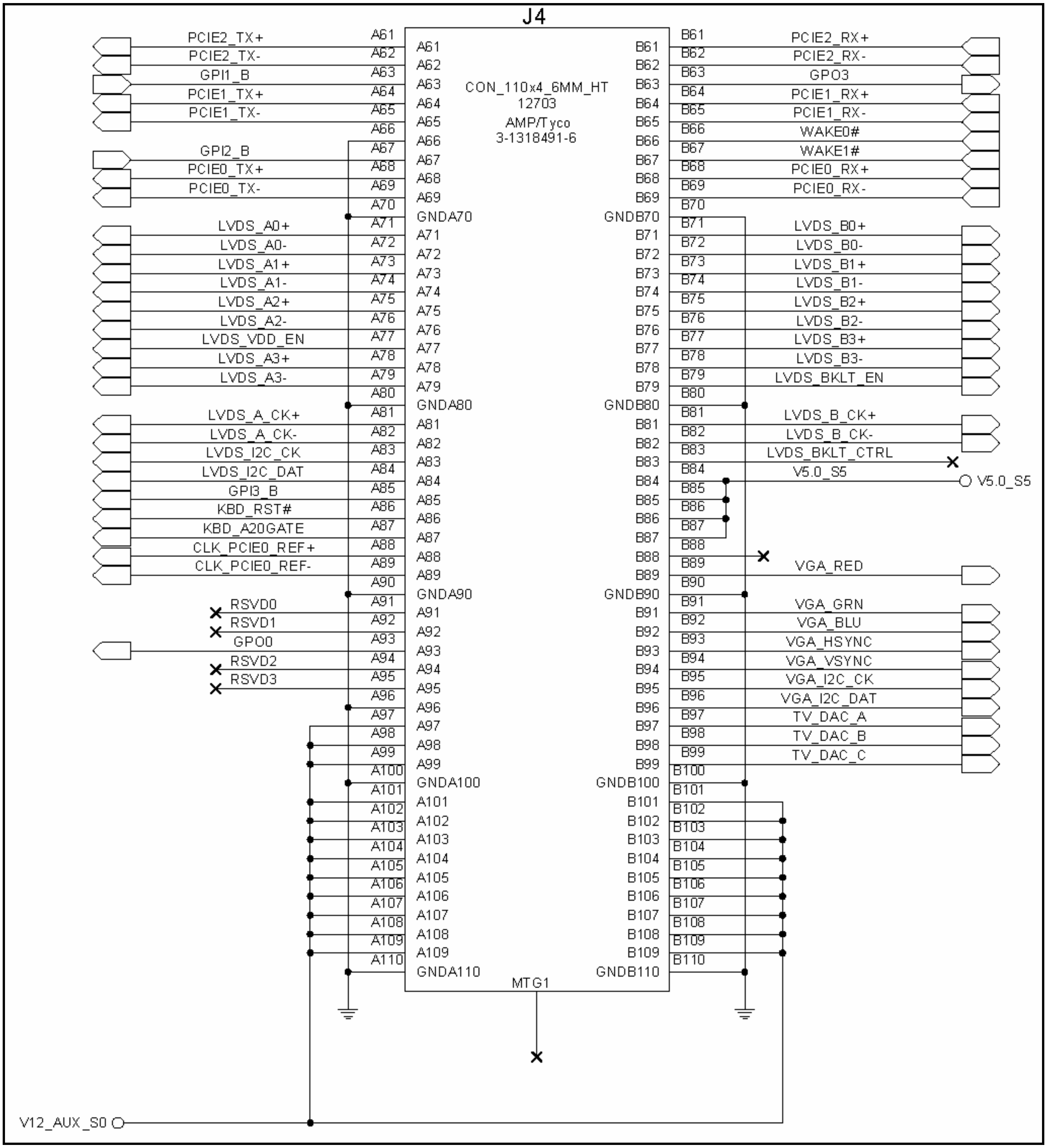
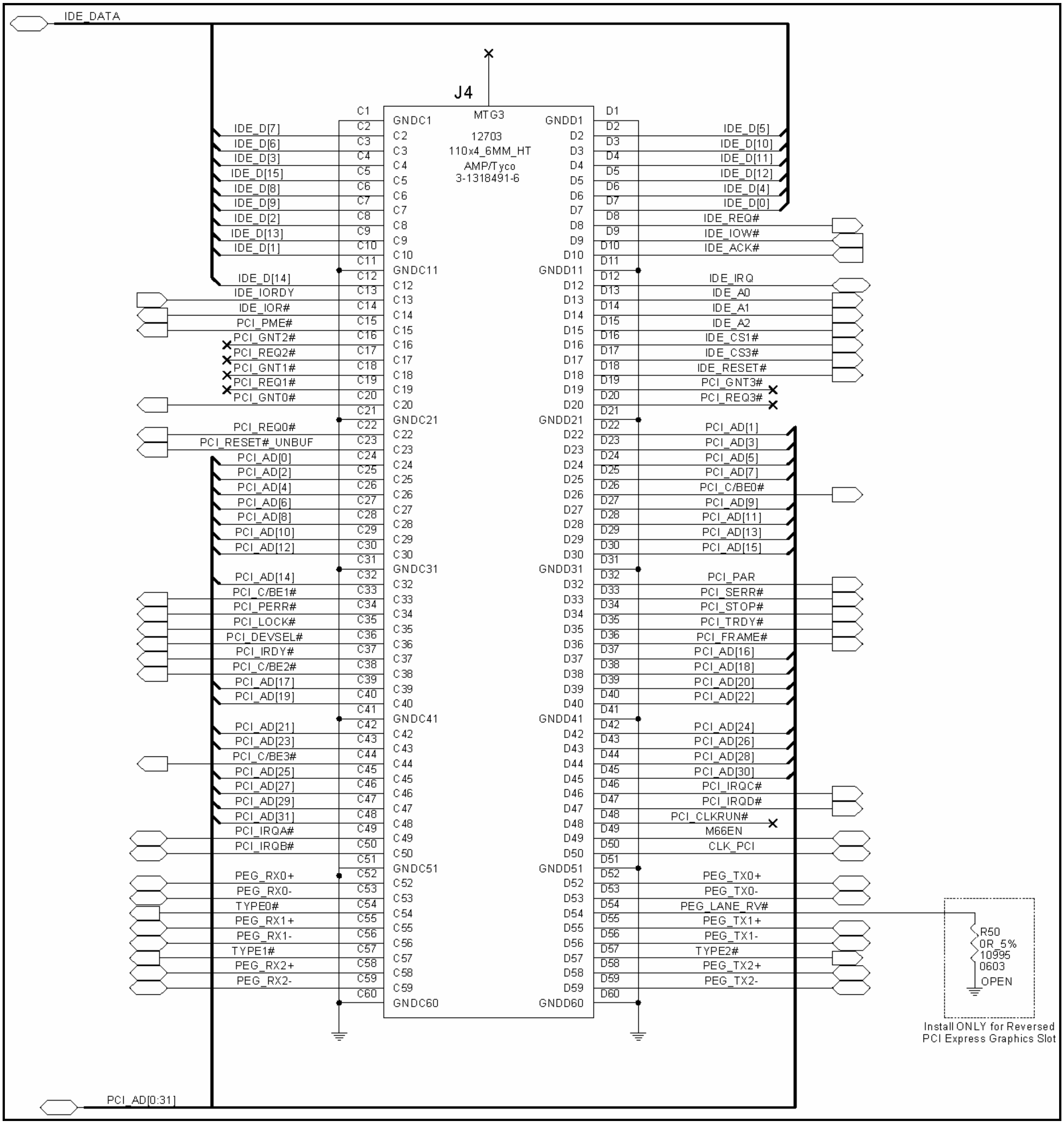
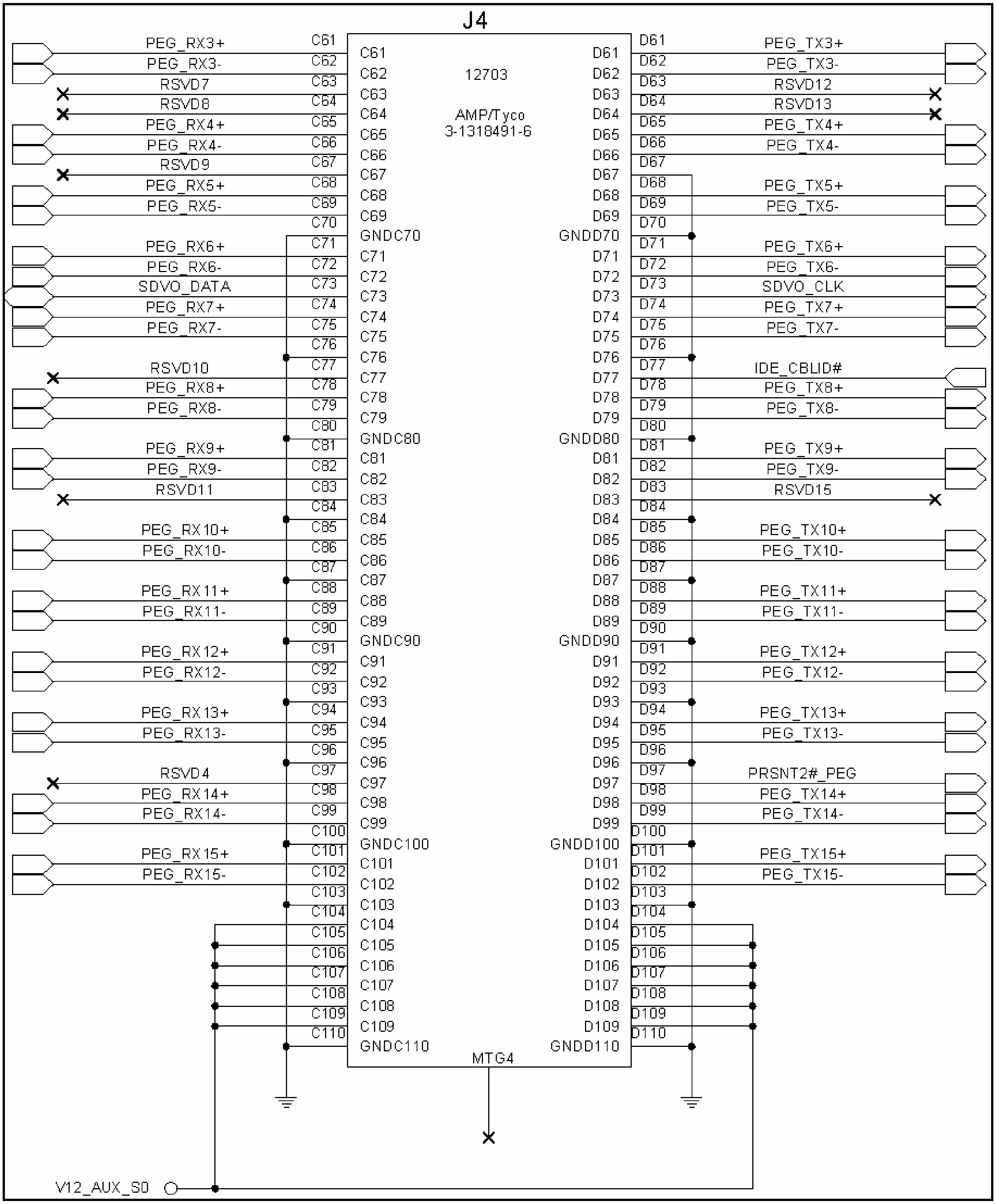


Figure 4-3: COM Express™ Connector Rows C-D (Pins 1-60) Schematic (Type 2 Pin-out)



The signal defined on Pin D54 PEG_LANE_RV# can reverse the mapping of the PCI Express Graphics (PEG) Lanes by strapping it to GND using a 0Ω resistor. See "*PEG Lane Reversal*" in Chapter 6 and Appendix C for additional details.

Figure 4-4: COM Express™ Connector Rows C-D (Pins 61-110) Schematic (Type 2 Pin-out)



5 PCIe Lanes 0-5

5.1 PCIe Lanes 0-5 – Signal Definitions

The COM Express™ Specification defines pins for six (0-5) PCI Express™ (PCIe™) lanes on the A-B Connector. Each ETXexpress Module must support a minimum of two lanes from this group. The manner in which lanes are grouped can vary with each Module. A lane "fill order" is described in the COM Express™ Specification.

Table 5-1: PCIe 0-5 Pin-outs

	PCIe 0-5			PCIe 0-5
A52	PCIE_TX5+		B52	PCIE_RX5+
A53	PCIE_TX5-		B53	PCIE_RX5-
A54			B54	
A55	PCIE_TX4+		B55	PCIE_RX4+
A56	PCIE_TX4-		B56	PCIE_RX4-
A57	GND		B57	
A58	PCIE_TX3+		B58	PCIE_RX3+
A59	PCIE_TX3-		B59	PCIE_RX3-
A60	GND (FIXED)		B60	GND (FIXED)
A61	PCIE_TX2+		B61	PCIE_RX2+
A62	PCIE_TX2-		B62	PCIE_RX2-
A63			B63	
A64	PCIE_TX1+		B64	PCIE_RX1+
A65	PCIE_TX1-		B65	PCIE_RX1-
A66	GND		B66	
A67			B67	
A68	PCIE_TX0+		B68	PCIE_RX0+
A69	PCIE_TX0-		B69	PCIE_RX0-
A70	GND (FIXED)		B70	GND (FIXED)
A71			B71	
A72			B72	
A73			B73	
A74			B74	
A75			B75	
A76			B76	
A77			B77	
A78			B78	
A79			B79	
A80	GND (FIXED)		B80	GND (FIXED)
A81			B81	
A82			B82	
A83			B83	
A84			B84	
A85			B85	
A86			B86	
A87			B87	
A88	PCIE0_CK_REF+		B88	
A89	PCIE0_CK_REF-		B89	
A90	GND (FIXED)		B90	GND (FIXED)

5.2 PCIe Lanes 0-5 – Routing Considerations

PCI Express (PCIe) signals are high-speed differential pairs with a nominal 100Ω differential impedance. Route them as differential pairs, preferably referenced to a continuous GND plane with a minimum of via transitions.

PCIe pairs need to be length-matched within a given pair (“intra-pair”), but the different pairs do not need to be matched (“inter-pair”).

PCB design rules for these signals are summarized in Appendix A.

The transmit pairs are designated as PCIE_TX0+ and PCIE_TX0- thru PCIE_TX5+ and PCIE_TX5-. Transmit in this context means that the signals are transmitted out of the Module.
No coupling capacitors are needed on Carrier Board PCIe transmit lines. The coupling caps are located on the Module.

The receive pairs are designated PCIE_RX0+ and PCIE_RX0- thru PCIE_RX5+ and PCIE_RX5-. Receive in this context means that the signals are received by the Module. Coupling capacitors are needed on the Carrier Board on these lines if the PCIe target device is “down” on the Carrier Board. Locate the coupling capacitors near the transmit pins of the Carrier Board’s PCIe target device. If the PCIe target device is on a slot card (device “up”), then no coupling caps are needed on the lines on the Carrier Board because the coupling caps will be on the slot card.

5.2.1 PCIe Polarity Inversion

Per the *PCI Express Card Electromechanical Specification*, all PCIe devices must support polarity inversion on each PCIe lane, independently of the other lanes. This means that, for example, you can route the Module PCIE_TX0+ signal to the corresponding ‘-’ pin on the slot or target device, and the PCIE_TX0- signal to the corresponding ‘+’ pin. If this makes the layout cleaner, with fewer layer transitions and better differential pairs, then take advantage of this PCIe feature.

5.2.2 PCIe Lane Reversal

Per the *PCI Express Card Electromechanical Specification*, all PCIe Cards optionally support lane reversal. Lane reversal means that, for example, it a x4 PCIe link, the ‘0’ pair can route to the target device ‘3’ pins; the ‘1’ pair to the target ‘2’ pins, the ‘2’ to the target ‘1’ pins, and the ‘3’ pair to the target ‘0’ pins. If this is done, it must be done with both the transmit and receive pairs.

The COM Express™ Specification does **not** require lane-reversal support and PCIe lane groups except for the PCI Express Graphics (PEG) group. This group is described in Section 6 below.

5.3 PCIe Lanes 0-5 – Reference Schematics

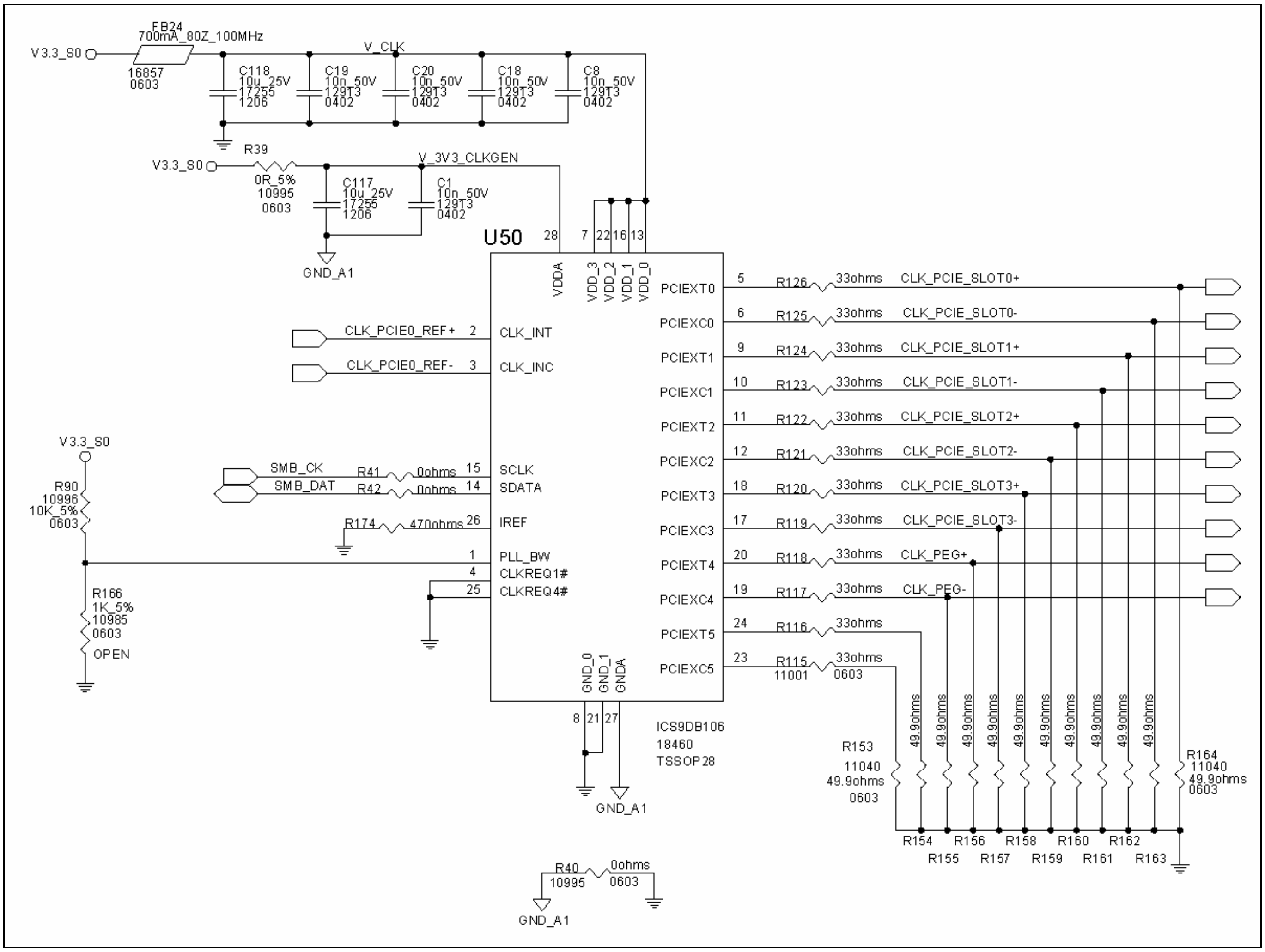
5.3.1 PCIe Reference Clock Buffer Example

The COM Express™ Specification calls for one copy of the PCIe reference clock pair to be brought out of the Module. This clock is a 100MHz differential pair and is sometimes known as a “hint” clock. The clock allows the PLL in the target PCIe device to lock faster onto the embedded clock in the PCIe bit stream.

If the Carrier Board implements only one PCIe device or slot, then the PCIe reference clock pair from the Module may be routed directly to that device or slot. However, if there are two or more PCIe devices or slots on the Carrier Board, then the Module PCIe reference clock should be buffered using a PLL based “zero-delay” buffer. Such devices are available from ICS (Integrated Circuits Systems), Cypress Semiconductor, and others.

The ICS9DB102, ICS9DB104 and ICS9DB106 have two, four and six differential output replicas of the input clock, respectively. The Cypress CY28401 provides eight copies of the differential input clock. Each target device (PCIe “device down” chip, slot, Express Card slot, PEG slot) should get an individual copy of the reference clock.

Figure 5-1: PCIe Reference Clock Buffer Schematic



The following notes apply to Figure 5-1 above.

- Nets CLK_PCIE0_REF+ and CLK_PCIE0_REF- are sourced from ETXexpress Module pins A88 and A89 respectively.
- Each clock pair is routed point to point to each connector or end device using differential signal routing rules.
- Each clock output pair from the ICS buffer are terminated close to the ICS buffer pins with a series resistor (shown as 33Ω) and a termination to GND (shown as 49.9Ω).
- SM Bus nets SMB_CK and SMB_DAT are sourced from ETXexpress Module pins B13 and B14 respectively.
    - SM Bus software can control the PLL bandwidth or bypass the PLL for board tests.
    - SM Bus software can enable or disable clock-buffer outputs. Disable unused outputs to reduce emissions.

- ICS chip pins CLKREQ1# and CLKREQ4# are pulled low to enable ICS outputs PCIEXT1, PCIEXC1 and PCIEXT4, PCIEXC4 ('T' and 'C' stand for 'true' and 'complement' in the ICS names) in hardware, rather than by software.

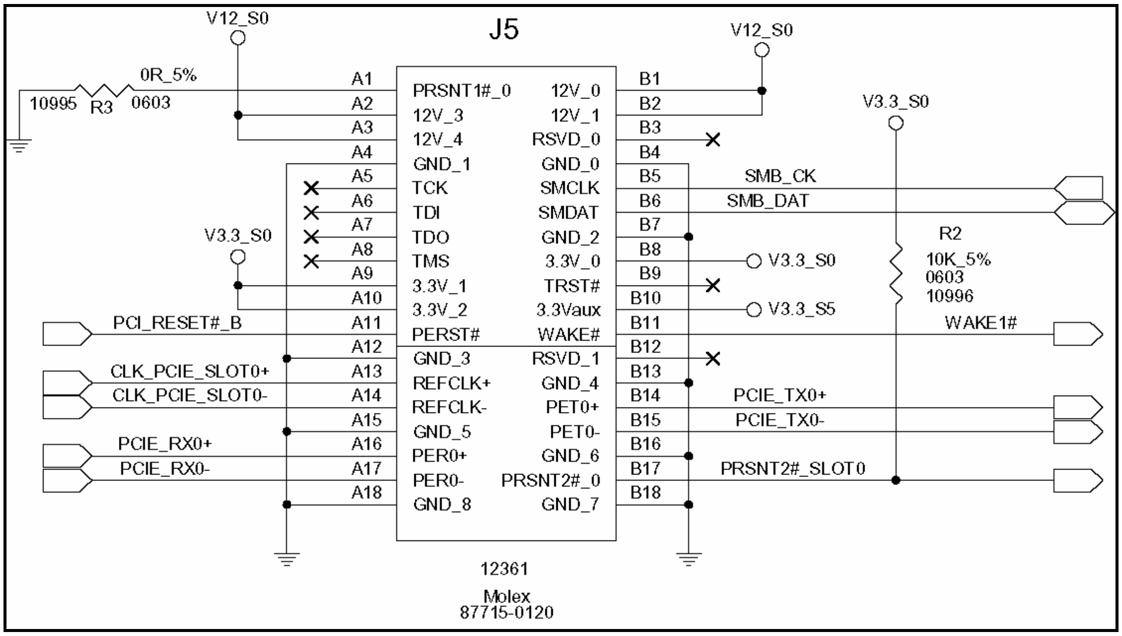
- The ICS chip IREF pin (pin 26) is pulled low thru the 475Ω fixed precision resistor to establish the reference current for differential current-mode output pairs.

- The ICS chip PLL_BW pin (pin 1) is pulled high to enable a high PLL bandwidth option.

5.3.2 PCIe x1 Slot Example

An example of an x1 PCIe slot is shown in Figure 5-2 below. A PCIe x1 slot is commonly used for GBE slot cards. The source specification for slot implementations is the PCI-SIG "*PCI Express Card Electromechanical Specification*™." See Appendix G for a reference to this specification.

Figure 5-2: PCIe x1 Slot Schematic



- The slot PRSNT1#_0 and PRSNT2#_0 are part of a mechanism that allows hot-plugged PCIe cards. However, most systems do not implement the support circuits needed to complete hot-plug capability. Please refer to the *PCI Express Card Electromechanical Specification* (source specification reference in Appendix G) for details.

- In practice, desktop systems do not seem to make use of the PRSNT2#_0 mechanism. The system can detect the presence of a PCIe device over the PCIe link directly.

- In Figure 5-2 above, PRSNT1#_0 (pin A1) is pulled low on the Carrier Board thru R35.

- On the slot card, PRSNT1#_0 (pin A1) is routed to PRSNT2#_0 (pin B17). The state of slot pin B17 may be read back by the BIOS or system software. If a slot card is present, this pin reads back low; if the slot is empty, the pin will be read high. In the Kontron Brownsville reference design, PRSNT2#_SLOT0 is routed to a GPI pin on the Super I/O device Winbond W83627HFJ (Figure 16-2, U1 pin 126) as a way to allow the slot PRSNT2#_0 state to be read. If the Carrier Board does not include the Winbond Super I/O, use an alternative input pin. The BIOS or system software adjustment may be necessary.

- The slot reset pin, PERST# (pin A11), is driven by net PCI_RESET#. This net is a buffered copy of the ETXexpress Module PCI reset line (Module pin C23; net name PCI_RESET_UNBUF# in Figure 4-3.). If there is only a single PCI and PCIe device on the Carrier Board, then it is not necessary to buffer the Module PCI_RESET_UNBUF# signal.

- The slot reset pin may alternatively be driven by Module pin B50 (net CB_RESET# in Figure 4-1). This is a must for Type 1 modules.

- Slot signals REFCLK+ and REFCLK- (pins A13 and A14) are driven by the Clock Buffer, which is shown in Figure 5.1. Plug-in cards can optionally use this clock source.

- Nets PCIE_TX0+ and PCIE_TX0- are sourced from ETXexpress Module pins A68 and A69 respectively. These nets drive the RX load on the slot card. These nets are AC-coupled on the module. No coupling capacitors are needed on the Carrier Board.

- Nets PCIE0_RX+ and PCIE0_RX- drive ETXexpress Module pins B68 and B69 respectively. These nets are driven by the TX source on the slot card. No coupling capacitors are needed on the Carrier Board.

- Nets SMB_CK and SMB_DAT are sourced from ETXexpress Module pins B13 and B14 respectively.

    - The SM Bus supports plug-in, card-management functions and provides Manufacturer information, a model number, and a part number.

    - SM Bus software can save the state of the slot-car device before a suspend event, report errors, accept control parameters, and return status.

    - Support for the SM Bus is optional on the slot card.

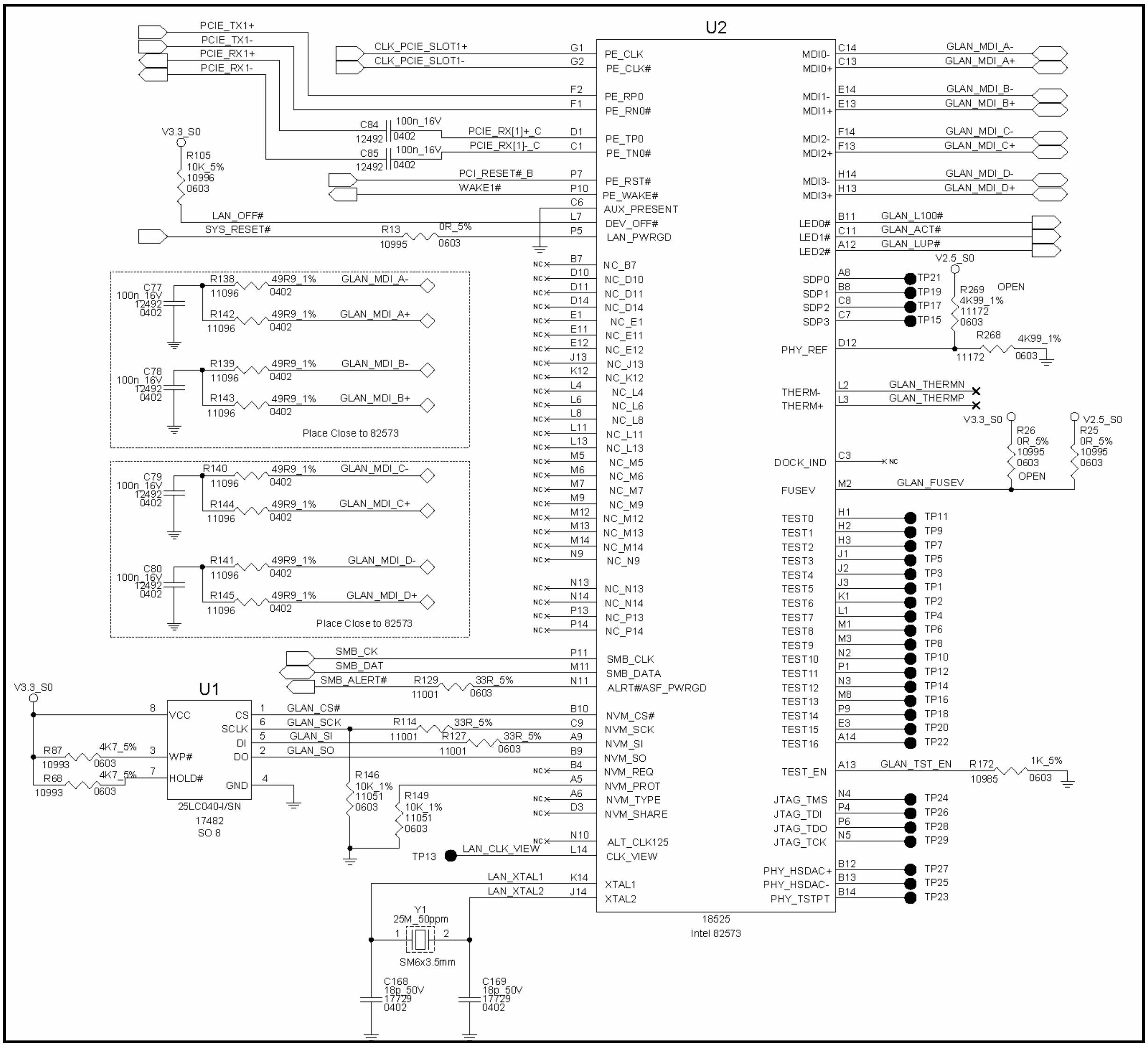
- WAKE1# is asserted by the slot card to cause ETXexpress Module wake-up at Module pin B67. This is an open-drain signal. It is an input to the Module and is pulled up on the Module. Other WAKE1# sources may pull this line low; it is a shared line.

- Slot JTAG pins on A5-A8 are not used.

5.3.3 PCIe x1 Device-Down Example: GBE Controller

Figures 5-3, 5-4 and 5-5 below show a “device-down” example. In the example, an Intel 82573 PCI Express-based Gigabit Ethernet (GBE) controller is used. This device is an integrated MAC / PHY and interfaces to the host system thru x1 PCIe link. Please note that this example has nothing to do with the ETXexpress Module LAN Ports 0, 1, 2.

Figure 5-3: PCIe Device Down GBE Schematic (1 of 3)



The following notes apply to Figure 5.3 above, PCIe Device-Down GBE Schematic 1 of 3.

- U2 pins G1 and G2 (PE_CLK and PE_CLK#) are sourced from the Clock Buffer as described earlier in this chapter.
- Nets PCIE1_TX+ and PCIE1_TX- are sourced from ETXexpress Module pins A64 and A65 respectively.
    - The x1 PCIe Lane Transmit interface on the ETXexpress Module drives the RX load on the GBE chip.

- PCIE1_RX+ and PCIE1_RX- are sourced from ETXexpress Module pins B64 and B65 respectively.
    - The x1 PCIe Lane Receive interface on the ETXexpress Module is driven by the TX source on the GBE chip.
        - The TX source needs to be AC-coupled near the source.
- PE_RST# is driven by PCI_RESET#_B from the ETXexpress Module pin C23 PCI_RESET# after buffering.
    - This resets the GBE chip for initialization.
- PE_WAKE# is asserted by the GBE chip and causes the ETXExpress Module to wake-up at ETXExpress Module pin B67 WAKE1#.
    - The GBE chip asserts PE_WAKE# when it receives a wake-up packet and is configured for Wake Up.
    - WAKE1# is pulled up on the module to facilitate the “wire-ORed” interconnect from other WAKE1# sources.
- AUX_PRESENT is tied low to indicate no Auxiliary Power.
- DEV_OFF# is tied high to always enable the chip. The Device Off signal can asynchronously disable the chip.
- LAN_PWRGD acts as a master reset for the GBE chip when it is pulled low. The signal is driven by System Reset.
- SMB_CK and SMB_DAT are sourced from ETXexpress Module pins B13 and B14 respectively.
    - The SM Bus supports GBE management functions and provides Manufacturer information, a model number, and a part number.
    - Save its state to suspend event, report errors, accept control parameters, and return status.
- SMB_ALERT# is sourced from the GBE chip (ALRT#/ASF_PWRGD) to drive ETXexpress Module pin B15.
    - This generates a System Management Interrupt SMI# and acts as a PCI Power Good input signal in ASF mode.
- NVM_xx signals interface with non-volatile memory U1, Serial Prom 25LC040.
- ALT_CLK125 is an alternate 125MHz clock and should not be connected.
- LAN_CLK_VIEW is brought out to a test point for test purposes.
- XTAL1 input is connected to the 25MHz parallel resonant crystal.
- XTAL2 internal oscillator output is connected to the crystal to create oscillation.
- MDI0+/- thru MDI3+/- connect to GBE magnetics, which are typically integrated in an RJ45 LAN connector.

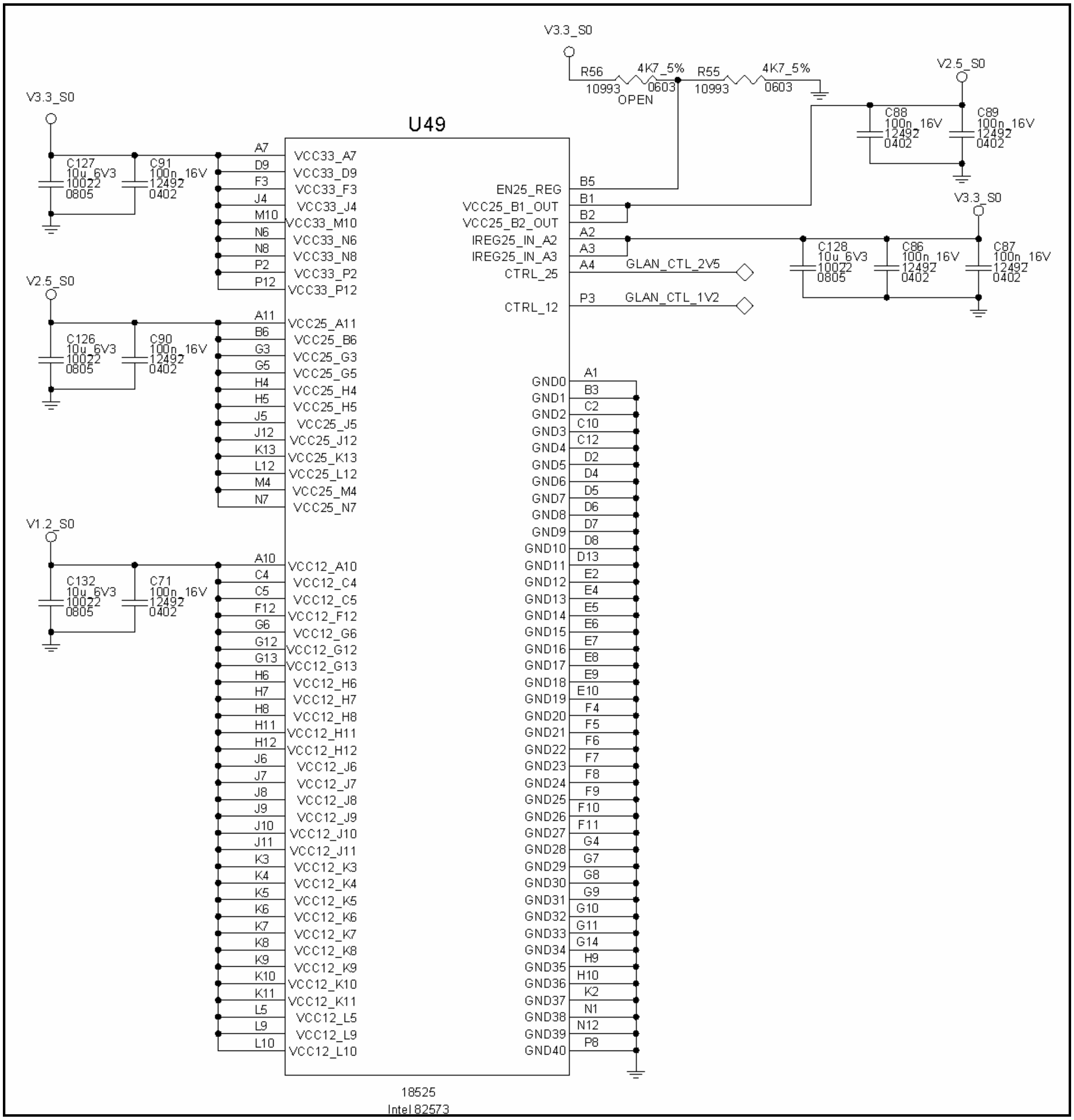
- Figure 5-3 above shows a termination that is close to the source to dampen and minimizes crosstalk.

- LED0# is interconnected to the LAN connector RJ45, LED 2. The dual-color (Orange and Green) LED indicates a 100 megabits per second LAN bit rate, using Orange illumination.
- LED1# is interconnected to the LAN connector RJ45, LED 1. The single-color (Yellow) LED indicates LAN activity, using Yellow illumination.
- LED2# is interconnected to the LAN connector RJ45, LED 2. The dual-color (Orange and Green) LED indicates a 1000 megabits per second LAN bit rate, using Green illumination.
- PHY_REF provides PHY analog reference input and should be pulled low thru the 4.9KΩ resistor.
- FUSEV should be connected to 2.5V.
- TEST_EN should be pulled down thru the 1KΩ resistor.

The following details apply to Figure 5.4 below, PCIe Device Down GBE Schematic 2 of 3.

- EN25_REG is pulled low thru the 4.7KΩ resistor to enable the external 2.5V regulator.
- CTRL_25 is activated by EN25_REG being low to control the external 2.5V regulator.
- CTRL_12 controls the external 1.2V regulator.

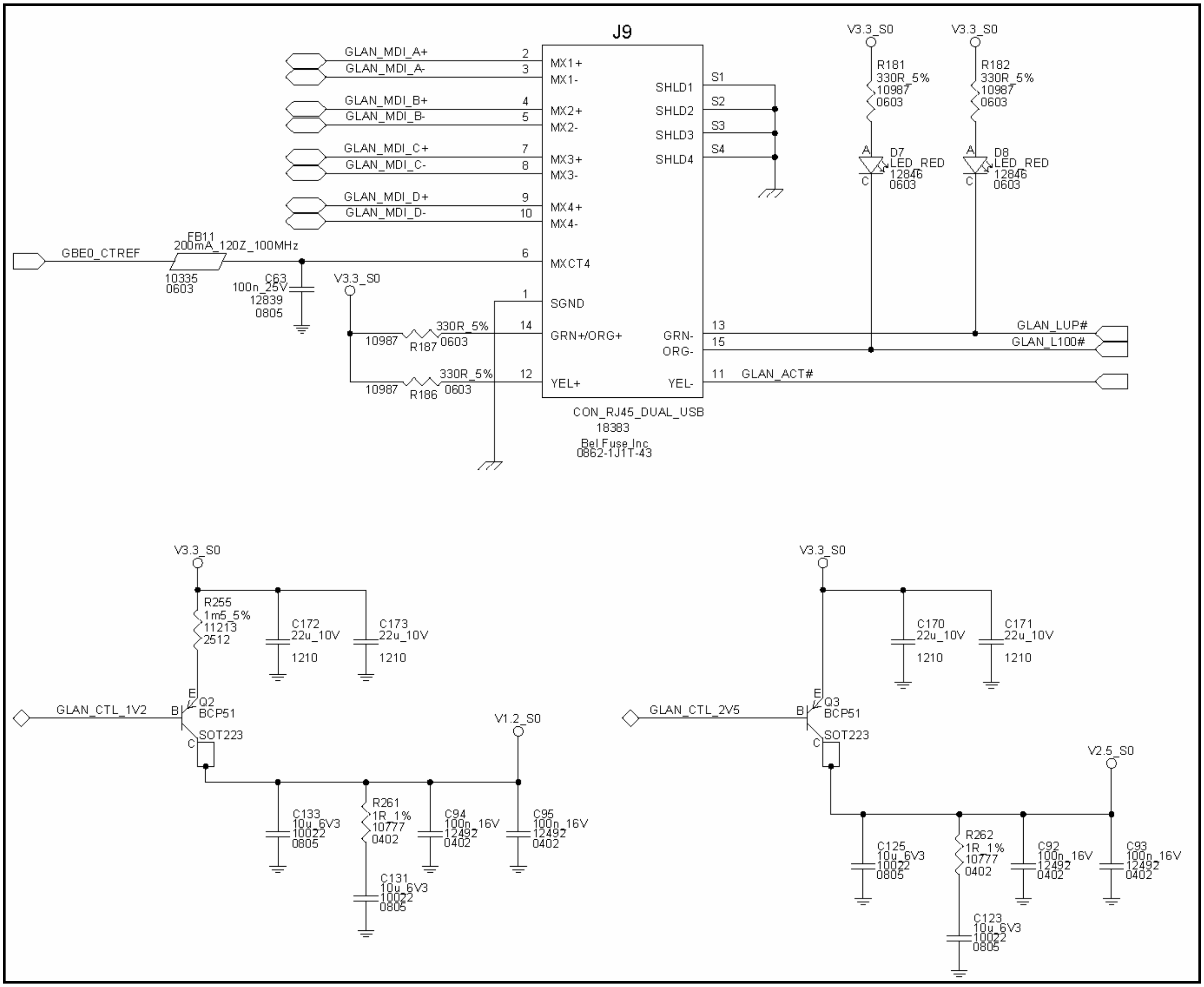
Figure 5-4: PCIe Device Down GBE Schematic (2 of 3)



The following notes apply to Figure 5.5 below, PCIe Device Down GBE Schematic 3 of 3.

- J6 is a combo connector that incorporates a 1 x RJ45 with GBE magnetics, dual LEDs, and 2 x USB Type A connectors. The USB portion of the connector is not shown.
- MX1+/- thru MX4+/- interconnect to the GBE controller.
- MXCT4 is connected to 2.5V.
- GRN+/ORG+ are connected to 3.3V thru a 330Ω current-limiting resistor to drive the Green or Orange LED.
- YEL+ is connected to 3.3V thru a 330Ω current-limiting resistor to drive the Yellow LED.
- GRN- is driven by a signal from the GBE controller to indicate a 1000 megabits per second LAN bit rate, which illuminates the Green LED.
- ORG- is driven by a signal from the GBE controller to indicate a 100 megabits per second LAN bit rate, which illuminates the Orange LED.
- YEL- is driven by a signal from the GBE controller to indicate LAN Activity, which illuminates the Yellow LED.
- Discrete circuitry at transistor Q2 shows GLAN_CTL_1V2 from the GBE controller. This turns on the transistor to output V1.2_S0 for input to the GBE controller.
- Discrete circuitry at transistor Q1 shows GLAN_CTL_2V5 from the GBE controller. This turns on the transistor to output V2.5_S0 for input to the GBE controller.

Figure 5-5: PCIe Device Down GBE Schematic (3 of 3)



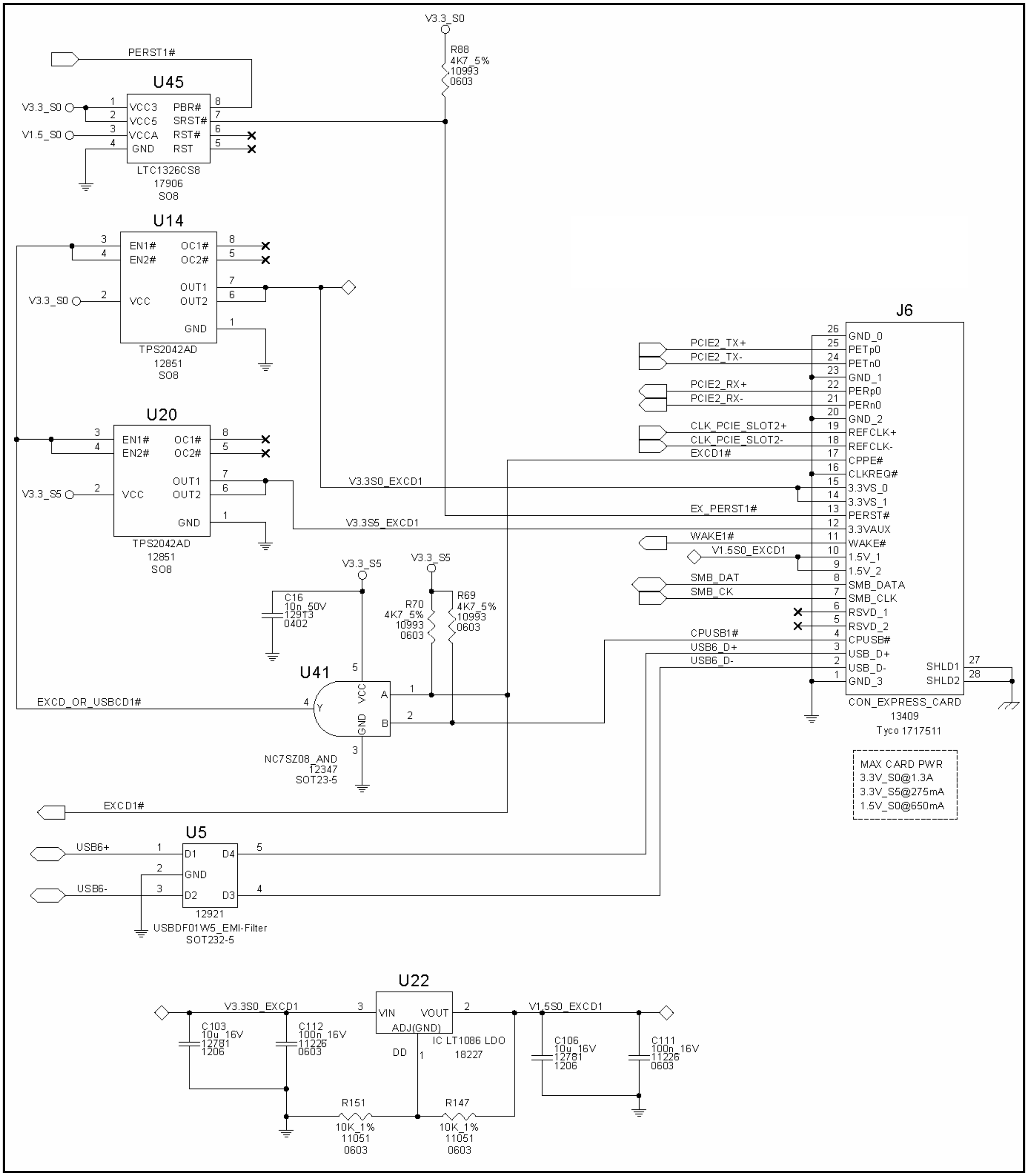
5.3.4 Express Card Examples

Hot-swappable Express Cards come in a small form factor and are designed primarily for mobile computing. The card's electrical interface is thru USB 2.0 or a single x1 PCIe link. Express Cards are the successor to Card Bus Cards (which are PCI-based). Card Bus cards, in turn, are the successors to PCMCIA cards. All three formats are defined by the PCMCIA Consortium.
An Express Card specification reference can be found in Appendix G.

The PCMCIA Consortium defines two form factors for Express Cards:

- Express Card/34 and Express Card/54 use a socket-style interconnect.
  - There are two mechanical Form Factors with Express Card/34, which are useable in either socket. Each has the same electrical interface.
  - Interface support for a PCIe x1 lane and USB 2.0 on the socket is required.
- Socket interface requirements for Carrier Boards include:
  - PCIe x1 Lane and USB 2.0
  - WAKE# and the SM Bus are optional at the socket and ETXexpress Module level.

Figure 5-6: PCIe Express Card 0 Schematic



The following notes apply to Figure 5-6 above, for the PCIe Card 0 example. A similar set of considerations applies to Figure 5-7 below, for Express Card 1. The net name references given here apply to Figure 5-6.

- Nets PCIE_TX2+ and PCIE_TX2- are sourced from ETXexpress Module pins A61 and A62 respectively. These lines drive PETp0 and PETn0 on the card socket for the PCIe receivers on the Express Card. No coupling capacitors are required on the Carrier Board. These lines are capacitively coupled on the ETXexpress Module.

- Nets PCIE_RX2+ and PCIE_RX2- drive ETXexpress Module pins B61 and B62 respectively. The x1 PCIe Lane Receive interface on the ETXexpress Module is driven by PERp0 and by PERn0 on the card socket from the PCIe transmit source on the Express Card. No coupling capacitors are required on the Carrier Board. These lines are capacitively coupled on the Express Card.

- REFCLK+ and REFCLK- are a 100MHz reference clock for PCIe use. They are sourced from the PCIe Reference Clock Buffer (described earlier in Section 5.3), or are sourced directly from the ETXexpress Module (if there is only a single destination for them). This reference clock pair is not needed for Express Cards that do not support PCIe and can be left unconnected.

- CPPE# is pulled low on the Express Card to indicate that a card is present and has a PCIe interface.

- CPUSB# is pulled low on the Express Card to indicate the presences of an Express Card and a USB 2.0 interface.

  - Either CPPE# or CPUSB# low causes net EXCD_0RUSBCD1# to go low, which enables the TPS2042AD Power FETs to provide power to the Express Card.

- CLKREQ# is used for dynamic-clock management.

  - When the signal is pulled low, the dynamic-clock management feature is not supported.

- PERST# is driven from the Linear Technology power-supply monitor chip that asserts EXCD0_RST# after a 200ms delay from EXCD0_PERST#, which comes from ETXexpress Module pin A48.

  - This indicates stable power to the Express Card and also serves as hardware reset.

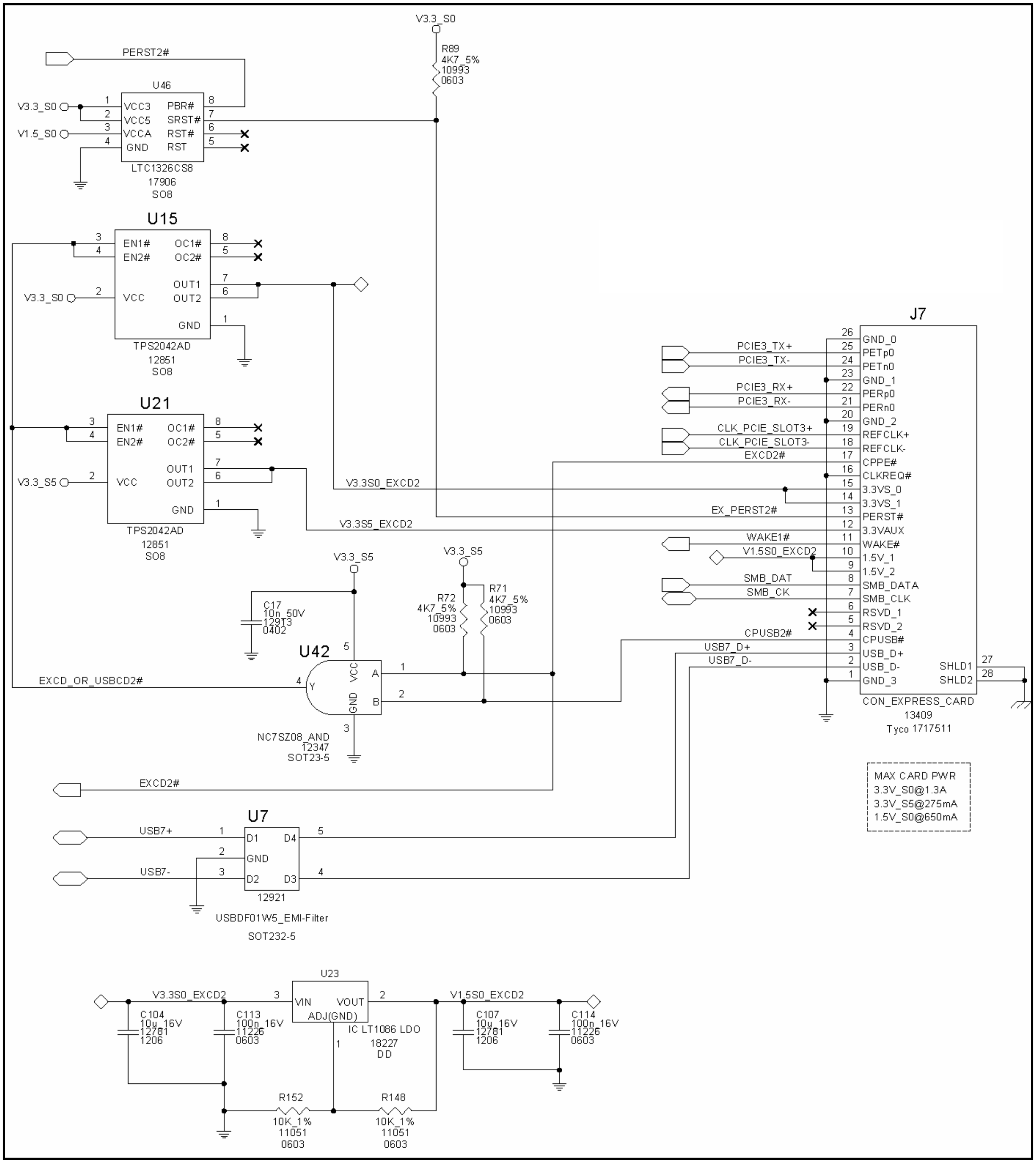
- WAKE# is asserted by the Express Card to cause the ETXexpress Module to wake-up at ETXexpress Module pin B67 WAKE1#.WA KE1# is pulled up on the module to facilitate the “wire-ORed” interconnect from other WAKE1# sources.

- SMB_CK and SMB_DAT are sourced from ETXexpress Module pins B13 and B14 respectively.

  - The SM Bus supports client-alerting, wireless RF management, and sideband management.
  - Support for the SM Bus is optional on the Carrier Board and the Express Card.

- USB6+ and USB6- are sourced from ETXexpress Module pins A37 and A36 respectively.

Figure 5-7: PCIe Express Card 1 Schematic



6 PEG, SDVO, and PCIe Lanes 16-31

6.1 PEG, SDVO and PCIe Lanes 16-31 – Signal Definitions

A common set of pins on the COM Express C-D Connector Rows is shared with PCI Express Graphics (PEG), SDVO channels B and C, or general-purpose PCIe Lanes 16-31. This pin-out and pin-sharing arrangement is shown in Table 6-1 below.

All signals are high-speed differential pairs with 100Ω differential impedance and 55Ω single- ended impedance except for the SDVO I^2C lines – SDVO_DATA and SDVO_CLK, all of which are low-speed, single-ended signals. Appendix A summarizes routing rules for differential pairs.

Table 6-1: PEG x16, SDVO B and C, and PCIe 16-31 Pin-outs

	PEG x16	SDVO	PCIe 16-31			PEG X16	SDVO	PCIe 16-31
C51	GND (FIXED)				D51	GND (FIXED)		
C52	PEG_RX0+	SDVO_TVCLKIN+	PCIE_RX16+		D52	PEG_TX0+	SDVOB_RED+	PCIE_TX16+
C53	PEG_RX0-	SDVO_TVCLKIN -	PCIE_RX16-		D53	PEG_TX0-	SDVOB_RED-	PCIE_TX16-
C54					D54	PEG_LANE_RV#		
C55	PEG_RX1+	SDVOB_INT+	PCIE_RX17+		D55	PEG_TX1+	SDVOB_GRN+	PCIE_TX17+
C56	PEG_RX1-	SDVOB_INT-	PCIE_RX17-		D56	PEG_TX1-	SDVOB_GRN-	PCIE_TX17-
C57					D57			
C58	PEG_RX2+	SDVO_FLDSTALL+	PCIE_RX18+		D58	PEG_TX2+	SDVOB_BLU+	PCIE_TX18+
C59	PEG_RX2-	SDVO_FLDSTALL -	PCIE_RX18-		D59	PEG_TX2-	SDVOB_BLU-	PCIE_TX18-
C60	GND (FIXED)				D60	GND (FIXED)		
C61	PEG_RX3+		PCIE_RX19+		D61	PEG_TX3+	SDVOB_CK+	PCIE_TX19+
C62	PEG_RX3-		PCIE_RX19-		D62	PEG_TX3-	SDVOB_CK-	PCIE_TX19-
C63					D63			
C64					D64			
C65	PEG_RX4+		PCIE_RX20+		D65	PEG_TX4+	SDVOC_RED+	PCIE_TX20+
C66	PEG_RX4-		PCIE_RX20-		D66	PEG_TX4-	SDVOC_RED-	PCIE_TX20-
C67					D67	GND		GND
C68	PEG_RX5+	SDVOC_INT+	PCIE_RX21+		D68	PEG_TX5+	SDVOC_GRN+	PCIE_TX21+
C69	PEG_RX5-	SDVOC_INT-	PCIE_RX21-		D69	PEG_TX5-	SDVOC_GRN-	PCIE_TX21-
C70	GND (FIXED)				D70	GND (FIXED)		
C71	PEG_RX6+		PCIE_RX22+		D71	PEG_TX6+	SDVOC_BLU+	PCIE_TX22+
C72	PEG_RX6-		PCIE_RX22-		D72	PEG_TX6-	SDVOC_BLU-	PCIE_TX22-
C73		SDVO_DATA			D73		SDVO_CLK	
C74	PEG_RX7+		PCIE_RX23+		D74	PEG_TX7+	SDVOC_CK+	PCIE_TX23+
C75	PEG_RX7-		PCIE_RX23-		D75	PEG_TX7-	SDVOC_CK-	PCIE_TX23-
C76	GND				D76	GND		
C77	RSVD				D77			
C78	PEG_RX8+		PCIE_RX24+		D78	PEG_TX8+		PCIE_TX24+
C79	PEG_RX8-		PCIE_RX24-		D79	PEG_TX8-		PCIE_TX24-
C80	GND (FIXED)				D80	GND (FIXED)		
C81	PEG_RX9+		PCIE_RX25+		D81	PEG_TX9+		PCIE_TX25+
C82	PEG_RX9-		PCIE_RX25-		D82	PEG_TX9-		PCIE_TX25-
C83	RSVD				D83			
C84	GND				D84	GND		
C85	PEG_RX10+		PCIE_RX26+		D85	PEG_TX10+		PCIE_TX26+
C86	PEG_RX10-		PCIE_RX26-		D86	PEG_TX10-		PCIE_TX26-
C87	GND				D87	GND		
C88	PEG_RX11+		PCIE_RX27+		D88	PEG_TX11+		PCIE_TX27+
C89	PEG_RX11-		PCIE_RX27-		D89	PEG_TX11-		PCIE_TX27-
C90	GND (FIXED)				D90	GND (FIXED)		
C91	PEG_RX12+		PCIE_RX28+		D91	PEG_TX12+		PCIE_TX28+
C92	PEG_RX12-		PCIE_RX28-		D92	PEG_TX12-		PCIE_TX28-
C93	GND				D93	GND		
C94	PEG_RX13+		PCIE_RX29+		D94	PEG_TX13+		PCIE_TX29+
C95	PEG_RX13-		PCIE_RX29-		D95	PEG_TX13-		PCIE_TX29-
C96	GND				D96	GND		
C97	RSVD				D97	PEG_ENABLE#		
C98	PEG_RX14+		PCIE_RX30+		D98	PEG_TX14+		PCIE_TX30+
C99	PEG_RX14-		PCIE_RX30-		D99	PEG_TX14-		PCIE_TX30-
C100	GND (FIXED)				D100	GND (FIXED)		
C101	PEG_RX15+		PCIE_RX31+		D101	PEG_TX15+		PCIE_TX31+
C102	PEG_RX15-		PCIE_RX31-		D102	PEG_TX15-		PCIE_TX31-

6.2 PEG, SDVO, and PCIe Lanes 16-31 – Routing Considerations

6.2.1 PCIe Polarity Inversion

Per the *PCI Express Card Electromechanical Specification*, all PCIe devices must support polarity inversion on each PCIe lane, independently of the other lanes. For example, you can route the ETXexpress Module PCIE_TX0+ signal to the corresponding '-' pin on the slot or target device, and the PCIE_TX0- signal to the corresponding '+' pin. If this makes the layout cleaner, with fewer layer transitions and better differential pairs, then take advantage of this PCIe feature.

6.2.2 PEG Lane Reversal

The COM Express™ Specification defines an input signal, PEG_LANE_RV#, on Module connector pin D54 to enable PEG lane reversal. Strapping PEG_LANE_RV# low on the Carrier Board causes the ETXexpress Module chipset to reverse the PEG lane order (PEG lane 0 on the chipset becomes PEG lane 15; PEG lane 1 becomes PEG lane 14; etc.)

This can be extremely useful. If you find that the PEG bus is crossed, or has a "bowtie," when placing parts on the Carrier Board, you can eliminate the bowtie by invoking PEG-lane reversal.

However, there are caveats:

- Lane reversal applies only to PEG lines. SDVO lines do not follow suit. If PEG lane reversal is invoked to eliminate a "bowtie" for a PEG x16 slot connector layout, and the use of both PEG and SDVO is desired, a "reverse pin-out" ADD2 card, designated as ADD2-R, will be needed for the SDVO application. A normal pin-out graphics card is still used. (There are no reverse pin-out graphics cards).
- Lane reversal may not apply if the lines are used for general purpose PCIe use, rather than x16 PEG use. Check the relevant ETXexpress Module User Guide.

6.2.3 PEG_ENABLE# – External Graphics Enable

The COM Express™ Specification defines an input signal on Module connector pin D97, PEG_ENABLE#, to select external graphics functions. This pin should be strapped to low on the ETXexpress Carrier Board to enable the x16 PEG interface and to disable the internal graphics function on the ETXexpress Module.

For graphics-slot implementations, this line is routed to the slot and the graphics card pulls the line low. If the slot is not populated, the Module PEG_ENABLE# floats and the Module uses internal graphics (if present on the Module). For "device-down" graphics applications, the PEG_ENABLE# line should be pulled down thru a resistor.

6.2.4 SDVO Option – Module Types 2, 3, 4, 5

A subset of the x16 PEG signals on the Module connector may be used for two SDVO channels, designated B and C, instead of PEG. This feature depends upon the design of the Module. These signals can interface to an SDVO device on the Carrier Board or to a slot for an ADD2 plug-in card.

Figure 6-1 below shows the interconnect between the Module connector and the Graphics slot that may be used with a normal pin-out ADD2 slot card. Normal pin-out ADD2 cards are designated as ADD2-N.

See SDVO details in Appendix A for Trace Routing Parameters and Guidelines.

6.2.5 SDVO Option – PEG Lane Reversal

If Module pin D54 PEG_LANE_RV# is strapped low to untwist a bowtie on the PEGx16 lines to an x16 slot, then an ADD2 card used in this slot must be a reverse pin-out ADD2 card.
Reverse pin-out ADD2 cards are designated ADD2-R.

If the SDVO device is "down" on the Carrier Board, then the PEG_LANE_REV# pin has no effect because SDVO lines are not reversed on the chipset – only PCIe x16 lines are.

6.2.6 SDVO_DATA & SDVO_CLK Termination

These signals require 3.5KΩ pull-up resistors to 2.5V for device-down applications. The pull-ups are not required on the ETXexpress Carrier Board for an ADD2 slot card application because the pull-ups are on the ADD2 card.

If these lines are pulled high, the system software assumes that the PEG interface will be used for SDVO rather than PEG.

6.2.7 General Purpose PCIe Lanes 16-31

Per the COM Express™ Specification, PEG lines may alternatively be used for general-purpose PCIe lanes. In this case, the lanes are referred to as PCIe lanes 16-31. This capability depends upon the Module design. On most chipsets that have a x16 PCIe interface for graphics, the lines are only available for general-purpose PCIe use if used in an x1 (instead of a x16) configuration. Chipsets that can make PCIe lanes 16-31 available for general purpose are likely to be server-class chipsets.

The reversal feature of the PEG lane described earlier in 6.2.2 does not apply in this case.

See Appendix A for Trace Routing Parameters and Guidelines.

6.3 PEG, SDVO, and PCIe Lanes 16-31 – Reference Schematics

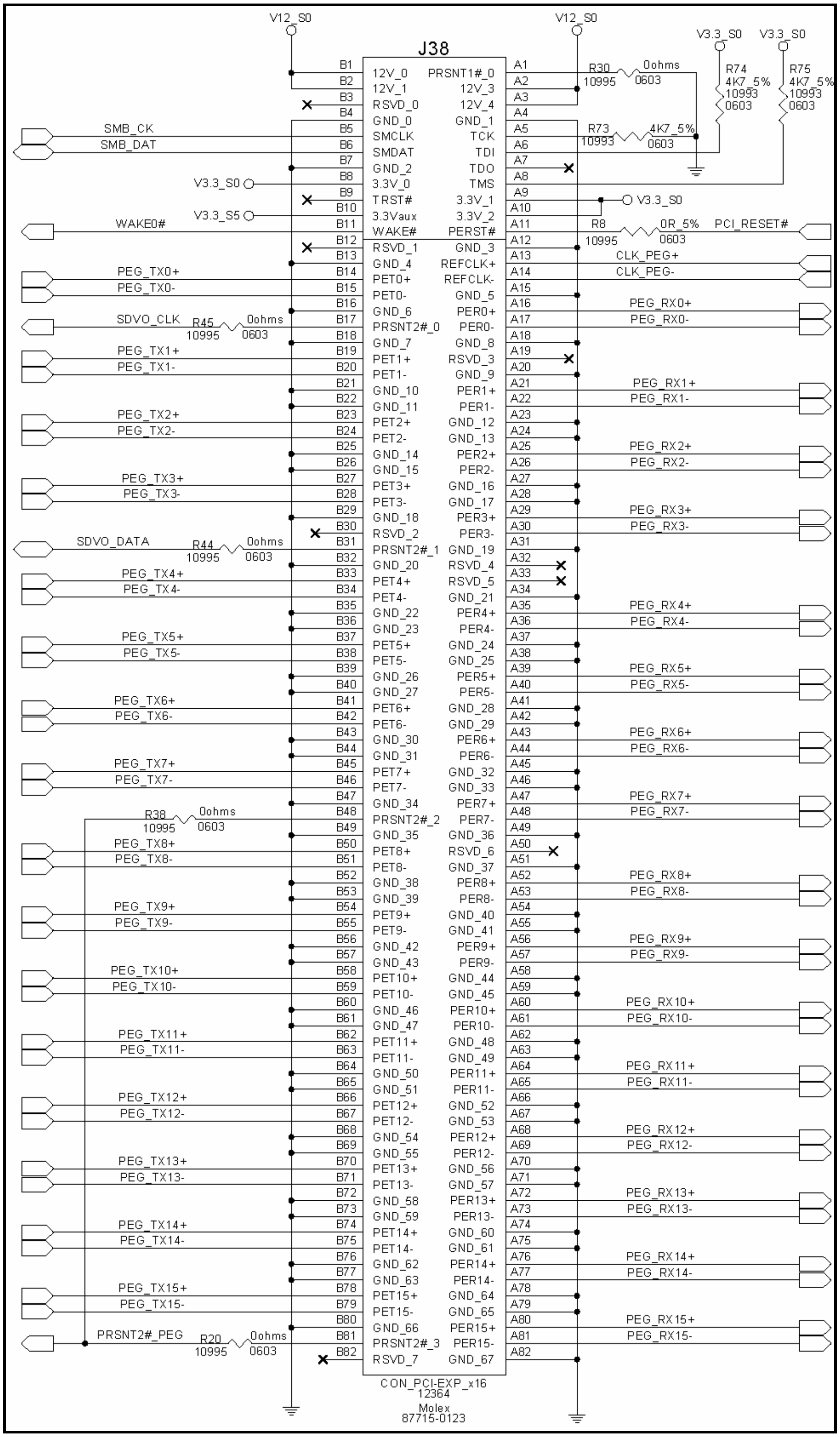
6.3.1 PEG Slot Normal Pin-out

The schematic for this example is shown in Figure 6-1 below.

- PEG Lanes 0-15 support a graphics-slot implementation.
- PEG_TX0+/- thru PEG_TX15+/- from the ETXexpress Module pins are connected to slot pins PET0+/- thru PET15+/- respectively.
- A normal pin-out is shown. The normal pin-out is preferred when the layout allows it because it is less confusing for all involved.
- The interface slot design in Figure 6-1 also is suitable for ADD2-N SDVO Plug-in cards.
- PEG Lanes have up to a 4GB/sec bandwidth capability, using an x16 interface.
- The Graphics Power Level delineation is as follows:
  25W (low profile), 75W (standard size), 150W (high end).
- The x16 connector can supply up to 75W of power.
- For a High End Card (75W to 150W), power will have to be supplied to the card via direct connection to the system power supply. Newer ATX power supplies have the appropriate connector.
- A High End card (75W to 150W) may use a two-slot I/O bracket for thermal management.
- The interface slot design shown also may be used for non-graphics PCIe Plug-in cards. The cards may have PCIe lane widths of x1, x4, x8, or x16. However, the Module may not support non-graphics PCIe applications over this interface.

- The WAKE# line may be asserted by the Graphics Card causing Module wake-up at ETXexpress Module pin B66 WAKE0#. WAKE0# is then pulled up on the ETXexpress Module to facilitate the “wire-ORed” interconnect from other WAKE0# sources.

Figure 6-1: PCIe X16 Graphics Slot– Normal Pin-out Schematic



These details apply to Figure 6-1 above.

- Nets SDVO_CLK and SDVO_DAT are sourced from ETXexpress Module pins D73 and C73 and are connected to Slot pins PRSNT2#_0 and PRSNT2#_1 respectively. They are used for an SDVO-specific I^2C bus.
  - The I^2C interface controls and configures SDVO functionality.
  - The two lowest "Card present" pins on the slot, PRSNT2#_0 and PRSNT2#_1 (slot pins B17 and B31) are used for the SDVO I^2C clock and data rather than to detect a card's presence.
  - PRSNT2#_0 and PRSNT2#_1 are not needed for PEG or SDVO because PEG cards are typically x8 or x16. Their presence is detected thru PRSNT2#_2 and PRSNT2#_3 respectively.
  - A 3.5KΩ resistor to 2.5V on these lines is not present on a PEG plug-in card but is on an SDVO plug-in card. Pull-ups allow the ETXexpress Module to determine if pins for PEG are being used for SDVO.
- ETXexpress Module pin D97 (PEG_ENABLE#) is connected to Slot pins B48 and B81 (PRSNT2#_2 and PRSNT2#_3) thru net PRESENT2#_PEG in Figure 6-1 above.
  - The dual-function signal enables Card detect and disables the on-module graphics capability.
  - The Card's presence is indicated by the Plug-In card, pulling PRSNT2#_2 or PRSNT2#_3 low. A PEG x8 card pulls PRSNT2#_2 low, and a PEG x16 card pulls PRSNT2#_3 low.
  - The internal graphics capability of the Module is disabled when the Module PEG_ENABLE# signal, pin D97, is pulled low by net PRSNT2#_PEG in Figure 6-1 above.
  - This signal is optionally routed to an input pin where it may be read by the BIOS or system software.
- Slot connector pin A1 (PRSNT1#_0) is pulled low on the Carrier Board. The slot card shorts this pin internally to PRSNT2#_2 (slot pin B48) for PEG x8 and PRSNT2#_3 (slot pin B81) for PEG x16.
- PERST# is driven by PCI_RESET#_B from Module pin C23, Module pin name PCI_RESET#, after buffering. This resets the plug-in card and causes initialization.
- REFCLK+ and REFCLK- are sourced from the Clock Buffer (described in Chapter 5). Plug-In cards may optionally use this clock source.
- PEG_RX0+/- thru PEG_RX15+/- from the ETXexpress Module pins are connected to PER0+/- thru PER15+/- respectively.

6.3.2 SDVO Slot – Normal Pin-Out

The following design details apply to Figure 6-1 above.

- SDVO channels B and C, SDVO_TV, SDVO_FLDSTALL are multiplexed with the PEG signals. Signals SDVO_I2C_CLK and SDVO_I2C_DAT are not multiplexed.

- SDVO_I2C_CLK and SDVO_I2C_DAT are sourced from ETXexpress Module pins D73 and C73 respectively.

    - A pull-up to 2.5V using a 3.5KΩ resistor is required for both lines on an SDVO plug-in card.
        - These pull-ups are not present on a PEG plug-in card.
        - If these two lines are sampled high by the ETXexpress Module, the PEG / SDVO lines are used for SDVO.
    - The SDVO_I2C bus relays display parameters and supports management functions.

- The slot (Figure 6-1 above) is suitable for an SDVO card with a normal pin-out (ADD2-N). A reverse pin-out card (ADD2-R) is used in a reverse pin-out slot (Figure 6-2 below).

6.3.3 PCIe x16 Non-Graphics

The 16 PCIe lanes listed in Table 6-1 above may be used for non-graphics applications in some situations. This is Module-dependent. Modules built with mobile chipsets (primarily intended for notebook use) usually do not have the capability to use the x16 PEG lines for anything other than an interface to a PCIe graphics chip. Some mobile chipsets allow the use of the PEG interface in a x1 mode for general-purpose use.

Chipsets that have wide PCIe lane capability for non-graphics uses usually are server-class chipsets. For modules that use server-class chipsets, the 16 PCIe lanes on the module usually used for graphics may instead be used for general purpose. In this case, the lanes are designated PCIe 16 thru 31. See Table 6-1 above.

With reference to Figure 6-1 above:

- The slot designed as shown is suitable for x8 and x16 cards with normal pin-outs.
    - A x8 slot card pulls Slot pin B48 (PRSNT2#_2) low and x16 pulls Slot pin B81 (PRSNT2#_3) low. These may be routed to a general purpose input pin to allow software to recognize whether a x8 or a x16 slot has been inserted.
- To support x1, x4 cards, interconnect PRSNT2#_0 and PRSNT2#_1 to the GPIO input pin on the Super I/O device.
    - Plug In x1 pulls PRSNT2#_0 low and x4 pulls PRSNT2#_1
- PEG_ENABLE# at ETXexpress Module pin D97 does not apply to this non-graphics interface.

6.3.4 PEG Slot – Reverse Pin-Out

The schematic for this example is shown in Figure 6-2 below.

- PEG_TX15+/- thru PEG_TX0+/- are sourced from the ETXexpress Module pins that are interconnected to PET0+/- thru PET15+/- respectively.
- PEG_RX15+/- thru PEG_RX0+/- from ETXexpress Module pins are interconnected to PER0+/- thru PER15+/- respectively.
- PEG_LANE_RV# on ETXexpress Module pin D54 should be strapped low.
  See Figure 4-3 above.
- This reverse pin-out eliminates a PCB layout "bow-tie."

6.3.5 SDVO Slot – Reverse Pin-out

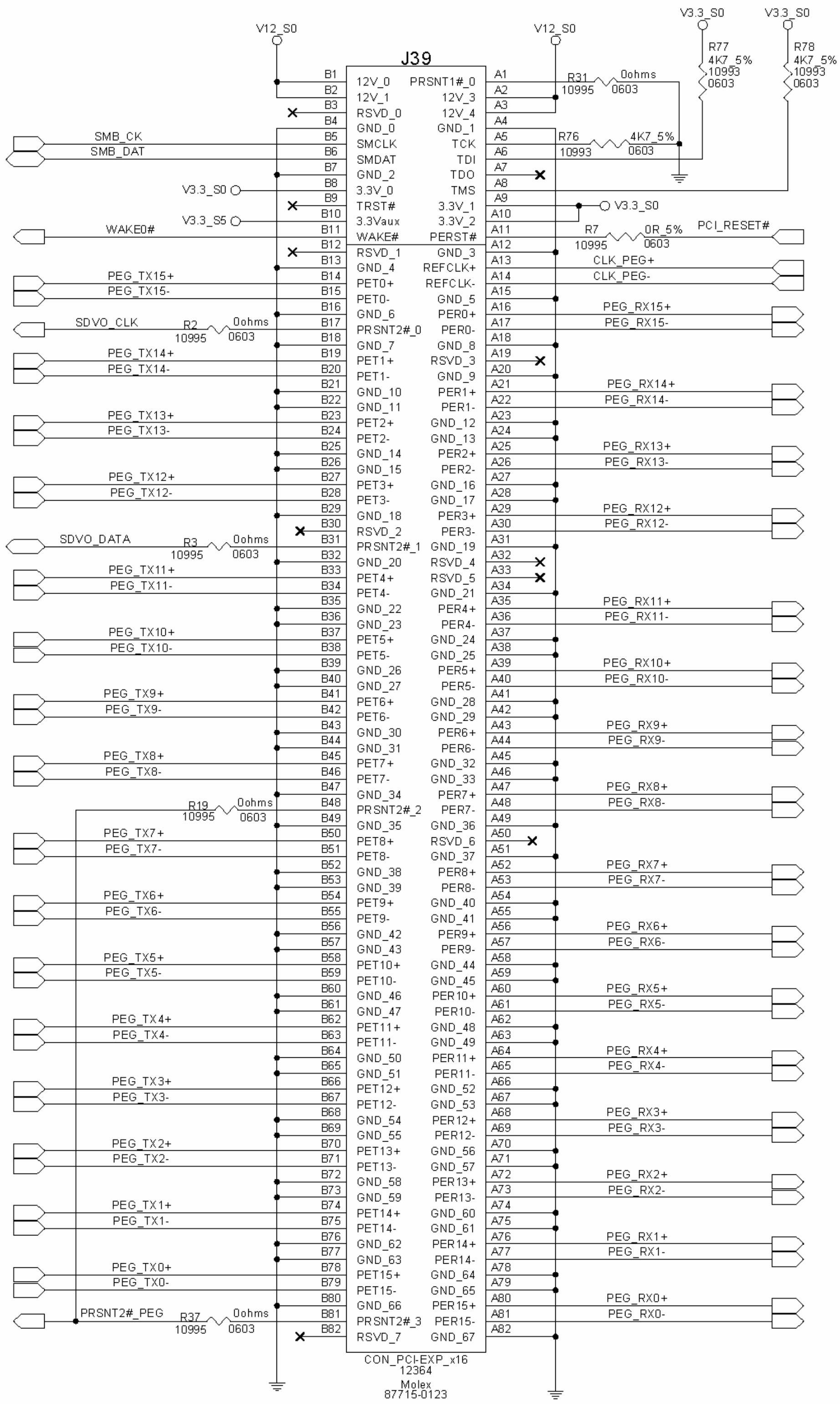
These design details apply to Figure 6-2 below.

- SDVO_I2C_CLK and SDVO_I2C_DAT are non-multiplexed and not reversed.
- SDVO channels B and C, SDVO_TV, SDVO_FLDSTALL are multiplexed with PEG signals and ARE reversed.
- The slot design shown in Figure 6.2 below is suitable for an SDVO card with a reverse pin-out.
- An SDVO card that has a REVERSED pin-out needs to be used. Such cards are designated ADD2-R.

6.3.6 PCIe x16 Non-Graphics – Reverse Pin-out

The reverse pin-out feature may not be available on non-graphics x16 , x8 and x4 implementations. Check relevant ETXexpress Module User Guides.

Figure 6-2: PCIe X16 Graphics Slot – Reverse Pin-out Schematic



NOTE: A reverse pinout requires a pulldown on the COM Express connector pin D54

6.3.7 SDVO to DVI-D Device-down

The schematic for this example can be found in Figures 6-3 and 6-4 below.

- PEG pins defined in Table 6-1 above support a single-channel, device-down application for SDVO to DVI implementation.
  - Table 6-1 above identifies the SDVO Channel B signals that are mapped to PEG pins, as defined in the COM Express™ Specification.
  - A Silicon Image transmitter IC (SIL1364) converts SDVO signals from the Module to a DVD-D format.
  - Pins are connected to the DVI-D Molex Connector 74320-4004.
- PEG_RX1+ and PEG_RX1- are sourced from ETXexpress Module pins C55 and C56 and are defined as SDVOB_INT+ and SDVOB_INT- in the COM Express™ Specification respectively. They are driven by SDI+ and SDI- from the chip.
  - The PEG Receive interface on the ETXexpress Module is driven by the TX source (Interrupt) on the SDVO chip.
  - The TX source needs to be AC-coupled near the source (SDI pins).
- EXT_RES is pulled low thru a 1.0KΩ resistor to generate a reference-bias current.
- PEG_TX0+/- thru PEG_TX3- from ETXexpress Module pins are defined as SDVO_RED+/-, GRN+/-, BLU+/- and CK+/- in the COM Express™ Specification respectively. They drive SDR+/-, SDG+/-, SDB+/- and SDC+/- on the chip.
  - The PEG Transmit interface on the ETXexpress Module drives the RX load on the graphics chip.
- SDVO_I2C_CLK and SDVO_I2C_DAT are sourced from ETXexpress Module pins D73 and C73 respectively.
  - A pull-up to 2.5V using a 3.5KΩ resistor is required for both lines on the Carrier Board for a device-down application. For an SDVO slot design, pull-ups are on the SDVO plug-in card.
  - The I^2C Bus supports management functions and provides Manufacturer information, a model number, and a part number.
  - Save its state for suspend event, report errors, accept control parameters, and return status.
- RESET# is driven by the PCI_RESET#_B from ETXexpress Module pin C23, PCI_RESET#, after buffering.
  - The signal resets the chip and causes initialization.
- A1 establishes the I^2C default address.
  - Pulled Low = 0X70 (unconnected).
  - Pulled High = 0X72 thru a 4.7KΩ resistor.
- HTPLUG – The Hot Plug input is driven by the Monitor Device, which causes the System OS to initiate a Plug and Play sequence that results in identifying the configuration of the Monitor. Protection diodes and a current-limiting resistor also are added.
- TEST – The factory test pin needs to be tied low for normal operation.

- EXT_SWING should be tied to AVCC pins thru a 360Ω resistor. It sets the amplitude voltage swing. Smaller values set a larger voltage swing and vice versa.

- SDAROM and SCLROM interface to a non-volatile memory U17, Serial Prom AT24C04.

- TX0+/- thru TX2+/- DVI output pins are TMDS low voltage differential signals.

- TXC+/- DVI Clock pins are TMDS low voltage differential signals.

- SCLDDC and SDADDC should be pulled up with a 2.2KΩ resistor. They serve as the signals for the I^2C interface to the DVI connector.

    - The interface supports the DDC (Display Data Channel) standard for EDID (Extended Display Identification Data) over I^2C.

    - The EDID includes the manufacturer's name, product type, phosphor or filter type, timings supported by the display, display size, luminance data and pixel mapping data (for digital displays only).

- SDAROM and SCLROM external pull-ups are not required because they are internally pulled up. They serve as signals for the I^2C interface to EEPROM AT24C04.

The following details apply to Figure 6.4 below, Schematic 2 of 2.

- The schematics show the requirements for decoupling and the filter caps for the SIL1364 graphics chip.

Figure 6-3: SDVO to DVI Schematic (1 of 2)

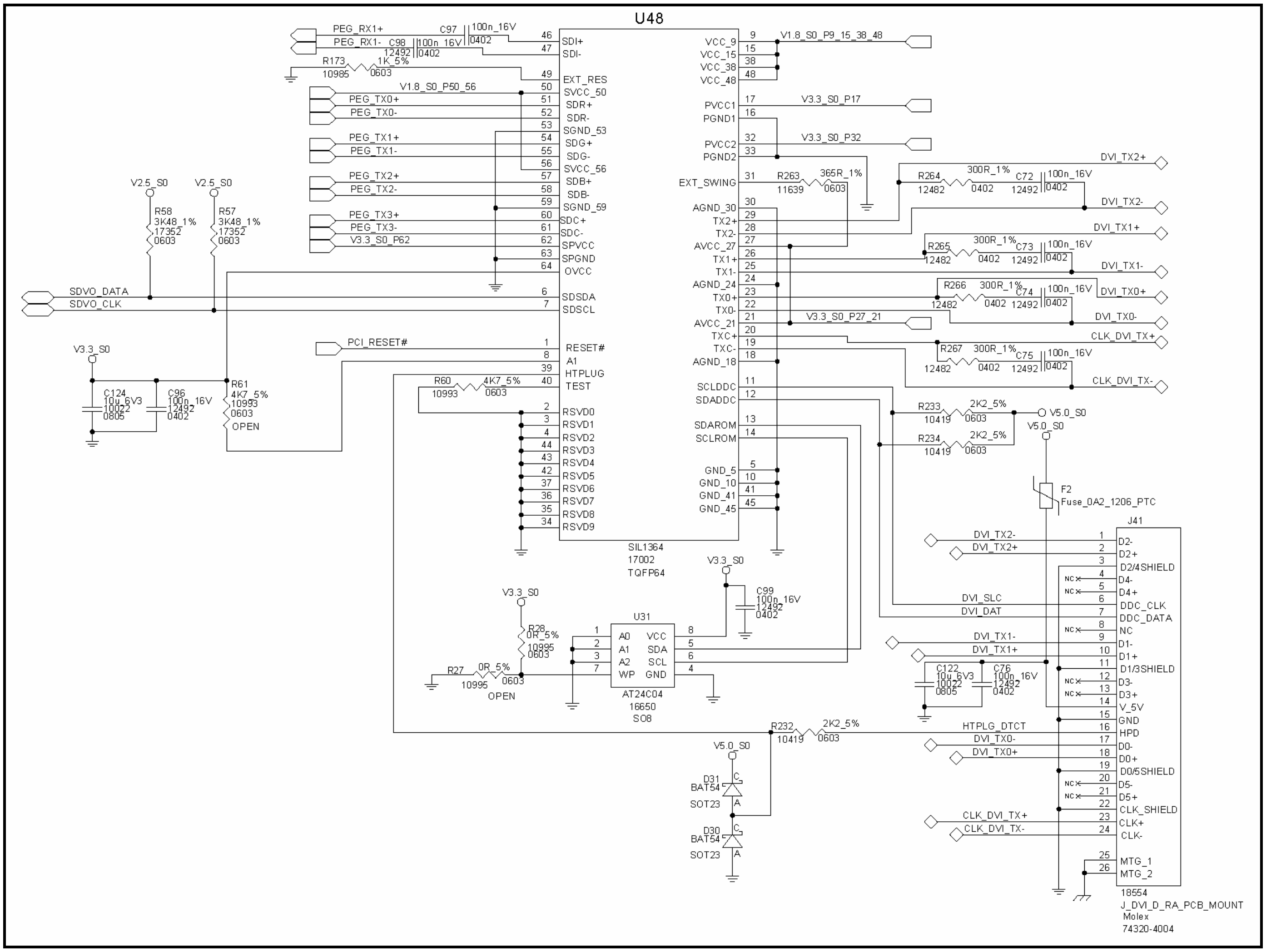
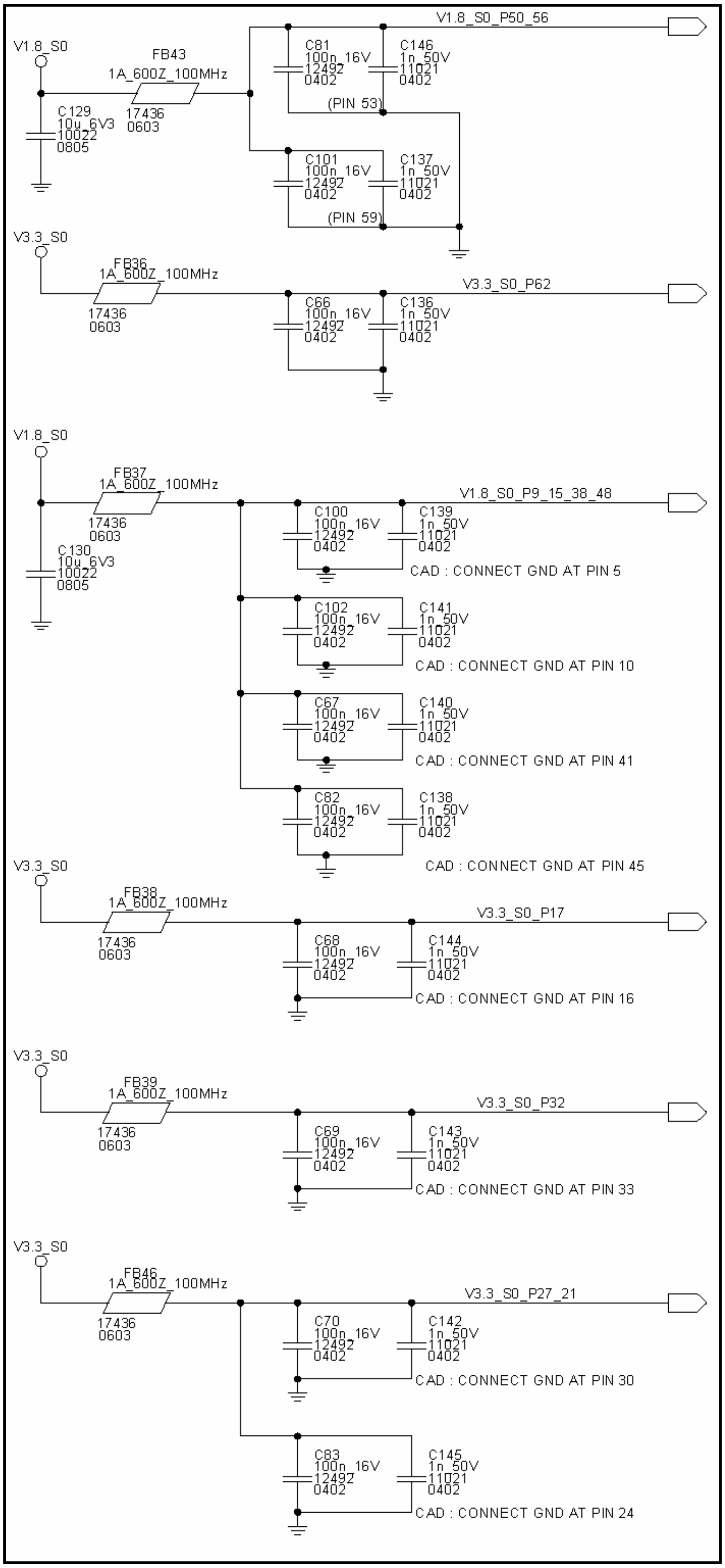


Figure 6-4: SDVO to DVI Schematic (2 of 2)



6.3.8 Other SDVO Output Options: LVDS, NTSC

- LVDS transmitters that accept SDVO inputs are available. The Chrontel CH7308 is one such device.

- NTSC encoders that accept SDVO inputs are available from vendors such as Chrontel.

7 LAN 0

7.1 LAN 0 – Signal Definitions

The LAN 0 port defines a set of pins on the A-B connector to support a 10/100 megabits per second or Gigabit Ethernet LAN (Local Area Network) implementation. All ETXexpress Modules must support at least 10/100 megabits per second operation on LAN0. The COM Express™ Specification specifies that LAN magnetics must reside on the Carrier Board, not on the Module. The LAN interface consists of four differential pair signals, designated as GBE0_MDI0+,- thru GBE0_MDI3+,-. Additionally, there are four single-ended signals that provide link-status information, along with a reference voltage for the magnetics center tap.

Table 7-1: LAN 0 Pin-outs

Row A			Row B	
A1	GND (FIXED)		B1	GND (FIXED)
A2	GBE0_MDI3-		B2	GBE0_ACT#
A3	GBE0_MDI3+		B3	
A4	GBE0_LINK100#		B4	
A5	GBE0_LINK1000#		B5	
A6	GBE0_MDI2-		B6	
A7	GBE0_MDI2+		B7	
A8	GBE0_LINK#		B8	
A9	GBE0_MDI1-		B9	
A10	GBE0_MDI1+		B10	
A11	GND (FIXED)		B11	
A12	GBE0_MDI0-		B12	
A13	GBE0_MDI0+		B13	
A14	GBE0_CTREF		B14	

7.2 LAN 0 – Routing Considerations

- The four differential pairs for LAN 0 are:

  GBE0_MDI0+ and GBE0_MDIO-
  GBE0_MDI1+ and GBE0_MDI1-
  GBE0_MDI2+ and GBE0_MDI2-
  GBE0_MDI3+ and GBE0_MDI3-

- Route LAN differential pairs with 100-ohm differential impedance and 55-ohm, single-ended impedance.

- Keep LAN connections as short as possible. Appendix A summarizes LAN trace-routing parameters.

- Terminate all unused connections on the RJ45 cable and the magnetics module to ground.

- For the magnetics module, separate the digital ground on the primary side and the chassis ground on the secondary side.

- The use of RJ45 jacks with integrated magnetics is strongly recommended.

7.3 LAN Magnetics Connections

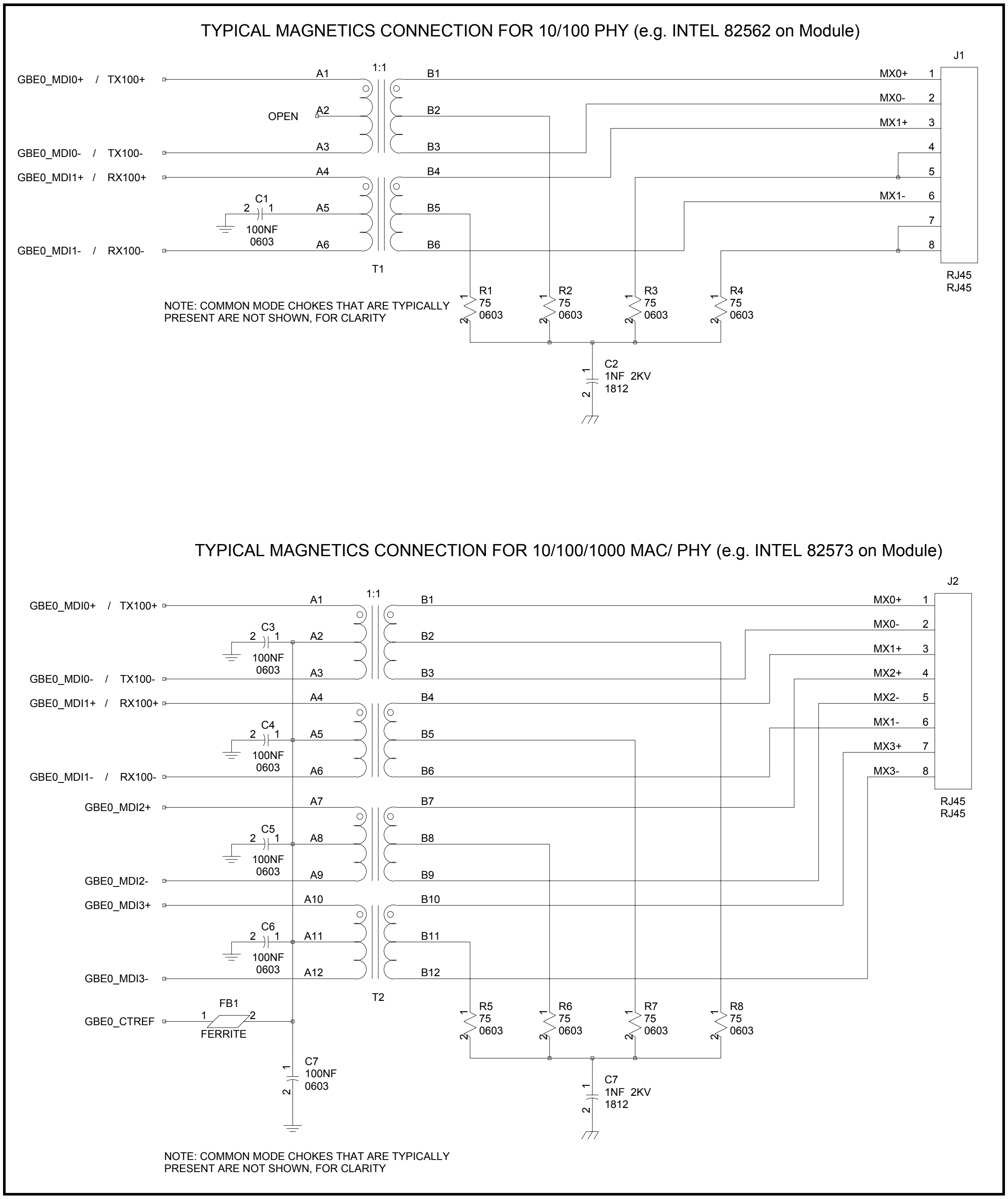
- The isolation transformers used for 10/100 PHY implementations and for GBE (10/100/1000) implementations are very similar. It is possible to use the same magnetics for these two cases, but the transformer center-taps need to be treated differently, as shown in Figure 7-1 below.

- For 10/100 megabits per second implementations, the Module 10/100 transmit pair uses Module pins GBE_MDI0+,-. The Module 10/100 receive pair uses Module pins GBE_MDI1+,-. Module pins GBE_MDIO2+,- and GBE_MDIO3+,- may be left unconnected if there is no need for GBE.

- Numerous magnetics modules are available that integrate most of the components shown in either the upper or lower parts of Figure 7-1 into a single device. Ferrite FB1 and capacitor C7 are not integrated, but all other components can be integrated (and are in some models). However, if a module is selected that ties all the center-taps together internally and includes capacitors C3, C4, C5 and C6 (as shown in the lower part of Figure 7-1), then the alternate center tap connections for 10/100 PHYs (upper part of Figure 7-1) cannot be achieved.

- It is possible to create a circuit using a fast analog multiplexor, such as the Pericom PI5C3257, to make the alternate center-tap connections for the 10/100 and GBE cases. The multiplexor switch is controlled by logic derived from the GBE0_CTREF signal. For Modules with a GBE controller such as the Intel 82573, GBE0_CTREF is driven to 2.5V. For Modules using a 10/100 PHY such as the Intel 82562, the Module leaves GBE0_CTREF floating. A Carrier Board can use GBE0_CTREF, with a pulldown resistor, to control a FET gate which in turn drives the PIC3257 control lines.

Figure 7-1: LAN 0 Magnetics Connections



7.4 LAN 0 – Reference Schematics

The following notes apply to Figure 7-2 below.

- Connector J1 is an RJ45 jack that has integrated magnetics, which are suitable for Modules with 10/100/1000 (GBE) PHYs and for Modules with 10/100 PHYs. The jack includes secondary side termination resistors and LEDs as indicated in the schematic. The jack shown is Pulse Engineering JK0-0036.

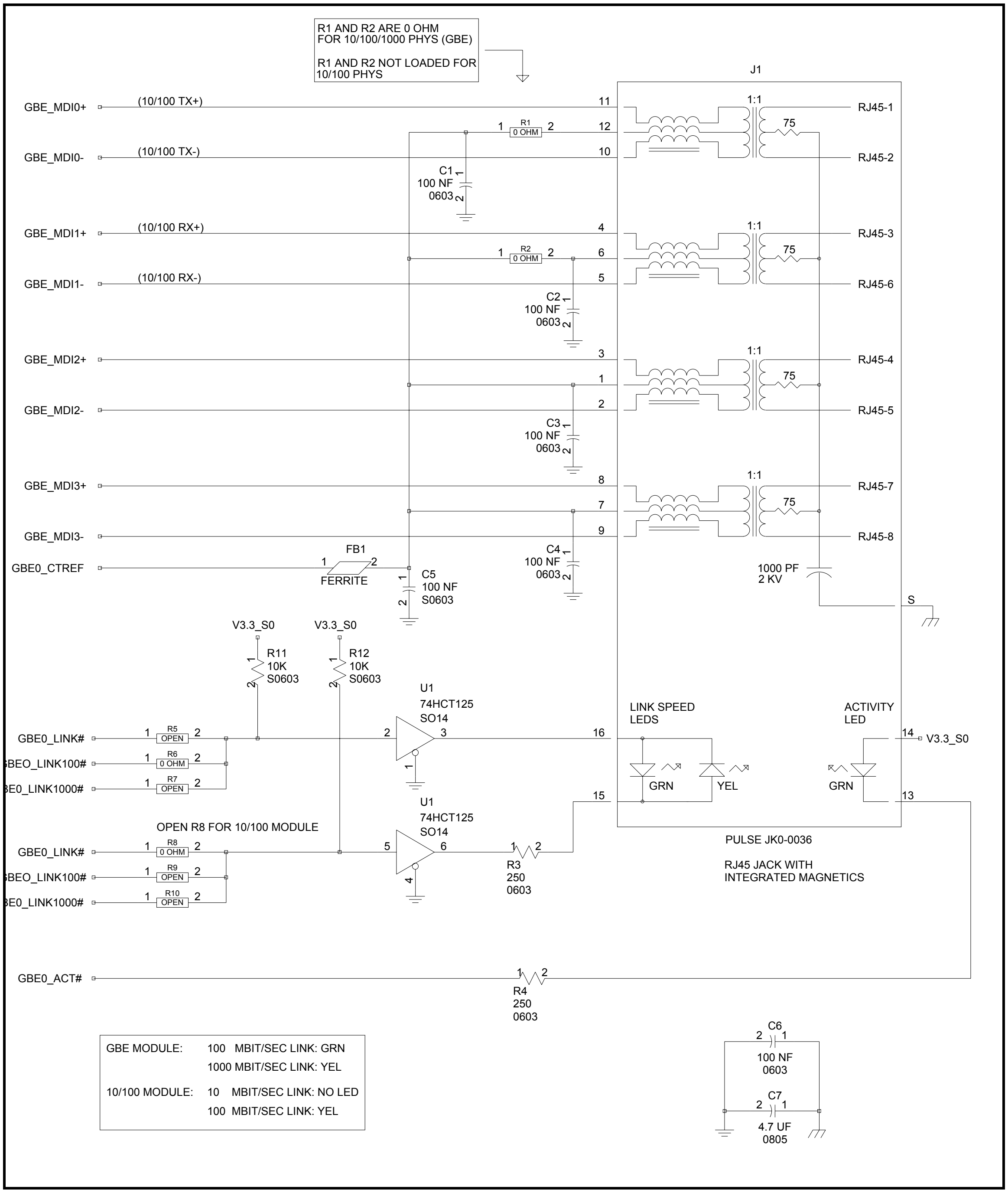
- If this jack is used with a Module that uses a 10/100 PHY rather than a GBE controller, then the center-tap connection for the 10/100 transmit pair (on nets GBE0_MDI0+.-) must be left open, by not loading resistor R1 in the figure. Similarly, the center-tap connection for the 10/100 receive pair must be disconnected from the DC bias provided by the GBE0_CTREF connection, by not loading resistor R2.

- There are some variations in the way Module implementations treat the COM Express Link lines (GBE0_LINK#, GBE0_LINK100#, GBE0_LINK1000#). The resistor options shown here allow for maximum flexibility in this regard.

- Discrete circuitry with additional LEDs are needed to show all 3 LAN bit rates independently.

- Check with your Kontron FAE or the Kontron Web site for additional Module-specific information on these topics.

Figure 7-2: 10/100/1000 Ethernet Schematic



8 USB Ports 0-7

8.1 USB 0-7 – Signal Definitions

An ETXexpress Module can support up to eight USB 2.0 ports. A minimum of four ports from this group are required for all Module Types. All eight ports appear on the COM Express A-B connector as shown in Table 8-1 below.

There are four USB over-current lines defined in the COM Express™ Specification. The over-current lines are shared by ports 0 and 1; by ports 2 and 3; by ports 4 and 5 and by ports 6 and 7. The over-current lines are inputs to the module that are driven low by open-drain off-module monitoring hardware to signal an over-current condition. Carrier Boards that supply power to external USB devices over a USB cable should implement current-limiting hardware and should drive the appropriate over-current line. If the USB target device is on the Carrier Board, then it is not necessary to implement the current-limiting and to drive the over-current line for that port.
The over-current line may be left open.

Table 8-1: USB 0-7 Pin-outs

Row A			Row B	
A36	USB6-		B36	USB7-
A37	USB6+		B37	USB7+
A38	USB_6_7_OC#		B38	USB_4_5_OC#
A39	USB4-		B39	USB5-
A40	USB4+		B40	USB5+
A41	GND (FIXED)		B41	GND (FIXED)
A42	USB2-		B42	USB3-
A43	USB2+		B43	USB3+
A44	USB_2_3_OC#		B44	USB_0_1_OC#
A45	USB0-		B45	USB1-
A46	USB0+		B46	USB1+

8.2 USB Ports 0-7 – Routing Considerations

Route USB signals as differential pairs, with a 90-ohm differential impedance and a 45-ohm, single-ended impedance. Ideally, a USB pair is routed on a single layer adjacent to a ground plane. USB pairs should not cross plane splits. Keep layer transitions to a minimum.
Reference USB pairs to a power plane if necessary. The power plane should be well-bypassed. Appendix A summarizes USB routing rules.

8.3 USB Ports 0-7 – Reference Schematics

The following notes apply to Figures 8.1 thru 8.4 below.

- J11, J12, and J13 are dual connectors that incorporate two USB Type A receptacles.

- The Texas Instruments TPS2042AD is a dual-power distribution switch that provides over-current protection.

    - EN1# and EN2# are tied low to turn power on thru OUT1 and OUT2.
    - OUT1 and OUT2 provide power to the USB connector pins thru ferrites to keep high frequency noise off of the USB cables. The ferrites should be adjacent to the connector pins.
    - OC1# and OC2# are over-current signals that are inputs to ETXexpress Module pins B44, A44, B38 and A38 for USB_0_1, USB_2_3, USB_4_5 and USB_6_7 respectively.
    - Each signal is driven low by the chip upon detection of overload, short-circuit or thermal trip, which causes the affected switch to turn off. The adjacent switch is not affected.
    - Do not pull the OC signals high to 3.3V on the ETXexpress Carrier Board; this is done on the ETXexpress Module.
    - The signal is asserted until the over-current or over-temperature condition is resolved.

- USB0+/- thru USB7+/- from the ETXexpress Module are routed thru a common mode choke to reduce radiated cable emissions. The part shown is a Coilcraft 0805USB-901MLC; this device has a common mode impedance of approximately 90 ohms at 100MHz.
  The common-mode choke should be placed close to the external connector.

Figure 8-1: USB Ports 0 and 1 Schematic (1 of 4)

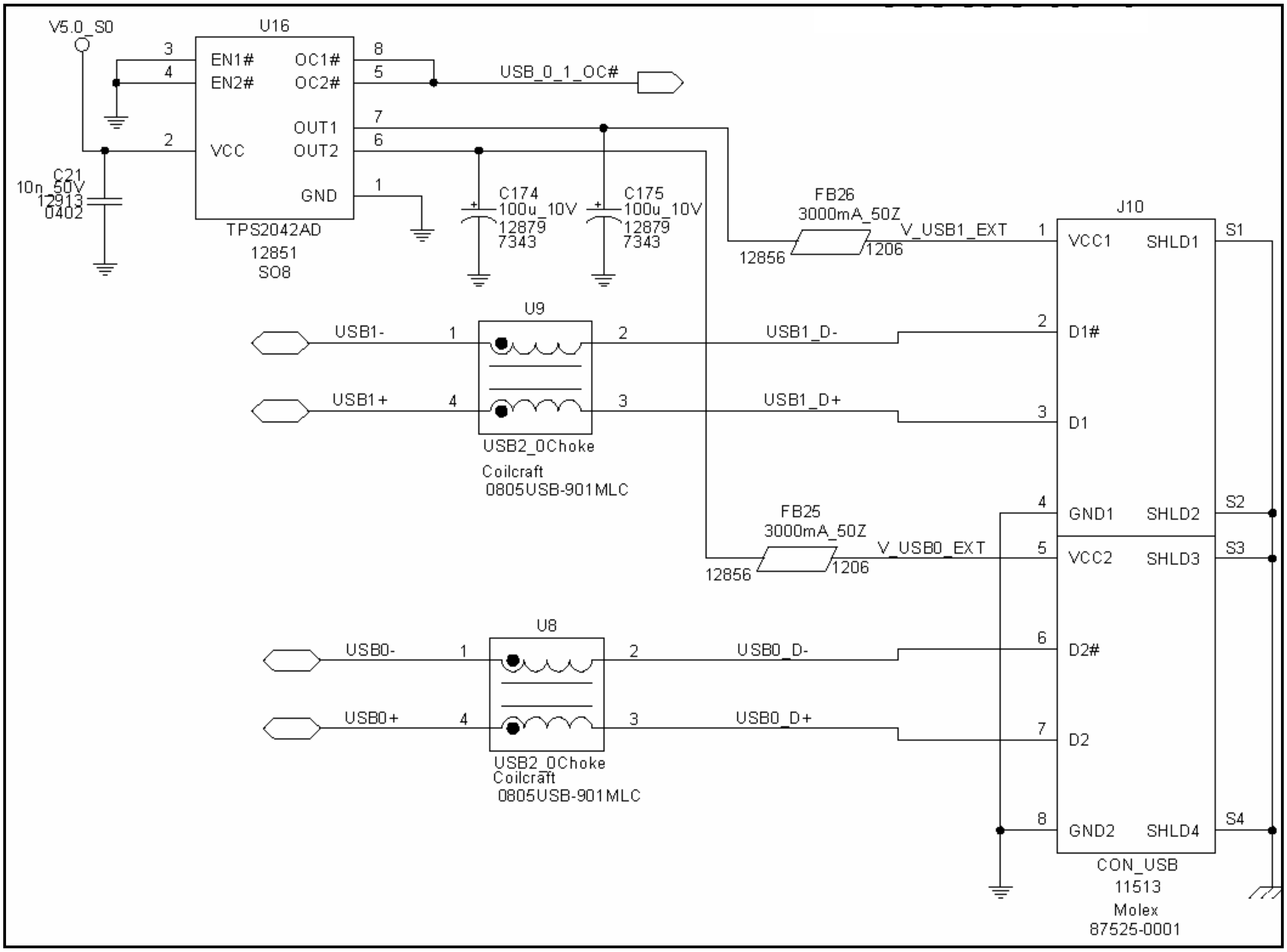


Figure 8-2: USB Ports 2 and 3 Schematic (2 of 4)

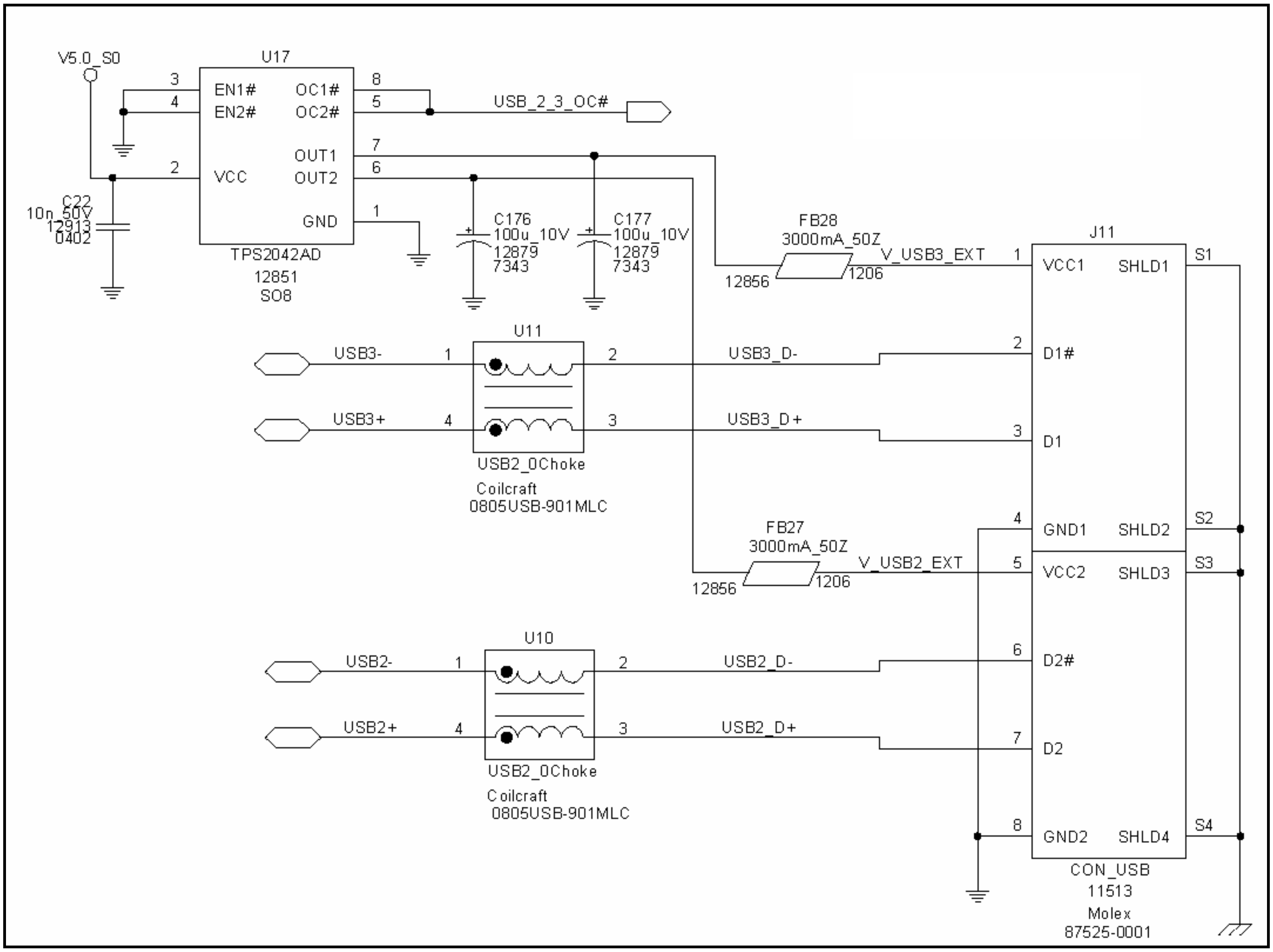


Figure 8-3: USB Ports 4 and 5 Schematic (3 of 4)

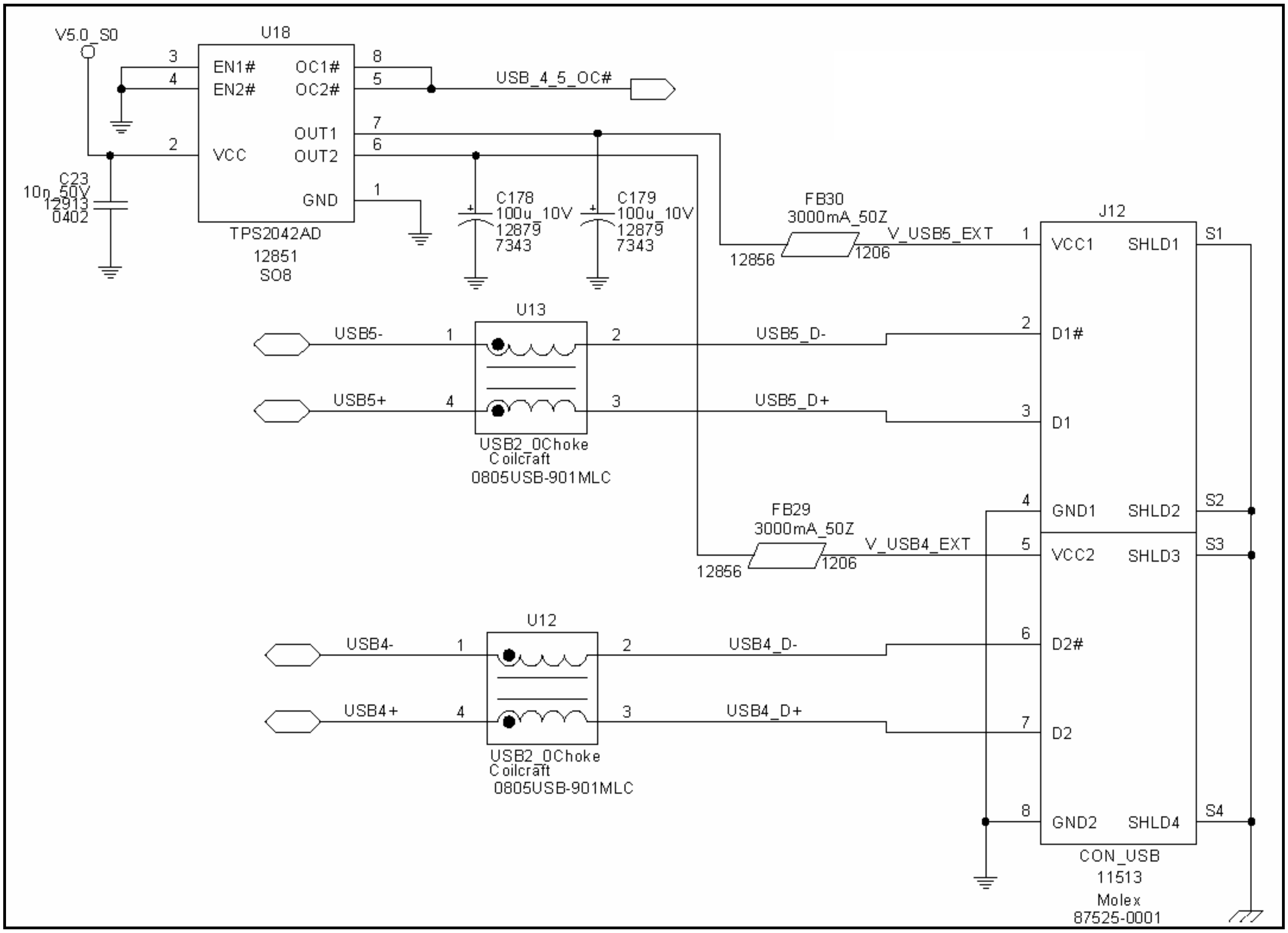
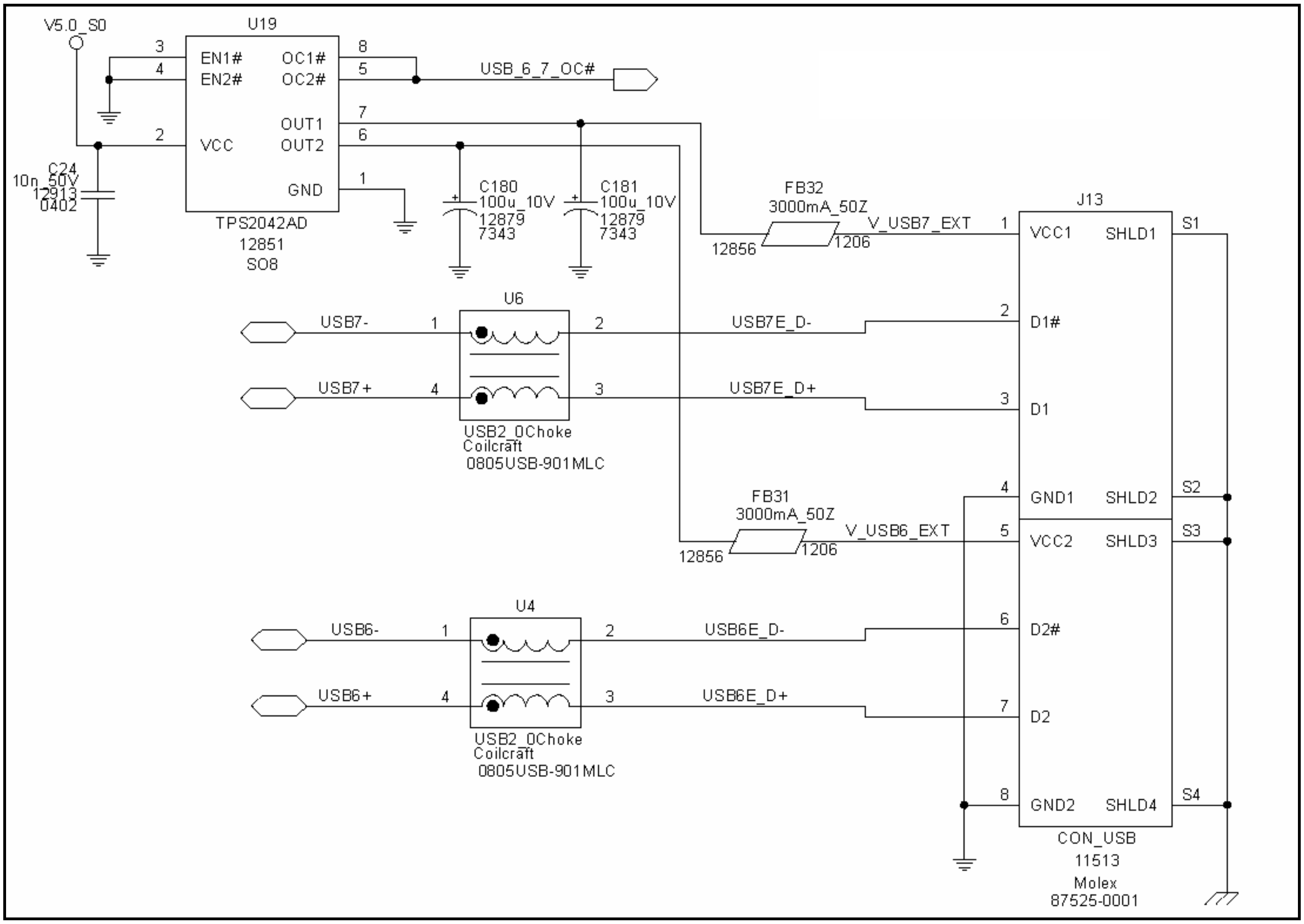


Figure 8-4: USB Ports 6 and 7 Schematic (4 of 4)



9 SATA 0-3

9.1 SATA 0-3 – Signal Definitions

Support for up to four SATA ports is defined on the COM Express A-B connector. Support for a minimum of two ports is required for all Module Types. The COM Express™ Specification allows for both SATA-150 (150 megabits per second; 1st generation of SATA) and SATA-300 (300 megabits per second; 2nd generation) implementations. Constraints for SATA-300 implementations are more severe than those for SATA-150. The COM Express™ Specification addresses both in the section on insertion losses.

Table 9-1: SATA 0-3 Pin-outs

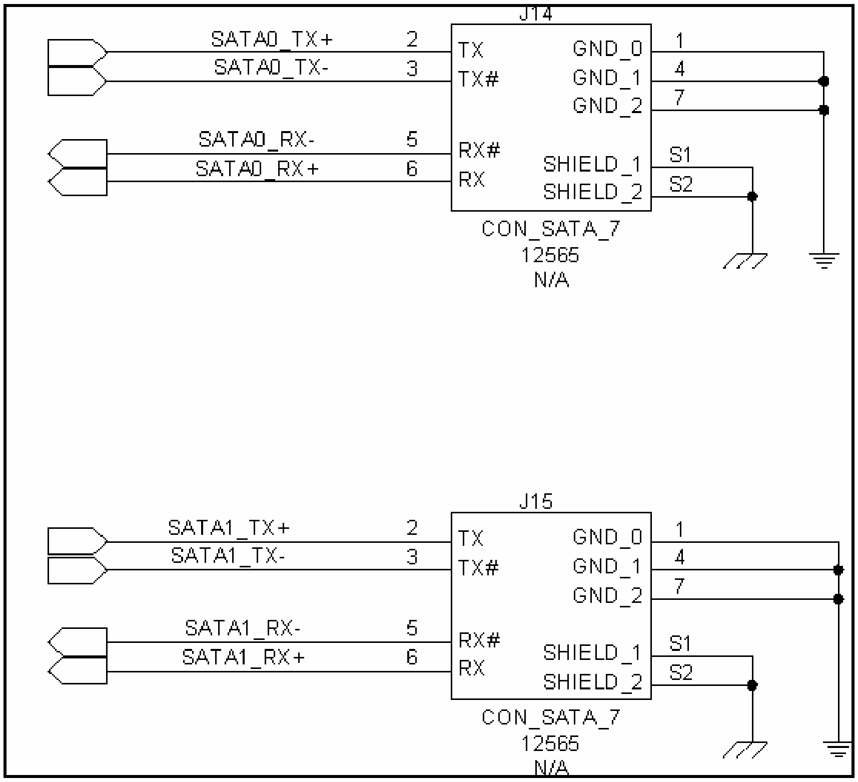
Row A			**Row B**		
A16	SATA0_TX+		B16	SATA1_TX+	
A17	SATA0_TX-		B17	SATA1_TX-	
A18			B18		
A19	SATA0_RX+		B19	SATA1_RX+	
A20	SATA0_RX-		B20	SATA1_RX-	
A21	GND (FIXED)		B21	GND (FIXED)	
A22	SATA2_TX+		B22	SATA3_TX+	
A23	SATA2_TX-		B23	SATA3_TX-	
A24			B24		
A25	SATA2_RX+		B25	SATA3_RX+	
A26	SATA2_RX-		B26	SATA3_RX-	

9.2 SATA 0-3 – Routing Considerations

Route SATA signals as differential pairs, with a 100-ohm differential impedance and a 55-ohm, single-ended impedance. Ideally, a SATA pair is routed on a single layer adjacent to a ground plane. SATA pairs should not cross plane splits. Keep layer transitions to a minimum. Reference SATA pairs to a power plane if necessary. The power plane should be quiet and well bypassed. SATA-150 routing rules also are summarized in Appendix A.

9.3 SATA 0-3 – Reference Schematic

Figure 9-1: SATA Port Schematic



The following notes apply to Figure 9-1 above.

- The connectors shown are Molex 67491-0019, a 1.27mm-pitch, 7-pin, high-speed vertical plug. This type carries SATA data pairs and the GND reference only. Power for the SATA drive is not included on this connector type. Power for the SATA drive is delivered thru a separate connector from the system ATX power supply.
- Alternate 22-pin connector types are available that deliver power and data to the SATA drive. This may be over a combined power/data cable or in a direct configuration in which the SATA drive mates directly to the 22-pin plug on the Carrier Board. Please refer to the SATA specification (Appendix G) for pin-out information.
- Nets SATA0_TX+/- thru SATA3_TX +/- are sourced from the ETXexpress Module SATA TX pins.
- Nets SATA0_RX+/- thru SATA3_RX +/- are sourced from SATA disks and are routed to the ETXexpress Module SATA RX pins.
- Coupling capacitors are not needed on Carrier Board SATA lines. They are present on the ETXexpress Module.

10 LVDS

10.1 LVDS – Signal Definitions

The COM Express™ Specification provides an optional LVDS interface on the COM Express A-B connector. Module pins for two LVDS channels are defined and designated as LVDS_A and LVDS_B.

Systems use a single-channel LVDS for most displays. Dual LVDS channels are used for very high-bandwidth displays. Single-channel LVDS means that one complete RGB pixel is transmitted per display input clock (also known as the shift clock. See Table 10-2 below for a summary of LVDS terms). Dual-channel LVDS means that two complete RGB pixels are transmitted per display input clock. The two pixels are adjacent along a display line. Dual-channel LVDS does not mean that two LVDS displays can be driven.

Each COM Express LVDS channel consists of four differential data pairs and a differential clock pair for a total of five differential pairs per channel. ETXexpress Modules and Module chipsets may not use all pairs. For example, for 18-bit TFT displays, only three of the four data pairs on the LVDS_A channel are used, along with the LVDS_A clock. The LVDS_B lines are not used. The manner in which RGB data is packed onto the LVDS pairs (including packing order and color depth) is not specified by the COM Express™ Specification. This may be Module-dependent. Further mapping details are given in Section 10.3 below.

There are five single-ended signals included to support the LVDS interface: two lines are used for an I^2C interface that may be used to support EDID, JILI, or other panel information and identification schemes. Additionally, there are an LVDS power enable (LVDS_VDD_EN) and backlight control and enable lines (LVDS_BKLT_CTRL and LVDS_BKLT_EN).

Table 10-1: LVDS A and B Pin-outs

Row A			Row B	
A70	GND (FIXED)		B70	GND (FIXED)
A71	LVDS_A0+		B71	LVDS_B0+
A72	LVDS_A0-		B72	LVDS_B0-
A73	LVDS_A1+		B73	LVDS_B1+
A74	LVDS_A1-		B74	LVDS_B1-
A75	LVDS_A2+		B75	LVDS_B2+
A76	LVDS_A2-		B76	LVDS_B2-
A77	LVDS_VDD_EN		B77	LVDS_B3+
A78	LVDS_A3+		B78	LVDS_B3-
A79	LVDS_A3-		B79	LVDS_BKLT_EN
A80	GND (FIXED)		B80	GND (FIXED)
A81	LVDS_A_CK+		B81	LVDS_B_CK+
A82	LVDS_A_CK-		B82	LVDS_B_CK-
A83	LVDS_I2C_CK		B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT		B84	

10.2 LVDS – Routing Considerations

Route LVDS signals as differential pairs (excluding the five single-ended support signals), with a 100-ohm differential impedance and a 55-ohm, single-ended impedance. Ideally, a LVDS pair is routed on a single layer adjacent to a ground plane. LVDS pairs should not cross plane splits. Keep layer transitions to a minimum. Reference LVDS pairs to a power plane if necessary.
The power plane should be well-bypassed.

Length-matching between the two lines that make up an LVDS pair (“intra-pair”) and between different LVDS pairs (“inter-pair”) is required. Intra-pair matching is tighter than the inter-pair matching.

All LVDS pairs should have the same environment, including the same reference plane and the same number of vias.

Appendix A summarizes LVDS routing rules.

10.3 LVDS – Color Mapping and Terms

10.3.1 FPD-Link and Open LDI Color Mapping

An LVDS stream consists of frames that pack seven data bits per LVDS frame. Details can be found in the tables below. The LVDS clock is one seventh of the source-data clock. The order in which panel data bits are packed into the LVDS stream is referred to as the LVDS color-mapping. There are two LVDS color-mappings in common use: FPD-Link and Open LDI. FPD-Link is the older standard but is being eclipsed by Open LDI.

The FPD-Link and Open LDI standards are the same for panels with color depths of 18 bits (6 Red, 6 Green, 6 Blue) or less. The 18 bits of color data and 3 bits of control data, or 21 bits total, are packed into 3 LVDS data streams. The LVDS clock is carried on a separate channel for a total of 4 LVDS pairs – 3 data pairs and a clock pair.

For 24-bit color depths, a 4th LVDS data pair is required (for a total of 5 LVDS pairs – 4 data and 1 clock). FPD-Link and Open LDI differ in this case. FPD-Link keeps the least significant color bits on the original 3 LVDS data pairs and adds the most significant color bits (the dominant or “most important” bits) to the 4th channel. Six bits are added: 2 Red, 2 Green, and 2 Blue (the seventh available bit slot in the 4th LVDS stream is not used).

A 24-bit, Open LDI implementation shifts the color bits on the original 3 LVDS data pairs up by two, such that the most significant color bits for both 18- and 24-bit panels occupy the same LVDS slots. For example, the most significant Red color bit is R5 for 18-bit panels and R7 for 24-bit panels. The 18-bit R5 and the 24-bit R7 occupy the same LVDS bit slot in Open LDI. The 4th LVDS data stream in Open LDI carries the least significant bits of a 24-bit panel – R0, R1, G0, G1, B0, and B1.

The advantage of Open LDI is that it provides an easier upgrade and downgrade path than FPD-Link does. An 18-bit panel can be used with an Open LDI 24-bit data stream by simply connecting the 1st three LVDS data pairs to the panel, and leaving the 4th LVDS data pair unused. This does not work with FPD-Link because the mapping for the 24-bit case is not compatible with the 18-bit case – the most significant data bits are on the 4th LVDS data stream.

Current Intel chipsets such as the 915GM and the 945GM use Open LDI mapping.

If you design LVDS de-serializers, work around the Module color-mapping by picking off the de-serializer outputs in the order needed. If you use a flat panel with an integrated LVDS receiver, it is important that the display’s color-mapping matches the Module’s color-mapping.

10.3.2 Note on Industry Terms

Some terms in this document that describe LVDS displays may vary from other documents (such as display data sheets from vendors, IC data sheets for graphics controllers and LVDS transmitters and receivers, the Open LDI specification, and ETXexpress Module documentation).

Examples of terms that may vary include:

- For dual-channel displays, terms are needed to describe the adjacent pixels. Various documents will reference for the same pair of pixels:
  - Odd and Even pixels (column count starts at 1)
  - Even and Odd pixels (column count starts at 0)
  - R10 and R20 for adjacent least significant Red bits
  - R00 and R10 for adjacent least significant Red bits
- Terms used to describe the clocks vary:
  - The Open LDI specification uses the term “pixel clock” differently from most other documents. In the Open LDI specification, the “pixel clock” period is seven pixel periods long. Most other documents refer to this concept as the “LVDS clock.”
- Transmit Bit Order
  - In this document, the seven bits in an LVDS frame are numbered 1 – 7, with Bit 1 being placed into the stream before Bit 2.
  - Some documents use an opposite convention. The Kontron JILI Version 2.0 Specification has the bits numbered in opposite order.

Display terms used in this document are defined in Table 10-2 below.

Table 10-2: LVDS Display Terms and Definitions

Term	Definition
Color-Mapping	Color-mapping refers to the order in which display color bits and control bits are placed into the serial LVDS stream. Each LVDS data frame can accept seven bits. The way in which the bits are serialized into the stream is arbitrary, as long as they are de-serialized in a corresponding way. Two main color-mapping schemes are FPD-Link and Open LDI. They are the same for 18-bit panels but differ for 24-bit panels.
DE	Display Enable – a control signal that asserts during an active display line.
Dual Channel	In a dual-channel bit stream, two complete RGB pixels are transmitted with each shift clock. The shift clock is one half the pixel frequency in this case. Dual channel LVDS streams are either 8 differential pairs (6 data pairs, 2 clock pairs, for dual 18 bit streams) or 10 differential pairs (8 data pairs, 2 clock pairs, for dual 24-bit streams).
Even Pixel	A pixel from an even column number, counting from 1. For example, on an 800x600 display, the even pixels along a row are in columns 2,4 … 800. The odd pixels are in columns 1,3,5 … 799.
FPD-Link	Flat Panel Display Link – an LVDS color-mapping scheme popularized by National Semiconductor. FPD Link color-mapping is the same as open LDI color-mapping for 18-bit displays but is different for 24-bit displays. FPD color-mapping puts the most significant bits of a 24-bit display onto the 4th LVDS channel.
HSYNC	Horizontal Sync – a control signal that occurs once per horizontal display line.
LCLK	LVDS clock – the low voltage differential clock that accompanies the serialized LVDS data stream. For a single-channel LVDS stream, the LVDS clock is 1/7th the pixel clock, which means there is one LVDS clock period for every 7 pixel clock periods. For a dual-channel LVDS data stream, the LVDS clock is 1/14th the pixel clock, which means there is one LVDS clock period for every 14-pixel clock periods.
Odd Pixel	A pixel from an odd column number, counting from 1. For example, on an 800x600 display, the odd pixels along a row are in columns 1,3,5, … 799. The even pixels are in columns 2,4 …800.
Open LDI	Open LVDS Display Interface – a formalization by National Semiconductor of de facto LVDS standards. See Appendix G for a reference to the standard. Open LDI color-mapping is the same as FPD-Link color-mapping for 18-bit displays, but is different for 24-bit displays. Open LDI color-mapping puts the least significant bits of a 24-bit display onto the 4th LVDS channel. Doing so means that an 18-bit display can operate on a 24-bit Open LDI link by using the first 3 LVDS data channels.
PCLK	Pixel clock – the clock associated with a single display pixel. For example, on a 640x480 display, there are 640 pixel clocks during the active display line period (and additional pixel clocks during the blanking periods). For a single-channel TFT display, the pixel clock is the same as the shift clock. For a dual-channel TFT display, the pixel clock is twice the frequency of the shift clock.
SCLK	Shift clock – the clock that shifts either a single pixel or a group of pixels into the display, depending on the display type. For a single-channel TFT display, the shift clock is the same as the pixel clock. For a dual-channel TFT display, the shift clock period is twice the pixel clock. For some display types, such as passive STN displays, the shift clock may be four- or eight-pixel clocks.
Single Channel	In a single-channel bit stream, a single RGB pixel is transmitted with each shift clock. The shift clock and the pixel clock are the same in this case. Single-channel LVDS streams are either 4 differential pairs (3 data pairs, 1 clock pair, for a single 18 bit stream) or 5 differential pairs (4 data pairs, 1 clock pair, for a single 24-bit stream).
Transmit Bit Order	The order, in time, in which bits are placed into the seven bit slots per LVDS frame. Bit 1 is earlier in time than bit 2, etc.
Unbalanced	Unbalanced means that the LVDS serializing hardware does not insert or manipulate bits to achieve a DC balance – i.e. an equal number of 0 and 1 bits, when averaged over multiple frames.
VSYNC	Vertical Sync – a control signal that occurs once per display frame.
Xmit Bit Order	See Transmit Bit Order.

10.3.3 LVDS Display Color Mapping Tables

LVDS display color-mappings for single- and dual-channel displays are shown in Tables 10-3 and 10-4 below.

For single-channel displays, ETXexpress Module LVDS B pairs are not used and may be left open. For single-channel, 18-bit displays, the LVDS_A3± channel is not used and may be left open.

For 18-bit, single-channel and 36-bit, dual-channel displays, the FPD-Link and Open LDI color-mappings are the same. For 24-bit, single-channel and 48-bit, dual-channel displays, mappings differ and care must be taken that the Module and display LVDS color-mappings agree.

Table 10-3: LVDS Display: Single Channel, Unbalanced Color-Mapping

	Xmit Bit Order	LVDS Clock	Open LDI 18 bit Single Ch	Open LDI 24 bit Single Ch	FPD Link 18 bit Single Ch	FPD Link 24 bit Single Ch
LVDS_A0±	1	1	G0	G2	G0	G0
	2	1	R5	R7	R5	R5
	3	0	R4	R6	R4	R4
	4	0	R3	R5	R3	R3
	5	0	R2	R4	R2	R2
	6	1	R1	R3	R1	R1
	7	1	R0	R2	R0	R0
LVDS_A1±	1	1	B1	B3	B1	B1
	2	1	B0	B2	B0	B0
	3	0	G5	G7	G5	G5
	4	0	G4	G6	G4	G4
	5	0	G3	G5	G3	G3
	6	1	G2	G4	G2	G2
	7	1	G1	G3	G1	G1
LVDS_A2±	1	1	DE	DE	DE	DE
	2	1	VSYNC	VSYNC	VSYNC	VSYNC
	3	0	HSYNC	HSYNC	HSYNC	HSYNC
	4	0	B5	B7	B5	B5
	5	0	B4	B6	B4	B4
	6	1	B3	B5	B3	B3
	7	1	B2	B4	B2	B2
LVDS_A3±	1	1				
	2	1		B1		B7
	3	0		B0		B6
	4	0		G1		G7
	5	0		G0		G6
	6	1		R1		R7
	7	1		R0		R6
LVDS_A_CK±			LCLK = PCLK / 7 SCLK = PCLK	LCLK= PCLK / 7 SCLK = PCLK	LCLK = PCLK / 7 SCLK = PCLK	LCLK = PCLK / 7 SCLK = PCLK

Table 10-4: LVDS Display: Dual Channel, Unbalanced Color-Mapping

	Xmit Bit Order	LVDS Clock	Open LDI 18 bit (36 bit) Dual Ch	Open LDI 24 bit (48 bit) Dual Ch	FPD Link 18 bit (36 bit) Dual Ch	FPD Link 24 bit (48 bit) Dual Ch
LVDS_A0±	1	1	Odd Pixel G0	Odd Pixel G2	Odd Pixel G0	Odd Pixel G0
	2	1	Odd Pixel R5	Odd Pixel R7	Odd Pixel R5	Odd Pixel R5
	3	0	Odd Pixel R4	Odd Pixel R6	Odd Pixel R4	Odd Pixel R4
	4	0	Odd Pixel R3	Odd Pixel R5	Odd Pixel R3	Odd Pixel R3
	5	0	Odd Pixel R2	Odd Pixel R4	Odd Pixel R2	Odd Pixel R2
	6	1	Odd Pixel R1	Odd Pixel R3	Odd Pixel R1	Odd Pixel R1
	7	1	Odd Pixel R0	Odd Pixel R2	Odd Pixel R0	Odd Pixel R0
LVDS_A1±	1	1	Odd Pixel B1	Odd Pixel B3	Odd Pixel B1	Odd Pixel B1
	2	1	Odd Pixel B0	Odd Pixel B2	Odd Pixel B0	Odd Pixel B0
	3	0	Odd Pixel G5	Odd Pixel G7	Odd Pixel G5	Odd Pixel G5
	4	0	Odd Pixel G4	Odd Pixel G6	Odd Pixel G4	Odd Pixel G4
	5	0	Odd Pixel G3	Odd Pixel G5	Odd Pixel G3	Odd Pixel G3
	6	1	Odd Pixel G2	Odd Pixel G4	Odd Pixel G2	Odd Pixel G2
	7	1	Odd Pixel G1	Odd Pixel G3	Odd Pixel G1	Odd Pixel G1
LVDS_A2±	1	1	DE	DE	DE	DE
	2	1	VSYNC	VSYNC	VSYNC	VSYNC
	3	0	HSYNC	HSYNC	HSYNC	HSYNC
	4	0	Odd Pixel B5	Odd Pixel B7	Odd Pixel B5	Odd Pixel B5
	5	0	Odd Pixel B4	Odd Pixel B6	Odd Pixel B4	Odd Pixel B4
	6	1	Odd Pixel B3	Odd Pixel B5	Odd Pixel B3	Odd Pixel B3
	7	1	Odd Pixel B2	Odd Pixel B4	Odd Pixel B2	Odd Pixel B2
LVDS_A3±	1	1				
	2	1		Odd Pixel B1		Odd Pixel B7
	3	0		Odd Pixel B0		Odd Pixel B6
	4	0		Odd Pixel G1		Odd Pixel G7
	5	0		Odd Pixel G0		Odd Pixel G6
	6	1		Odd Pixel R1		Odd Pixel R7
	7	1		Odd Pixel R0		Odd Pixel R6
LVDS_A_CK±			LCLK= PCLK / 14 SCLK = PCLK / 2	LCLK = PCLK / 14 SCLK = PCLK / 2	LCLK= PCLK / 14 SCLK = PCLK / 2	LCLK = PCLK / 14 SCLK = PCLK / 2
LVDS_B0±	1	1	Even Pixel G0	Even Pixel G2	Even Pixel G0	Even Pixel G0
	2	1	Even Pixel R5	Even Pixel R7	Even Pixel R5	Even Pixel R5
	3	0	Even Pixel R4	Even Pixel R6	Even Pixel R4	Even Pixel R4
	4	0	Even Pixel R3	Even Pixel R5	Even Pixel R3	Even Pixel R3
	5	0	Even Pixel R2	Even Pixel R4	Even Pixel R2	Even Pixel R2
	6	1	Even Pixel R1	Even Pixel R3	Even Pixel R1	Even Pixel R1
	7	1	Even Pixel R0	Even Pixel R2	Even Pixel R0	Even Pixel R0
LVDS_B1±	1	1	Even Pixel B1	Even Pixel B3	Even Pixel B1	Even Pixel B1
	2	1	Even Pixel B0	Even Pixel B2	Even Pixel B0	Even Pixel B0
	3	0	Even Pixel G5	Even Pixel G7	Even Pixel G5	Even Pixel G5
	4	0	Even Pixel G4	Even Pixel G6	Even Pixel G4	Even Pixel G4
	5	0	Even Pixel G3	Even Pixel G5	Even Pixel G3	Even Pixel G3
	6	1	Even Pixel G2	Even Pixel G4	Even Pixel G2	Even Pixel G2
	7	1	Even Pixel G1	Even Pixel G3	Even Pixel G1	Even Pixel G1
LVDS_B2±	1	1				
	2	1				
	3	0				
	4	0	Even Pixel B5	Even Pixel B7	Even Pixel B5	Even Pixel B5
	5	0	Even Pixel B4	Even Pixel B6	Even Pixel B4	Even Pixel B4
	6	1	Even Pixel B3	Even Pixel B5	Even Pixel B3	Even Pixel B3
	7	1	Even Pixel B2	Even Pixel B4	Even Pixel B2	Even Pixel B2
LVDS_B3±	1	1				
	2	1		Even Pixel B1		Even Pixel B7
	3	0		Even Pixel B0		Even Pixel B6
	4	0		Even Pixel G1		Even Pixel G7
	5	0		Even Pixel G0		Even Pixel G6
	6	1		Even Pixel R1		Even Pixel R7
	7	1		Even Pixel R0		Even Pixel R6
LVDS_B_CK±			LCLK= PCLK / 14 SCLK = PCLK / 2	LCLK = PCLK / 14 SCLK = PCLK / 2	LCLK= PCLK / 14 SCLK = PCLK / 2	LCLK = PCLK / 14 SCLK = PCLK / 2

10.4 LVDS – Reference Schematics

Reference schematics are presented below for 18-bit single-channel, 24-bit single-channel, and 48-bit dual-channel LVDS receivers. The examples are meant for illustration only. Often the LVDS receivers are integrated onto the panel electronics. If so, the panel is usually referred to as an LVDS panel. The panel documentation may describe the LVDS de-serializer circuit in detail, or it may just show the bit packing scheme expected by the display. If the LVDS receiver is not integrated into the display, the display is referred to as a parallel-input display.

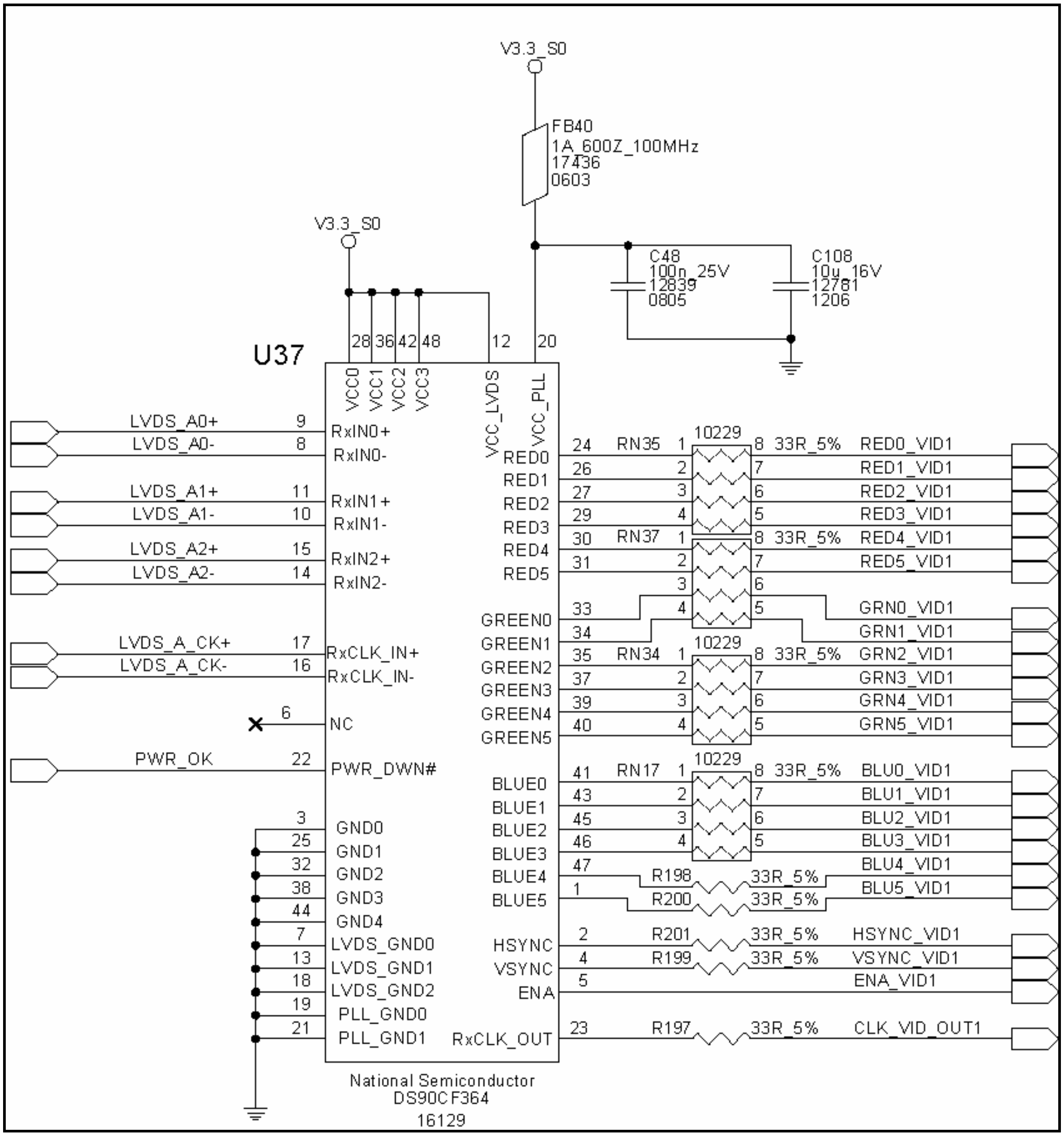
Alternatively, the de-serializers may be implemented on small LVDS receiver boards, such as the Kontron JILI boards (Section 10.5, below) that are mounted on or close to a parallel input flat panel display.

For 24-bit single-channel displays and 48-bit dual-channel displays, make sure that the Module LVDS color-mapping scheme matches the display's LVDS color-mapping.

10.4.1 LVDS Single Channel 18-bit Receiver

A National DS90CF364 +3.3V LVDS 65MHz receiver chip is shown. The chip de-serializes three differential data streams and differential clock stream to 18 bits of RGB data and 3 bits of LCD timing and control CMOS/TTL outputs.

Figure 10-1: LVDS 18-bit Receiver Schematic



These notes refer to Figure 10-1 above.

- LVDS_A0+/- thru LVDS_A2+/- are sourced from ETXexpress Module pins and drive Receiver input pins RxIN0+/- thru RxIN2+/- respectively. They serve as the data source for RGB output.

- LVDS_A_CK+/- are sourced from ETXexpress Module pins and drive Clock input pins RxCLK+/- respectively. They serve as the timing and control source for the Receiver.

- LVDS signals that are listed are terminated with 100Ω resistors across each pair that are close to the device.

- The receiver PWR_DWN# pin is connected to the system PWR_OK net in this example. PWR_DWN# could alternatively be driven by a GPO pin to allow software to control this function.

- RED0 thru RED5 pins output the color Red RGB signal that is shown and are terminated in series with 33Ω resistors that are interconnected to the appropriate flat-panel connector.

- GRN0 thru GRN5 pins output the color Green RGB signal that is shown and are terminated in series with 33Ω resistors that are interconnected to the appropriate flat-panel connector.

- BLU0 thru BLU5 pins output the color Blue RGB signal that is shown and are terminated in series with 33Ω resistors that are interconnected to the appropriate flat-panel connector.

- HSYNC pin output for Horizontal Sync that is shown is terminated in series with 33Ω resistors that are interconnected to the appropriate flat-panel connector.

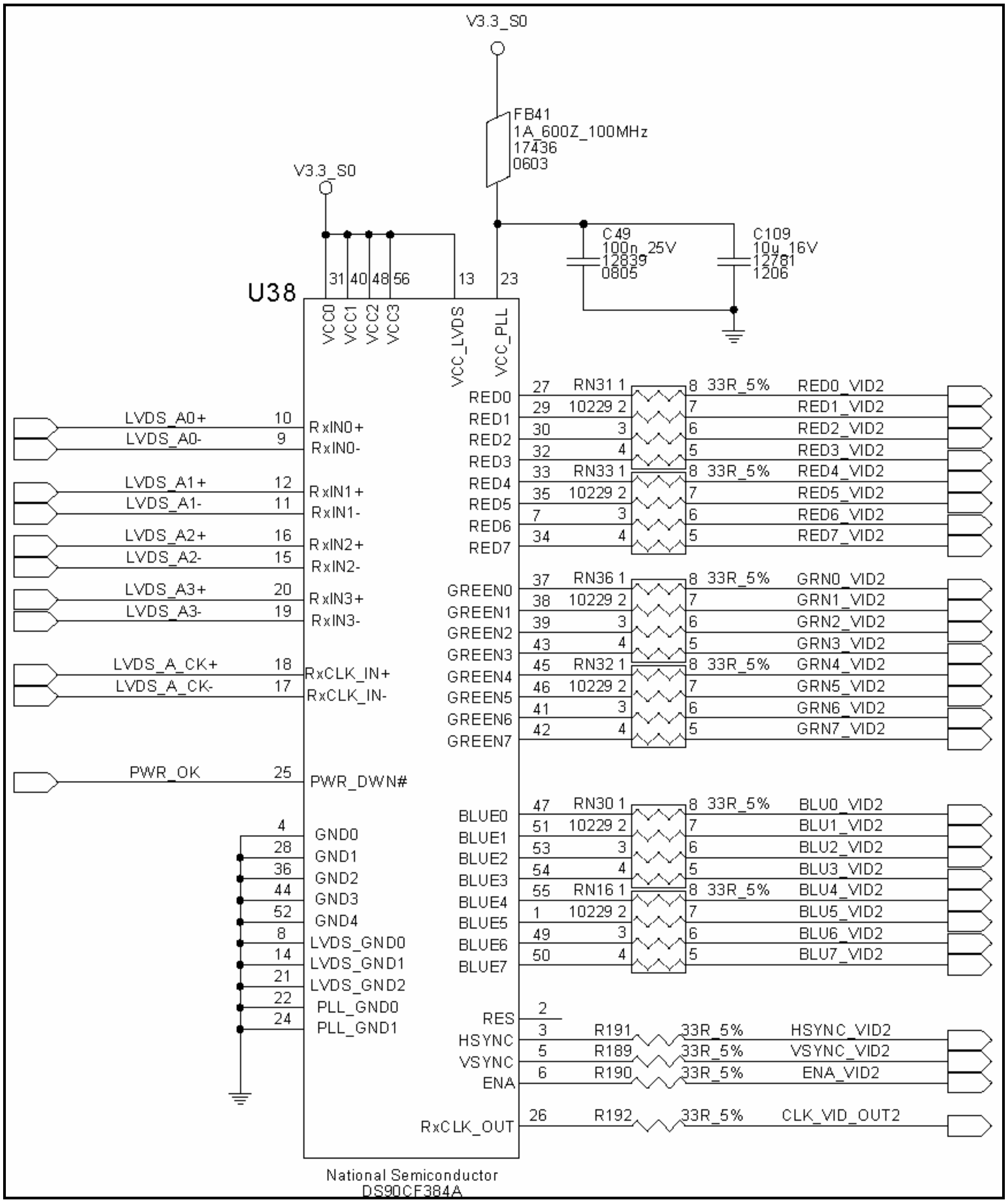
- VSYNC pin output for Vertical Sync that is shown terminated in series with 33Ω resistors that are interconnected to the appropriate flat-panel connector.

- ENA pin output for Data Enable that is shown is terminated in series with 33Ω resistors that are interconnected to the appropriate flat-panel connector.

- RxCLK_OUT pin output for the Clock Output that is shown is terminated in series with 33Ω resistors that are interconnected to the appropriate flat-panel connector.

10.4.2 LVDS 24-bit Receiver

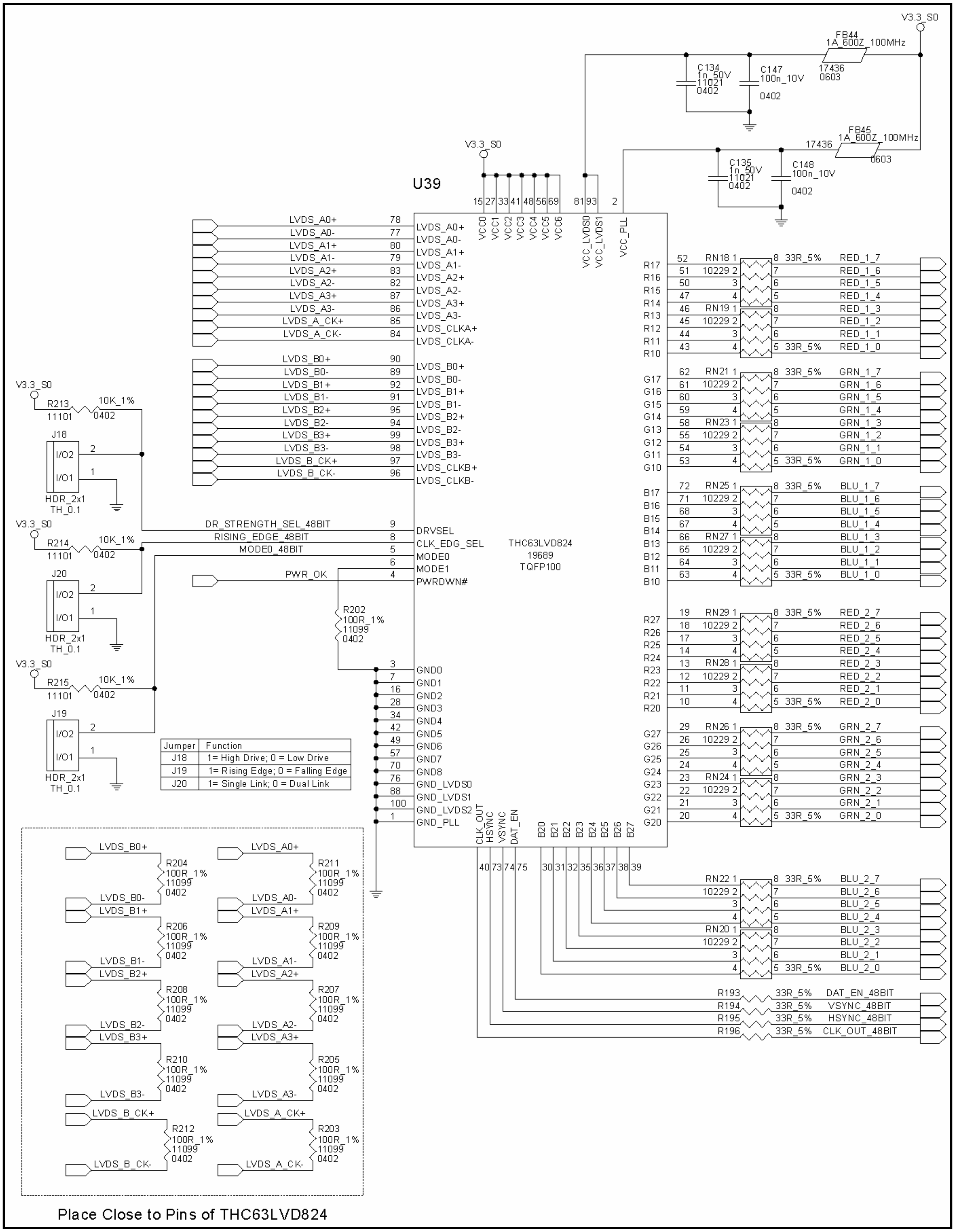
Figure 10-2: LVDS to 24-bit Receiver Schematic



The National DS90CF384A output-pin labels, as shown above, assume that the source transmitter uses FPD color-mapping. This circuit could be used with an Open LDI source, but the color bits from the DS90CF384A would have to be re-arranged. Net RED0_VID2 (Open LDI R0) would tie (through a series terminator, if desired) to chip pin 7 (FPD-Link R6); net RED1_VID2 (Open LDI R1) to chip pin 34 (FPD-Link R7); net RED2_VID2 (Open LDI R2) to chip pin 27 (FPD-Link R0), etc., per the 24 bit Open LDI and FPD-Link columns in Table 10-3 above.

10.4.3 LVDS 48-bit Receiver (Dual 24 bit)

Figure 10-3: LVDS to 48-bit Receiver Schematic



Jumper	Function
J18	1= High Drive; 0 = Low Drive
J19	1= Rising Edge; 0 = Falling Edge
J20	1= Single Link; 0 = Dual Link

These notes apply to Figure 10-3 above.

- The Thine THC63LVD824 de-serializes the data to drive a 48-bit, flat-panel display.
- This devices assumes that the source stream uses Open LDI color-mapping.
- LVDS_A0+/- thru LVDS_A3+/- are sourced from ETXexpress Module pins and drive Receiver Input pins LVDS_A0+/- thru LVDS_A3+/- respectively. They are the data source for RGB1 (odd pixel) outputs.
- LVDS_A_CK+/- are sourced from ETXexpress Module pins and drive Clock Input pins LVDS_CLKA+/- respectively. They are the timing and control source for the Receiver.
- LVDS_B0+/- thru LVDS_B3+/- are sourced from ETXexpress Module pins and drive Receiver Input pins LVDS_B0+/- thru LVDS_B3+/- respectively. They are the data source for RGB2 (even pixel) outputs.
- LVDS_B_CK+/- are sourced from ETXexpress Module pins and drive Clock Input pins LVDS_CLKB+/- respectively. They are the timing and control source for the Receiver.
- The LVDS_A and _B clocks are two copies of the same clock.
- The LVDS signals are terminated with 100Ω resistors across each pair. The termination should be close to the receiver pins (within a few inches).
- DRVSEL may be pulled low to reduce the output signal drive strength and reduce EMI.
- CLK_EDGE _SEL is pulled high for the Rising Edge Output clock Triggering Edge or low for Falling Edge; Figure 10-3 above shows a jumper-select implementation set to select either.
- The MODE0 pin on the Thine device should be low for dual channel LVDS operation. The device also can operate in a single-channel mode. In this case the LVDS_B input stream is not used, and the RGB2 outputs are not used.
- The receiver PWR_DWN# pin is connected to the system PWR_OK net in this example. PWR_DWN# could alternatively be driven by a GPO pin to allow software to control this function.

10.5 JILI – Non-Native LVDS Display – Reference Schematics

JILI (Jumptec Intelligent LVDS Interface) is a Kontron hardware and software standard that interfaces the host computer system via LVDS to flat-panel displays. Target displays are usually medium- to high-resolution TFT displays with parallel (CMOS, non-LVDS) interfaces.
A link to the Kontron JILI Specification can be found in Appendix G.

A JILI implementation consists of some or all of the following components:

- A 40-pin, flat-foil connector (FFC) on the Carrier Board pinned out per the JILI Specification. The 40-pin connector includes serialized LVDS display information, an I^2C link, +5V power for the display electronics, +12V power for the display backlight inverter, and a control line for the display backlight.

- A flat-foil ribbon cable.

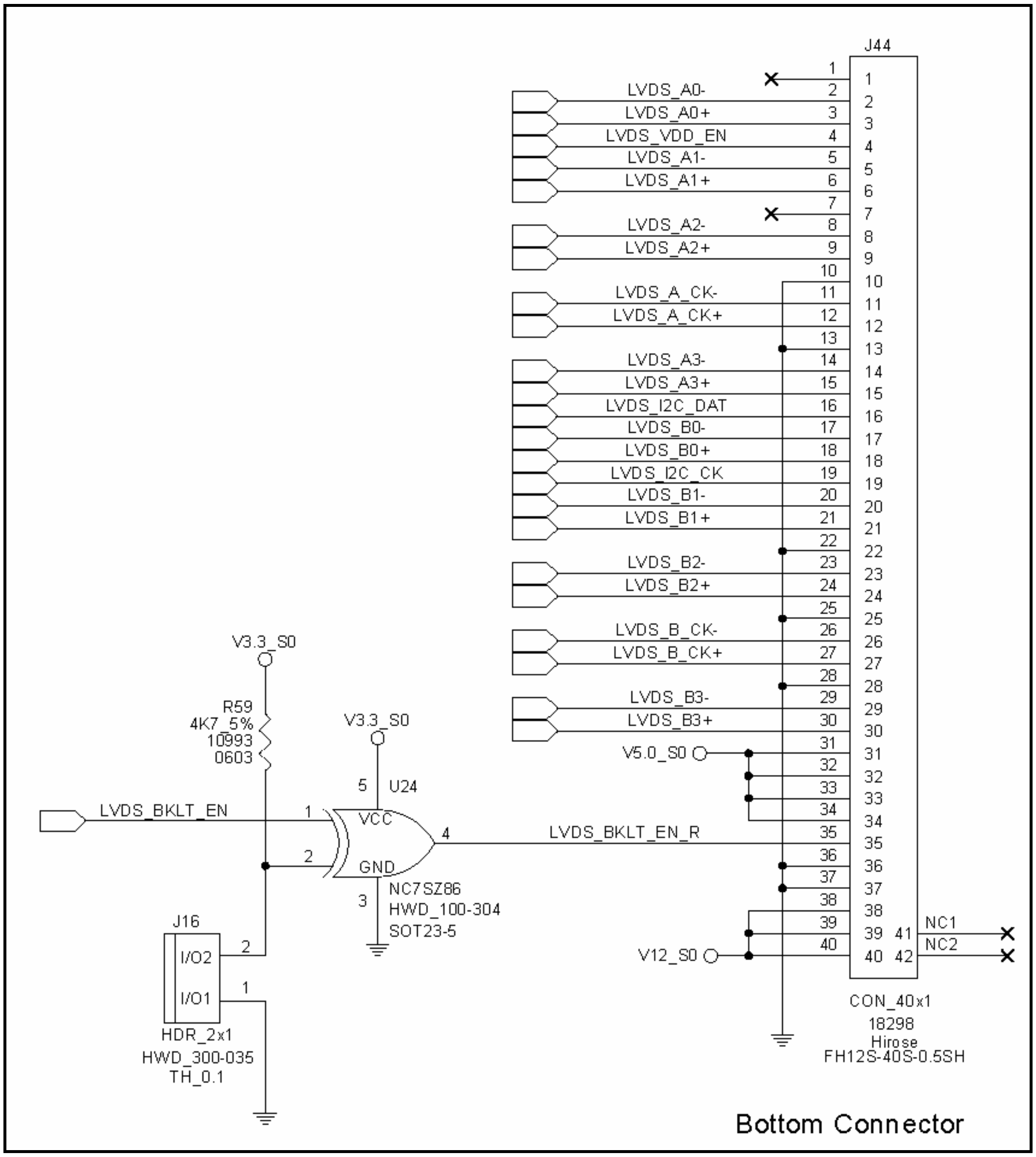
- A small JILI receiver board that includes a mating 40-pin, flat-foil connector, an LVDS receiver, termination resistors and a few related circuit components, an EEPROM loaded with a JILI-compliant data structure describing the target display characteristics, and an output connector that mates with the target display's connector. JILI receiver boards are designed to mate either directly to the target display connector or to be mounted on the target display with a short mating cable.

- A JILI-aware BIOS.

The JILI-aware BIOS queries the JILI receiver board EEPROM via the LVDS_I2C link and sets up the Module's graphics controller appropriately.

In some situations, the JILI hardware forms the physical connection but the JILI software component is not used. The display parameters may be hard-coded into the module BIOS or selected form a table in the BIOS setup screen.

Figure 10-4: JILI Connector Schematic – Carrier Board Connector



The following notes apply to the JILI Connector shown in Figure 10-4 above.

- The connector used is a 40-pin, flat-foil connector, high-density, 0.5mm-pitch connector (Hirose FH12S-40S-0.5SH). FFC (Flat Foil Cable) connectors come in “top-mount” and “bottom-mount” versions. The “top” and “bottom” refer to whether the exposed part of the flat-foil cable are up or down when inserting the cable. The pin-outs reverse for the two cases. In general, they can be quite confusing. Trace the entire signal path thru the various connectors in the system to ensure that you obtain the expected connectivity. “Top mount” and “bottom mount” do not refer to which side of the PCB is being used but rather how the FFC is inserted into the FFC connector.

- There are two construction styles of flexible flat-foil cables: “opposite-side” and “same-side” termination. An “opposite-side” cable has conductors at the two ends of the cable exposed on opposite sides of the cable. If an “opposite-side” FFC is used with a pair of “top-mount” connectors, or with a pair of “bottom-mount” connectors, then the pin numbering on the two ends is preserved. If a “same-side” FFC is used with a pair of “top-mount” FFC connectors, the pin numbering reverses at the two ends (i.e. for a 40-pin FFC, pin 1 maps to pin 40, pin 2 to pin 39, etc.). See the Kontron JILI Version 2.0 Specification for an illustration of an “opposite-side” FFC.

- LVDS_VDD_EN from the ETXexpress Module controls power to the panel.

- LVDS_A0+/- thru LVDS_A3+/- are sourced from ETXexpress Module pins and drive JILI Connector pins.

- LVDS_A_CK+/- are sourced from ETXexpress Module pins and drive JILI Connector pins.

- LVDS_B0+/- thru LVDS_B3+/- are sourced from ETXexpress Module pins and drive JILI Connector pins.

- LVDS_B_CK+/- are sourced from ETXexpress Module pins and drive JILI Connector pins.

- LVDS_I2C_DAT and LVDS_I2C_CK are sourced from the ETXexpress Module and drive the JILI Connector pins for I^2C interface.

- LVDS_BKLT_EN from the ETXexpress Module controls the panel-backlight enable/disable.

    - The jumper implementation shown in Figure 10-4 above with the EX-OR gate allows for polarity inversion of this signal. Experience has shown this to be a worthwhile option.

    - If the jumper is installed, the backlight control signal is not inverted. If the jumper is open, the signal is inverted.

10.6 EDID and Native LVDS Displays

10.6.1 EDID and E-EDID

Many contemporary panels incorporate an I^2C-accessible EEPROM that stores a VESA EDID (Video Electronics Standards Association Extended Display Identification Data) or VESA E-EDID (Enhanced EDID) data structure. This data structure fully describes the display parameters and capabilities to the host system. To take advantage of this, the ETXexpress Module's BIOS needs to incorporate EDID or E-EDID support. Check the relevant ETXexpress Module User Guide.

EDID and E-EDID are similar in concept to the software aspect of the Kontron JILI EEPROM, but EDID is broader in scope and is a broader-based standard. EDID and E-EDID are not limited to LVDS displays or flat panels.

10.6.2 Native LVDS Displays

A "native LVDS" display is a display that incorporates a LVDS receiver into the display electronics. To use a native LVDS display with your Carrier Board design, note the following:

- Check the display and Module documentation for the LVDS color-mapping that each uses. For 18-bit or dual 18-bit (also known as 36-bit) panels, there should not be an issue but for 24-bit and dual 24-bit (48-bit) panels, there is a difference.
- If the Module supports the display resolution and the color-mapping used, then all that should be needed on the Carrier Board to support the display is a connector on the Carrier Board that allows easy connection to the display. If the display uses an FFC connector, then often the solution is an FFC connector of the same type mounted on the Carrier Board. The LVDS signals listed in Table 10-1 above are brought to the appropriate connector pins.
- See the notes below Figure 10-4 above in Section 10.5 for a discussion of some FFC connector and cable pitfalls.
- The cabling system between the Carrier Board and the display should have a 100-ohm differential impedance for signal pairs.
- The differential pairs should be terminated with 100 ohms (or whatever the pair's differential impedance value is) across the pairs. Check panel documentation to see if this termination is included on the panel.

11 IDE / LAN 1 and 2

11.1 IDE / LAN 1 and 2 – Signal Definitions

Per the COM Express™ Specification, a set of pins on the Module C-D connectors may be used for an IDE port or a pair of LAN ports, depending on the Module Type.

- For Module Types 2 and 4, IDE support is required; LAN 1 and 2 are not available. The IDE (PATA) signals support up to 2 devices in a master/slave configuration.
- For Module Types 3 and 5, LAN 1 and 2 are optionally available; IDE is unavailable.

Table 11-1: IDE (PATA) and LAN 1 and 2 Pin-outs

Pin	IDE (Mod. Types 2,4)	LAN 1 and 2 Mod. Types 3,5		Pin	IDE Mod. Types 2,4	LAN 1 and 2 Mod. Types 3,5
C1	GND (FIXED)			D1	GND (FIXED)	
C2	IDE_D7	GBE1_ACT#		D2	IDE_D5	GBE2_ACT#
C3	IDE_D6	GBE1_MDI3-		D3	IDE_D10	GBE2_MDI3-
C4	IDE_D3	GBE1_MDI3+		D4	IDE_D11	GBE2_MDI3+
C5	IDE_D15	GBE1_LINK100#		D5	IDE_D12	GBE2_LINK100#
C6	IDE_D8	GBE1_MDI2-		D6	IDE_D4	GBE2_MDI2-
C7	IDE_D9	GBE1_MDI2+		D7	IDE_D0	GBE2_MDI2+
C8	IDE_D2	GBE1_LINK1000#		D8	IDE_REQ	GBE2_LINK1000#
C9	IDE_D13	GBE1_MDI1-		D9	IDE_IOW#	GBE2_MDI1-
C10	IDE_D1	GBE1_MDI1+		D10	IDE_ACK#	GBE2_MDI1+
C11	GND (FIXED)			D11	GND (FIXED)	
C12	IDE_D14	GBE1_MDI0-		D12	IDE_IRQ	GBE2_MDI0-
C13	IDE_IORDY	GBE1_MDI0+		D13	IDE_A0	GBE2_MDI0+
C14	IDE_IOR#	GBE1_LINK#		D14	IDE_A1	GBE2_LINK#
				D15	IDE_A2	GBE2_CTREF
				D16	IDE_CS1#	RSVD
				D17	IDE_CS3#	RSVD
				D18	IDE_RESET#	RSVD
				D77	IDE_CBLID#	RSVD

11.2 IDE / LAN 1 and 2 – Routing Considerations

11.2.1 IDE

The IDE signals are single-ended signals with a nominal impedance of 55 ohms.
See the IDE (PATA) section in Appendix B for Trace Routing Parameters and Guidelines.

11.2.2 *LAN 1 and 2*

Routing considerations for LAN 1 and 2 are the same as those for LAN 0, described in Section 7.3 above, and in Appendix A. Please refer to those sections.

11.3 IDE (PATA) – Reference Schematics

11.3.1 IDE 40-Pin Header (3.5 Inch Drives)

A diagram illustrating connections from the Module connector to a 0.1-inch pitch, two-row, 40-pin header suitable for use with standard 3.5-inch parallel ATA drives is shown in Figure 11-1 below. All off-page connections in this diagram are routed directly to the Module pins. No pull-ups or other termination are required.

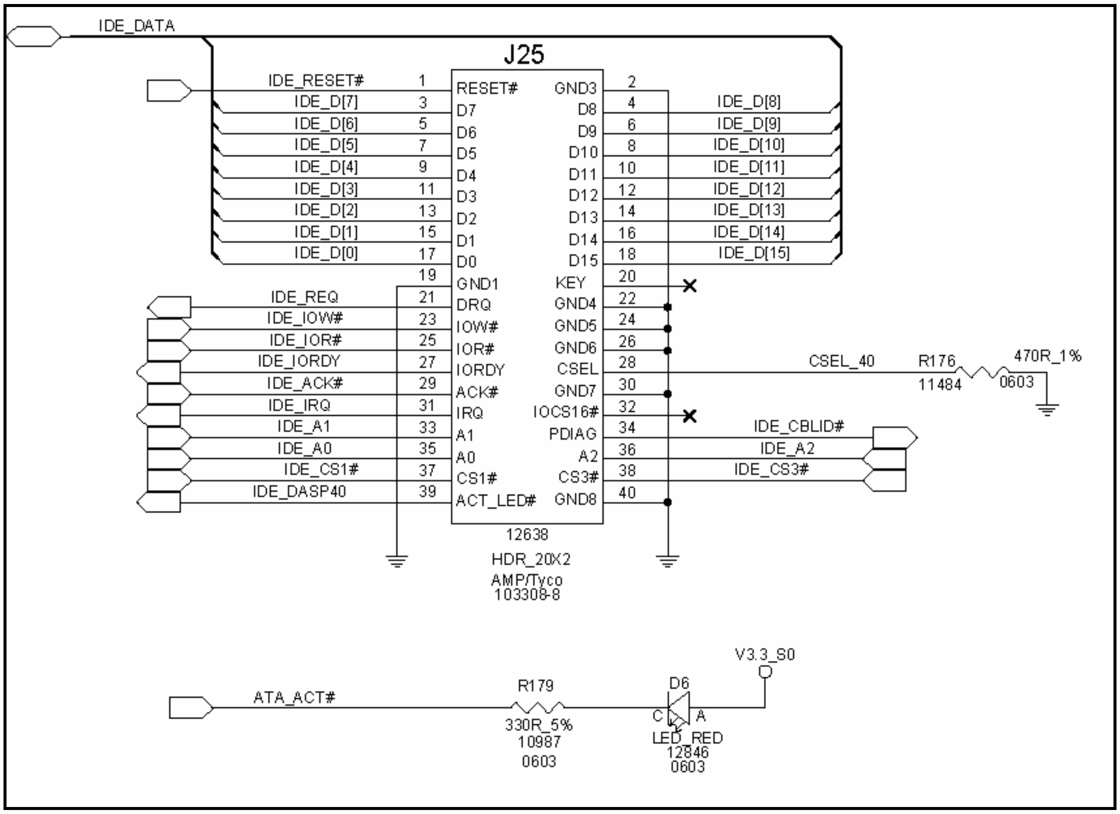
Power to the parallel ATA drive is handled on a separate 4-pin connector and is not shown here.

The 40-pin IDE header is used with a 40-pin, 0.5-inch pitch, flat cable for slower drives.
An industry standard 80-pin, 0.25-inch pitch cable is used for Ultra-DMA 66 and 100 drives.
The cable assemblies have sockets with 40 positions that mate with the header shown in Figure 11-1 and with the corresponding connector on the parallel ATA drive. The extra 40 conductors on the 80-conductor cable are tied to GND isolate the adjacent signals for improved signal integrity. The 80-pin cable assembly also ties pin 34 on the 40-pin header (net IDE_CBLID# in Figure 11-1) to GND. If IDE_CBLID# is sampled low by the Module BIOS, it assumes that the proper high- speed cable is in place and sets up the drive parameters accordingly.

Jumper settings on the hard drives determine Master / Slave configuration.

The drive activity LED shown is driven by Module pin A28 (COM Express pin ATA_ACT#).

Figure 11-1: IDE 40-Pin Schematic

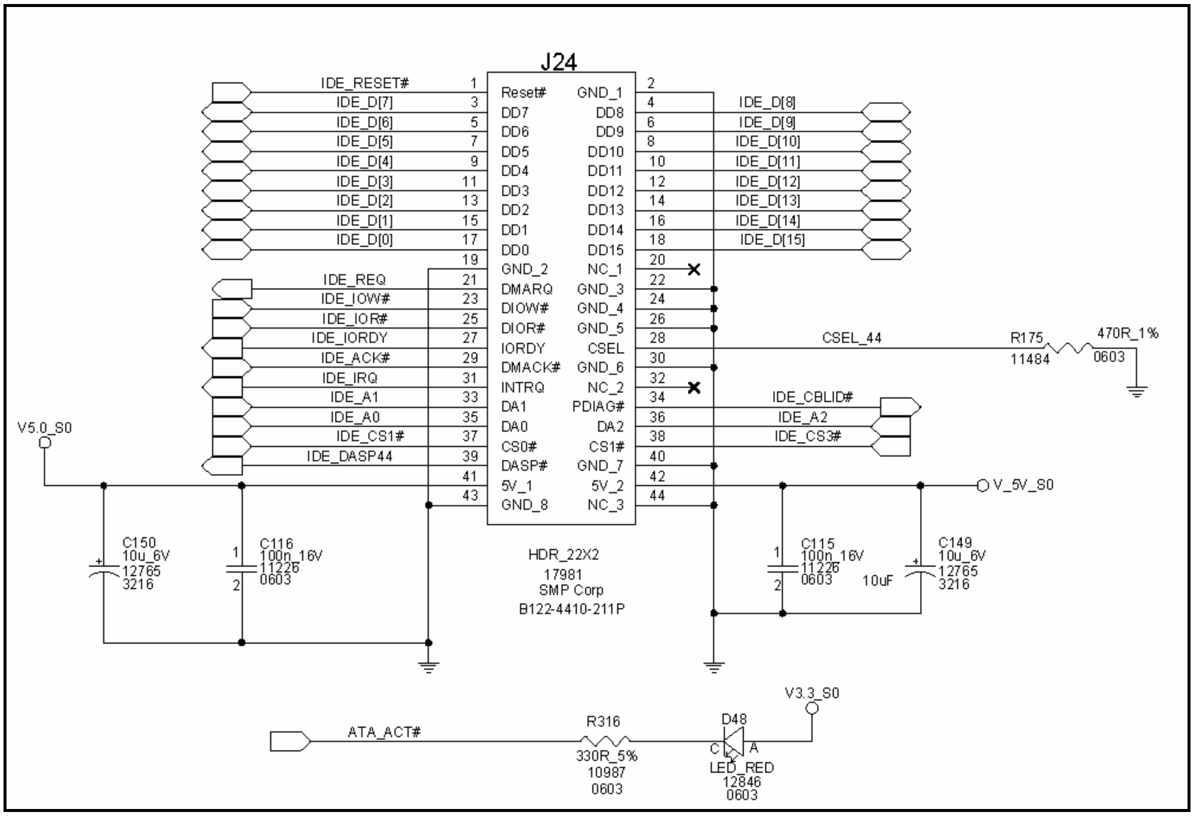


11.3.2 IDE 44 Pin Header (2.5 Inch Drives)

Figure 11.2 below shows a 44-pin, 2mm-pitch header used for 2.5"-IDE hard drives in laptops. The cabling used is a 44-pin, 1mm-pitch, flat-ribbon cable. Power to the drive is supplied over the 44-pin cable on Conductors 41 and 42.

The drive-activity LED shown is driven by Module pin A28 (COM Express pin ATA_ACT#).

Figure 11-2: IDE 44 Pin Schematic



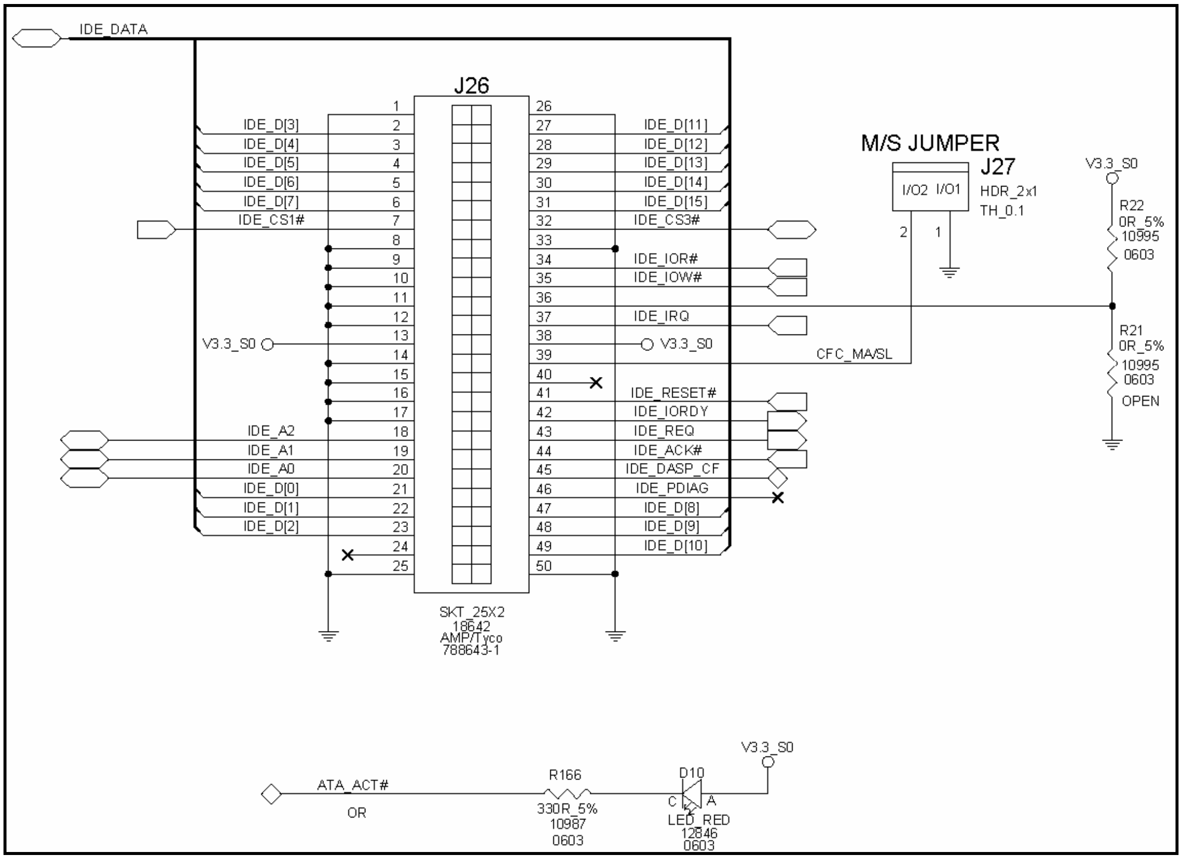
11.3.3 50-Pin Compact Flash Header

Figure 11.3 below shows a socket implementation for a Compact Flash.

Socket pin 39, net CFC_MA/SL, is connected to a jumper to select Master or Slave configuration. If jumpered low, the drive is configured for Master mode. This allows a Compact Flash boot.
A Compact Flash boot also can be toggled under software control via a GPIO pin.

The drive activity LED shown is driven by Module pin A28 (COM Express pin ATA_ACT#).

Figure 11-3: Compact Flash Schematic



12 VGA

12.1 VGA – Signal Definitions

Pins for an analog VGA interface are defined in the COM Express™ Specification for all Module Types. Implementation of the VGA interface is optional. The VGA interface consists of three analog color signals (Red, Green, Blue); digital Horizontal and Vertical Sync signals, and I^2C for DDC (Display Data Control) implementation.

Table 12-1: VGA Pin-outs

Row B	
B89	VGA_RED
B90	GND (FIXED)
B91	VGA_GRN
B92	VGA_BLU
B93	VGA_HSYNC
B94	VGA_VSYNC
B95	VGA_I2C_CK
B96	VGA_I2C_DAT

12.2 VGA – Routing Considerations

Route the three analog VGA signals (VGA_RED, VGA_GRN, VGA_BLU) and the two sync signals (VGA_HSYNC and VGA_VSYNC) as single-ended signals with a trace impedance of 75Ω.

The three analog color signals should be back-terminated to ground thru 150 ohms. The signals should be given generous spacing to each other and to other signal groups. Shorter routes are preferred, although longer routes can work if carefully done. Reference the signals to a continuous, low-noise ground plane.

A schematic example is given in Section 12.3 below. Place the shown termination resistors, ESD- and EMI-suppression components, close to the external DB15 connector.

See the VGA section in Appendix B for additional Trace Routing Parameters and Guidelines.

The VGA_I2C signals may be routed as general digital signals with a nominal 55Ω single-ended impedance.

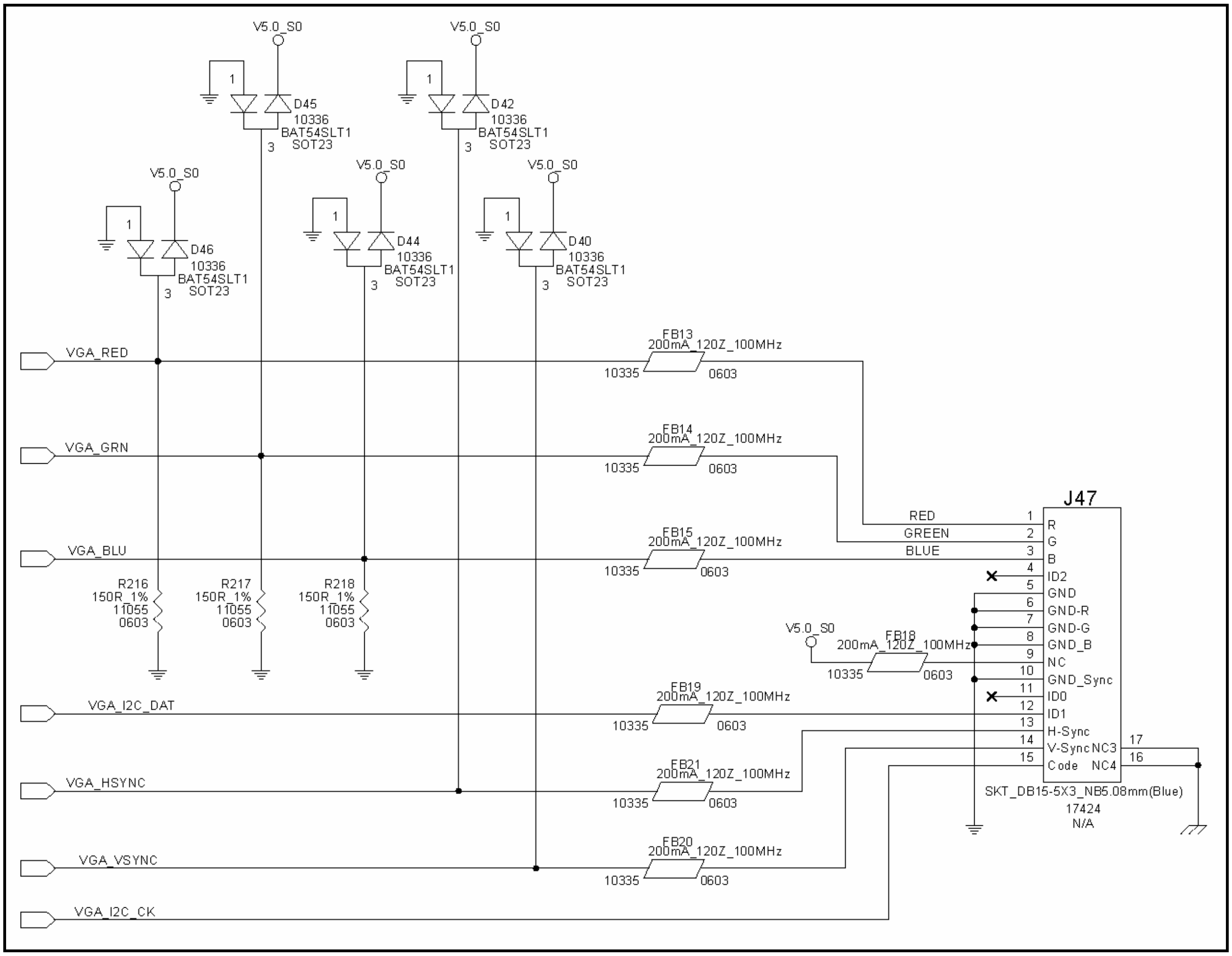
12.3 VGA – Reference Schematics

A schematic example of a VGA connector implementation is shown in Figure 12-1 below.

All signals along the left edge of Figure 12-1 are sourced directly from the ETXexpress Module. No additional pull-ups or terminations beyond what is shown in the figure are required.

- Analog signals VGA_RED, VGA_GRN, VGA_BLU are back-terminated to 150Ω resistors to ground.
- Analog signals VGA_RED, VGA_GRN, VGA_BLU are connected to the DB15 VGA connector thru ferrite beads to suppress radiated noise.
- The dual Schottky diodes shown provide ESD protection and should have a low C rating (~5pf max) and small leakage (~10μA).
- The dual Schottky diodes are clamped to +5V and ground in this figure. They could alternatively be clamped between +3V and ground.
- The VGA_HSYNC, VGA_VSYnc, and VGA_I2C signals also are connected to the DB15 connector thru ferrite beads to suppress radiated noise.
- The connector used is a right angle high density DB15 receptacle.
  A suitable part is AMP/Tyco part number 1-11076-4.

Figure 12-1: Analog VGA Connector Schematic



13 TV-Out

13.1 TV-Out – Signal Definitions

Three pins on the COM Express A-B connector are defined for an analog TV-Out interface. TV-Out implementation is optionally available on all Module Types. Three video modes are allowed:

- Composite Video – all color, brightness, blanking, and sync information are encoded onto a single signal.
- S-Video - Separated Video - video signal with two components – brightness (luma) and color (chroma). This is also known as Y-C video.
- Component Video – a video signal that consists of three components. The components may be RGB, or may be encoded using other three component encoding schemes such as YUV, YCbCr, and YPbPr.

An ETXexpress Module may support all, some, or none of these modes. Within the modes, there are different encoding schemes such as Composite Video, which can be in NTSC or PAL format, and may be Module-dependent.

The COM Express TV-Out pins consist of three analog signals: TV_DAC_A, TV_DAC_B, and TV_DAC_C, which are detailed in Table 13-1 below.

Table 13-1: TV-Out Pin-outs

Module Pin Number	Module Pin Name	Composite Video	S-Video	Component Video
B97	TV_DAC_A	CVBS	Unused	Pb
B98	TV_DAC_B	Unused	Luminance	Y
B99	TV_DAC_C	Unused	Chrominance	Pr

13.2 TV_Out – Routing Considerations

Route the three analog TV-Out signals (TV_DAC_A, TV_DAC_B, and TV_DAC_C) as single- ended signals with a trace impedance of 75Ω. Back-terminate the three signals to ground thru 150 ohms. The signals should be given generous spacing to each other and to other signal groups. Shorter routes are preferred although longer routes can work if carefully done. Reference the signals to a continuous, low-noise ground plane.

A schematic example is given in Section 13.3 below. Place the shown termination resistors, ESD and EMI suppression components, close to external connectors.

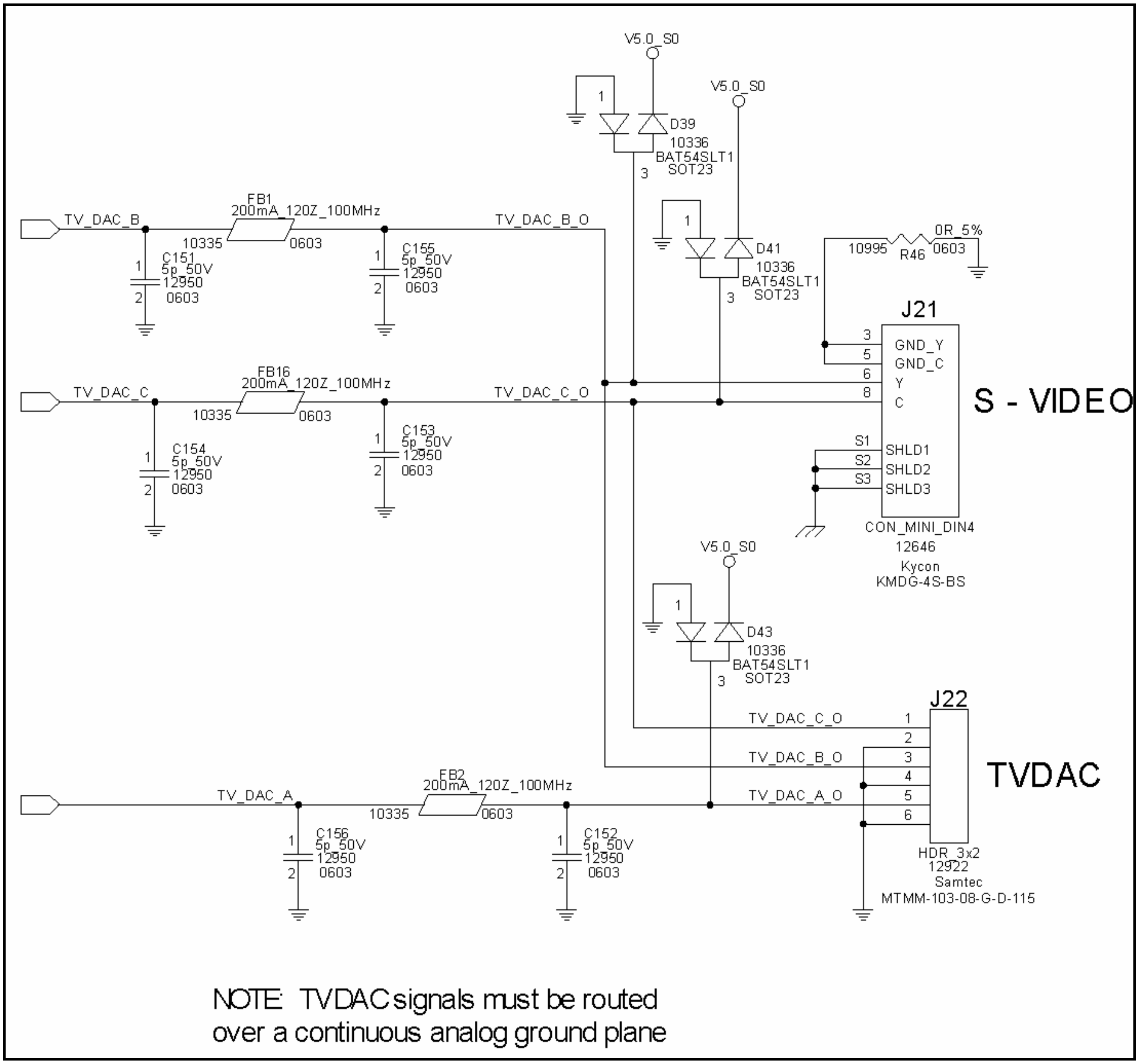
See the TV-Out section in Appendix B for additional Trace Routing Parameters and Guidelines.

13.3 TV-Out – Reference Schematics

A schematic example of a mini-DIN S-Video and Component Video implementation is shown in Figure 13-1 below. All signals along the left edge of the figure are sourced directly from the ETXexpress Module. No additional pull-ups or terminations beyond what is shown in the figure are required. The TV_DAC signals are terminated thru 150 ohms to ground on the ETXexpress Module.

- The TV_DAC_ signals are routed thru pi-filters (cap-ferrite-cap) to suppress radiated noise. The suggested capacitor and ferrite values are shown in the figure.
- The dual Schottky diodes shown provide ESD protection and should have a low C rating (~5pf max) and small leakage (~10μA).
- The dual Schottky diodes are clamped to +5V and ground in this figure. They could alternatively be clamped between +3V and ground.
- Place all components shown in Figure 13-1 below in close proximity to each other. Minimize the stubs formed by the two-connector implementation.

Figure 13-1: TV-OUT, S-Video and Component Video Connectors Schematic



14 Digital Audio Interface: AC'97 and HD Audio

14.1 AC'97 and HD Audio – Signal Definitions

The COM Express™ Specification allocates seven pins on the A-B connector to support digital AC'97 and HD interfaces to audio Codecs on the Carrier Board. The pins are available on all Module types. High-definition (HD) audio uses the same digital-signal interface as AC '97 audio. Codecs for AC '97 and HD Audio are different.

Table 14-1: AC'97 Pin-outs

Row A			Row B	
A28			B28	AC_SDIN2
A29	AC_SYNC		B29	AC_SDIN1
A30	AC_RST#		B30	AC_SDIN0
A31	GND (FIXED)		B31	GND (FIXED)
A32	AC_BITCLK		B32	
A33	AC_SDOUT		B33	

14.2 AC'97 – Routing Considerations

- The AC_ signal set is comprised of single-ended signals that have a nominal trace impedance of 55Ω.
- Route AC_ signals in a point-to-point fashion above a continuously quiet reference plane.
- Create separate Analog and Digital Ground Planes and split them across the Codec. Tie the Analog Ground to Digital Ground at a single point.
- Partition the design to group Analog parts as one group and Digital parts as another group.
- Route Analog and Digital signals as far apart as possible.
- Keep the Clock as far away as possible from analog input and voltage-reference pins.
- Use metal film resistors.
- Fill the region between the Analog signals with copper and tie it to Analog Ground.
- Fill the region between the Digital signals with copper and tie it to Digital Ground.
- Locate the Crystal or Oscillator close to Codec.
- Place the Codec in the quietest part of the Carrier Board – away from significant current paths or ground bounce.
- See application notes from the Codec vendor for other useful information.
- See additional routing constraints in Appendix B.

14.3 AC ’97 – Reference Schematics

A sample AC ’97 CODEC circuit that uses the Cirrus Logic CS4299 is given in Figures 14-1 thru 14-5 below.

- The ETXexpress Module provides AC ’97 interface support for up to 3 Codecs via AC_SDIN[0:2]. The rest of the signals are common to each Codec.
- The Codec BIT_CLK output goes to the ETXexpress Module pin A32 AC_BTCLK.
  - A 12.288MHz clock is sourced from the primary Codec.
  - This clock drives additional Codecs in multiple Codec applications.
  - The clock facilitates serial synchronous communication between the ETXexpress Module and the Codecs.
- The Codec SDATA_OUT input is sourced by ETXexpress module pin A33 AC_SDOUT.
  - This line carries control information and the output data stream for the digital audio.
  - The signal is connected to additional Codecs in multiple Codec applications.
- The Codec SDATA_IN output drives ETXexpress Module pin A30 AC_SDIN0.
  - Status information and input streams for the digital audio go to the ETXexpress Module.
  - Additional Codecs are interconnected using separate lines AC_SDIN[1:2] in multiple Codec applications.
- The Codec SYNC input is sourced by ETXexpress Module pin A29 AC_SYNC.
  - The timing signal comes from the ETXexpress Module.
  - The signal is connected to additional Codecs in multiple Codec applications.
- The Codec RESET# input is sourced by ETXexpress Module pin A30 AC_RST#.
  - The signal is connected to additional Codecs in multiple Codec applications.
- The Codec signals LINE_OUT_L and LINE_OUT_R are stereo outputs that are AC-coupled to an audio amplifier. The AC-coupling is shown with the amplifier in Figure 14-2 below. The amplifier shown is a 6W amplifier with AC-coupled outputs. Power-audio amplifiers such as this one need substantial heat-sinking.
- MIC1 is an analog input that is sourced from a jack that uses AC-coupling. See Figures 14-1 and 14-3. Note the use of microphone-biasing.
- LINE_IN_L and LINE_IN_R are stereo inputs that are sourced from a phono jack that uses AC-coupling. See Figures 14-1 and 14-4.
- CD_L and CD_R are stereo inputs that are sourced from an external connector using AC-coupling. See Figure 14-1.
- The Codec S/PDIF_OUT (Sony/Philips Digital Interface) output signal can be connected to drive external audio equipment.

Figure 14-1: AC'97 Codec Schematic

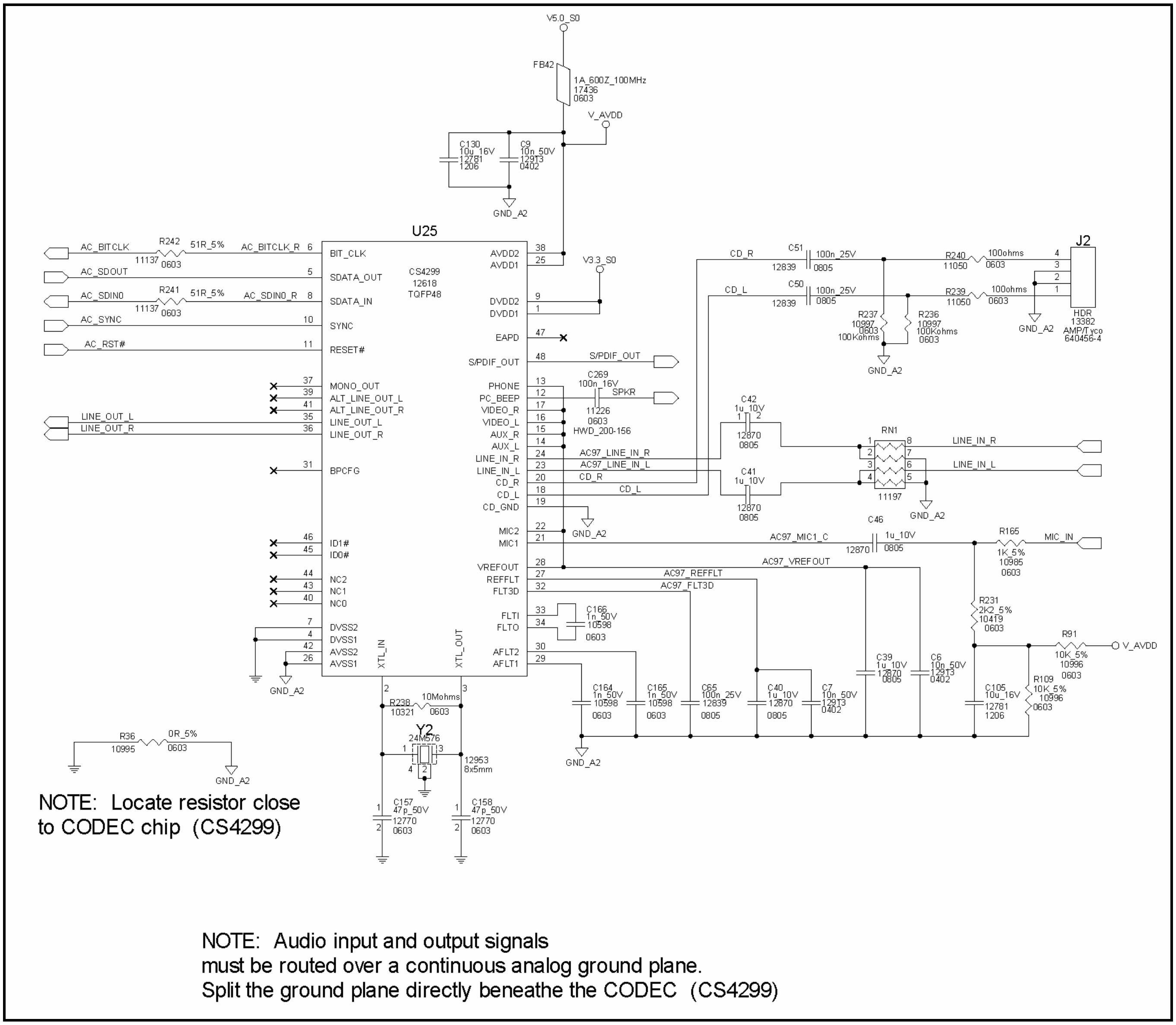


Figure 14-2: Audio-Amplifier Schematic

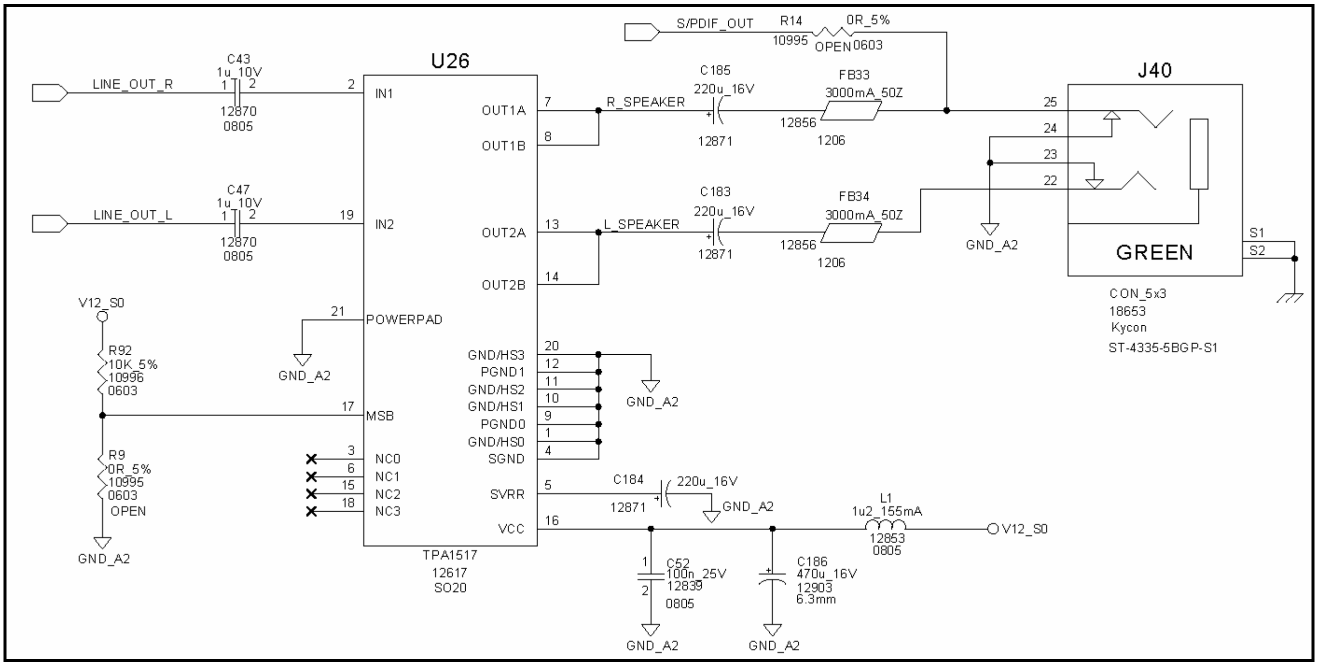


Figure 14-3: Microphone-Input Schematic

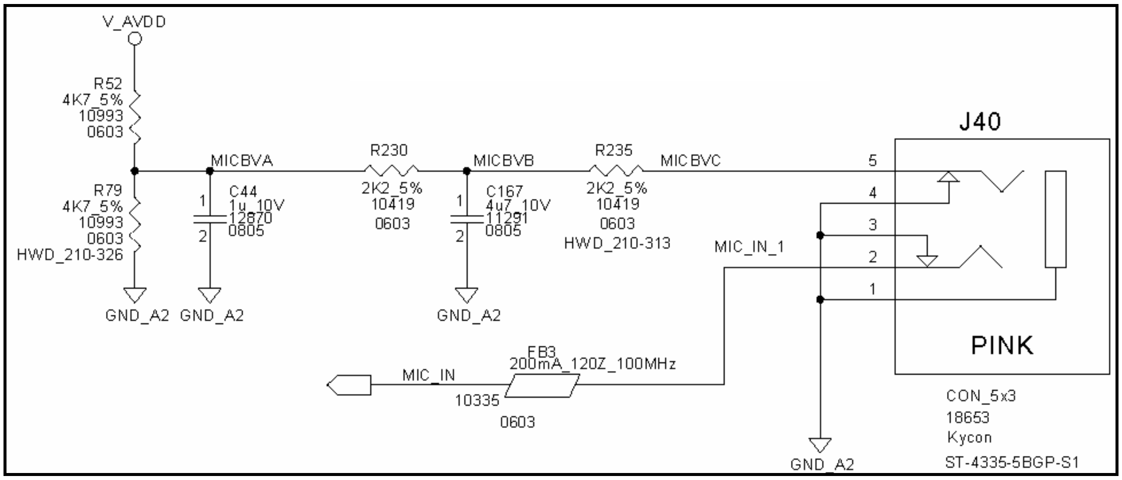


Figure 14-4: Line-In Schematic

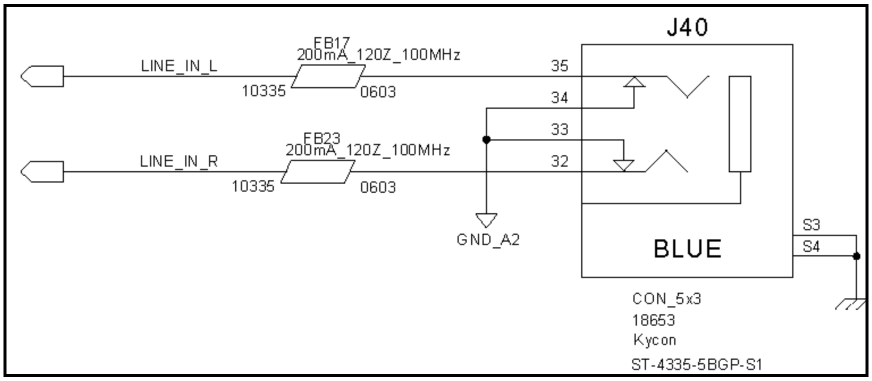
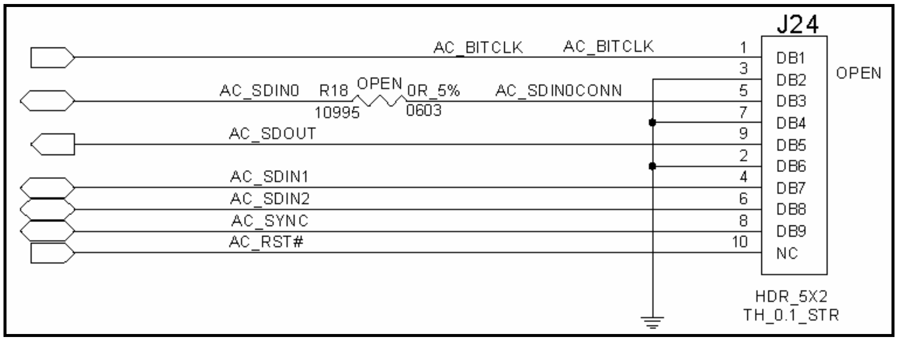


Figure 14-5: Optional AC'97 Expansion Schematic



14.4 High-Definition Audio

A different Codec is required to implement high-definition audio. Suitable devices are available from Sigmatel. The model numbers are STAC9200, STAC9220, or STAC9221. The STAC9221 has a pin-out that, except for four pins, is the same as the Cirrus Logic CS4299 AC '97 Codec used in the AC '97 example in Figure 14-5 above. A circuit-build option that allows either AC '97 audio or HD audio should be achievable.

15 PCI Bus and PCIe Lanes 6-15

15.1 PCI Bus and PCIe Lanes 6-15 – Signal Definitions

The set of pins shown in Table 15-1 below are defined by the COM Express™ Specification to be either a 32-bit PCI bus or a set of general-purpose PCI Express (PCIe) Lanes 6-15.

For Module Types 2 and 3, support for a PCI bus is required. PCIe Lanes 6-15 are not available. For Module Types 4 and 5, PCIe Lanes 6-15 are optionally available; the PCI bus is unavailable.

PCI bus signals support up to four REQ/GNT pairs. The PCI bus typically runs at 33MHz, although some Modules may run the bus at 66MHz. The COM Express PCI bus is specified to be 5V tolerant, with 3.3V signaling. All necessary PCI pull-ups are included on the Module.

Table 15-1: PCI Bus and PCIe 6-15 Pin-outs

Module Pin	Module Type 2,3 PCI Bus	Module Type 4,5 PCIe 6-15		Module Pin	Module Type 2,3 PCI Bus	Module Type 4,5 PCIe 6-15
C15	PCI_PME#	RSVD				
C16	PCI_GNT2#	RSVD				
C17	PCI_REQ2#	RSVD				
C18	PCI_GNT1#	RSVD				
C19	PCI_REQ1#	PCIE_RX6+		D19	PCI_GNT3#	PCIE_TX6+
C20	PCI_GNT0#	PCIE_RX6-		D20	PCI_REQ3#	PCIE_TX6-
C21	GND (FIXED)			D21	GND (FIXED)	
C22	PCI_REQ0#	PCIE_RX7+		D22	PCI_AD1	PCIE_TX7+
C23	PCI_RESET#	PCIE_RX7-		D23	PCI_AD3	PCIE_TX7-
C24	PCI_AD0	RSVD		D24	PCI_AD5	RSVD
C25	PCI_AD2	RSVD		D25	PCI_AD7	RSVD
C26	PCI_AD4	PCIE_RX8+		D26	PCI_C/BE0#	PCIE_TX8+
C27	PCI_AD6	PCIE_RX8-		D27	PCI_AD9	PCIE_TX8-
C28	PCI_AD8	RSVD		D28	PCI_AD11	RSVD
C29	PCI_AD10	PCIE_RX9+		D29	PCI_AD13	PCIE_TX9+
C30	PCI_AD12	PCIE_RX9-		D30	PCI_AD15	PCIE_TX9-
C31	GND (FIXED)			D31	GND (FIXED)	
C32	PCI_AD14	PCIE_RX10+		D32	PCI_PAR	PCIE_TX10+
C33	PCI_C/BE1#	PCIE_RX10-		D33	PCI_SERR#	PCIE_TX10-
C34	PCI_PERR#	RSVD		D34	PCI_STOP#	RSVD
C35	PCI_LOCK#	RSVD		D35	PCI_TRDY#	RSVD
C36	PCI_DEVSEL#	PCIE_RX11+		D36	PCI_FRAME#	PCIE_TX11+
C37	PCI_IRDY#	PCIE_RX11-		D37	PCI_AD16	PCIE_TX11-
C38	PCI_C/BE2#	RSVD		D38	PCI_AD18	RSVD
C39	PCI_AD17	PCIE_RX12+		D39	PCI_AD20	PCIE_TX12+
C40	PCI_AD19	PCIE_RX12-		D40	PCI_AD22	PCIE_TX12-
C41	GND (FIXED)			D41	GND (FIXED)	
C42	PCI_AD21	PCIE_RX13+		D42	PCI_AD24	PCIE_TX13+
C43	PCI_AD23	PCIE_RX13-		D43	PCI_AD26	PCIE_TX13-
C44	PCI_C/BE3#	RSVD		D44	PCI_AD28	RSVD
C45	PCI_AD25	RSVD		D45	PCI_AD30	RSVD
C46	PCI_AD27	PCIE_RX14+		D46	PCI_IRQC#	PCIE_TX14+
C47	PCI_AD29	PCIE_RX14-		D47	PCI_IRQD#	PCIE_TX14-
C48	PCI_AD31	RSVD		D48	PCI_CLKRUN#	RSVD
C49	PCI_IRQA#	PCIE_RX15+		D49	PCI_M66EN	PCIE_TX15+
C50	PCI_IRQB#	PCIE_RX15-		D50	PCI_CLK	PCIE_TX15-
C51	GND (FIXED)	GND (FIXED)				

15.2 PCI Bus – Routing Considerations

15.2.1 PCI Bus Routing – General Signals

Route the PCI bus with 55-ohm, single-ended signals. The bus may be referenced to ground (preferred), or to a well-bypassed power plane, or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching is not required.

See the PCI bus section in Appendix B for a summary of trace routing parameters and guidelines.

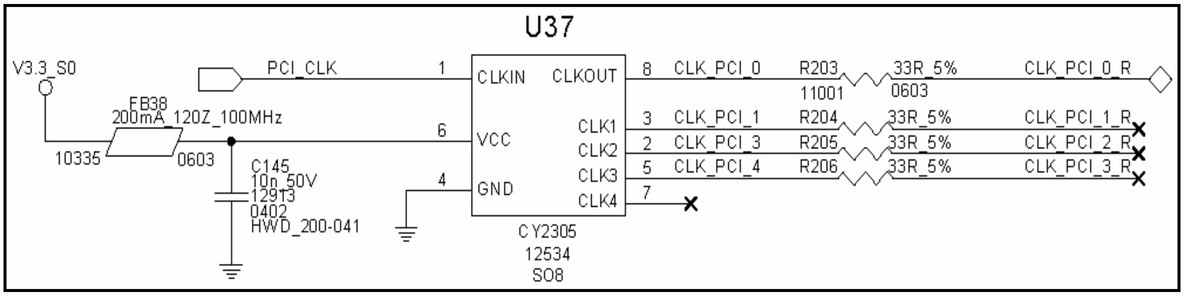
15.2.2 PCI Clock Routing

The COM Express™ Specification allows 1.6 ns +/- 0.1ns for the propagation delay of the PCI clock from the Module pin to the destination pin of the PCI device. Using a typical propagation delay value of 180 ps / inch, this works out to 8.88 inches of Carrier Board trace for a device-down application. For device-up situations, the PCI Local Bus Specification allows 2.5 inches of clock trace on the slot card. This is deducted from the 8.88 inches, yielding 6.38 inches. On a Carrier Board with a small form factor, serpentine clock traces may be required to meet the clock-length requirement.

Route the PCI clock as a single-ended, 55-ohm trace with generous clearance to other traces and to itself. A continuous ground-plane reference is recommended. Routing the clock on a single ground references internal layer is preferred to reduce EMI.

The COM Express™ Specification brings a single PCI clock out of the Module. If there are multiple PCI targets on the Carrier Board design, then a zero delay clock buffer as shown in Figure 15-1 below is recommended, providing a separate copy of the PCI clock to each target.
A Cypress Semiconductor device is shown. The overall delay from the Module PCI clock pin to the target PCI device clock pin should be 1.6 ns.

Figure 15-1: PCI Bus Clock Buffer Schematic



15.3 PCI Bus – Reference Schematics

15.3.1 PCI Bus Slot Example

Figure 15-1 above illustrates a Carrier Board PCI Bus slot.

- The COM Express™ Specification requires that the PCI bus use 3.3V signaling and have a tolerance for 5V. This allows Carrier Boards to use 3.3V or 5V PCI bus slots and devices.

- The COM Express™ Specification calls out a 32-bit PCI bus. The bus may be 33MHz or 66MHz. Module signal PCI_M66EN alerts the Carrier Board that the Module is 66MHz-capable. The Module pulls this line high if it is 66MHz-capable.

- The interface supports up to four REQ# / GNT# Pairs for a combination of device-down or slot applications.

- Most PCI signals are connected in parallel to all slots or devices. The following pins from each slot or device are the exceptions:

  - IDSEL is connected thru a resistor to a different PCI_AD (PCI address) line for each slot. The suggested value is 22 ohm. The PCI_AD line used should be determined from Table 15-2 above.

  - CLK is connected to a different copy of the Module PCI clock signal for each slot. Only one PCI device or slot should be driven from each Module PCI clock output.

  - The slot INTA# pin is connected to a different Module interrupt signal for each slot, per Table 15-2 above. This reduces interrupt latency by giving each slot an individual interrupt rather than a shared interrupt.

  - REQ# is connected to a different Module request signal for each slot, per Table 15-2 above.

  - GNT# is connected to a different Module grant signal for each slot, per Table 15-2 above.

- Per Section 15.2.2 above, the PCI clock from the Module pin to the slot pin should be about 6.38 inches long.

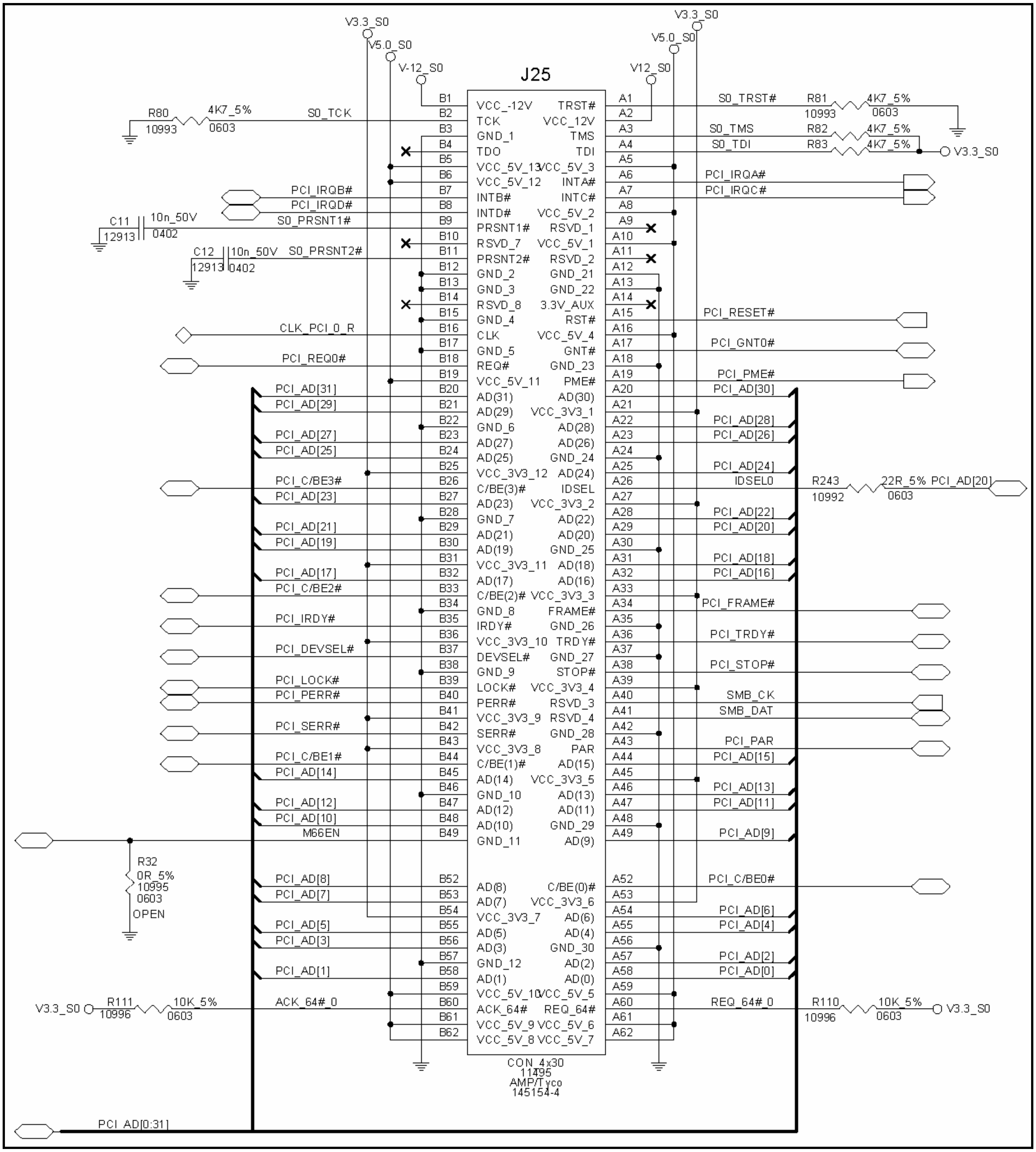
15.3.2 PCI Bus Device-Down Considerations

- A PCI device that is implemented directly on the Carrier Board uses a subset of the signals shown on the slot connector. Some pins on the slot connector are used for slot and management functions of the PCI card and are not necessary to operate the PCI device.
- An individual PCI device will not use pins REQ_64#, ACK_64#, M66EN, PRSNT1#, PRSNT2#, or the reserved pins.
- Most devices do not implement test pins TCK, TDO, TDI, TMS, and TRST.
- Most PCI devices use INTA# only and do not have a connection for INTB#, INTC# or INTD#. However, the INTA# pin of the device should not necessarily be connected to the ETXexpress PCI_IRQA# signal. See Table 15-2 for more information.
- Per Section 15.2.2 above, the PCI clock from the Module pin to the device pin should be about 8.88 inches long.

15.4 PCIe Lanes 6–15 Option – Module Types 4 and 5

The set of pins used for the PCI bus implementation in Module Types 2 and 3 is reallocated for a set of general purpose PCI Express (PCIe) lanes in Module Types 4 and 5. The PCIe lanes are designated lanes 6 thru 15. The design and routing concerns for these PCIe lanes are the same as those for PCIe lanes 0 thru 5, described in Section 5. Please refer to that section.

Figure 15-2: PCI Slot 5V, 32 Bit/33MHz Schematic



16 LPC Bus Implementation

16.1 LPC Bus – Signal Definitions

The LPC (Low Pin Count) bus is a versatile, easy-to-use bus than can carry low-bandwidth peripherals such as serial ports, firmware memory, legacy peripherals and general-purpose inputs and outputs. The LPC bus uses four data bits and a 33MHz clock, yielding a maximum bandwidth of approximately 16 megabytes per second – about double the bandwidth of the legacy ISA bus. It is straightforward to develop PLDs or FPGAs that interface to the LPC bus.
A PLD circuit example is given in Section 16.3.5 below.

The LPC bus is implemented on the COM Express A-B connector per Table 16-1 below.

Table 16-1: LPC Signals

Module Pin	Signal Name		Module Pin	Signal
			B3	LPC_FRAME#
			B4	LPC_AD0
			B5	LPC_AD1
			B6	LPC_AD2
			B7	LPC_AD3
			B8	LPC_DRQ0#
			B9	LPC_DRQ1#
			B10	LPC_CLK
			B18	SUS_STAT#
A34	BIOS_DISABLE#			
A50	LPC_SERIRQ		B50	CB_RESET#

- Signal CB_RESET# is an active-low-reset output from the Module. Use CB_RESET# to reset LPC devices.
- Signal SUS_STAT# is a Module output that may be used to notify LPC devices of an imminent suspend operation.
- The BIOS_DISABLE# signal, if pulled low on the Carrier Board, disables the Module BIOS. The BIOS may instead reside on the Carrier Board on either the LPC or PCI buses.

16.2 LPC Bus – Routing Considerations

16.2.1 LPC Bus Routing – General Signals

LPC signals are similar to PCI signals and may be treated similarly. Route the LPC bus as 55-ohm, single-ended signals. The bus may be referenced to ground (preferred), or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching is not required.

See the LPC bus section in Appendix B for a summary of trace-routing parameters and guidelines.

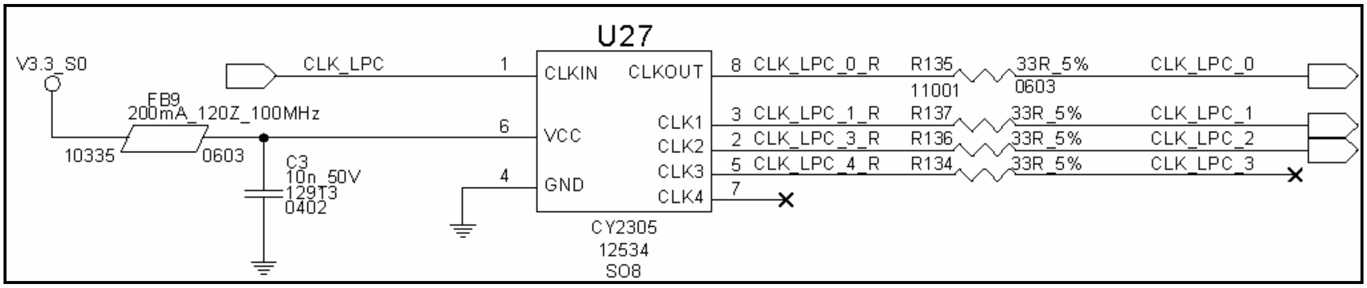
16.2.2 LPC Bus Clock Routing

The LPC bus clock is similar to the PCI bus clock and should be treated similarly. The COM Express™ Specification allows 1.6 ns +/- 0.1ns for the propagation delay of the LPC clock from the Module pin to the LPC device destination pin. Using a typical propagation delay value of 180 ps / inch, this works out to 8.88 inches of Carrier Board trace for a device-down application. For device-up situations, 2.5 inches of clock trace are assumed to be on the LPC slot card (by analogy to the PCI specification). This is deducted from the 8.88 inches, yielding 6.38 inches.
On a Carrier Board with a small form factor, serpentine clock traces may be required to meet the clock-length requirement.

Route the LPC clock as a single-ended, 55-ohm trace with generous clearance to other traces and to itself. A continuous ground-plane reference is recommended. Routing the clock on a single ground references internal layer is preferred to reduce EMI.

The COM Express™ Specification brings a single LPC clock out of the Module. If there are multiple LPC targets on the Carrier Board design, then a zero delay clock buffer is recommended. The buffer recommendation is the same as the one shown for the PCI clock in Section 15, Figure 15-1 above. This provides a separate copy of the LPC clock to each target. The overall delay from the Module LPC clock pin to the target LPC device clock pin should be 1.6 ns.

Figure 16-1: LPC Clock Buffer Schematic



16.2.3 LPC Firmware Hub – Carrier Board BIOS – Reference Schematic

An example of a Carrier Board Firmware Hub (FWH) implementation is shown in Figure 16-2 below. Use the FWH to store and execute BIOS code.

An interesting feature of the COM Express™ Specification is the inclusion of the BIOS_DISABLE# pin. If this pin is pulled low on the Carrier Board, then the BIOS on the Module is disabled. The BIOS can instead reside on the Carrier Board LPC or PCI buses. This is useful in some regulatory situations in which it is required that regulatory technicians remove the BIOS, check its integrity, and replace it. There is usually room on a Carrier Board for a socketed BIOS, whereas the Module BIOS is often a surface-mount device. The use of this feature is illustrated in the example below.

- The BIOS device shown in Figure 16-2 below is an ST Microelectronics M50FW080 or SST SST49LF008A Firmware Hub in a 32-pin PLCC package. The socket used is a 32-pin PLCC socket, AMP/Tyco 822498-1. This is a surface-mount socket, and PCBs can be laid out such that the socket or the FWH itself is soldered to the Carrier Board.

- The FWH is connected to the system via the LPC interface. Data and address information are carried on the LPC_AD[0:3] lines. LPC_FRAME indicates the start of a new frame.

- FWH pins 2 (RST#) and 24 (INIT#) reset the FWH. These pins are logically combined together internally on the FWH, and a low on either pin will reset the FWH.

- FWH pins 6, 5, 4, 3, 30 – (FGPI [0:4]) are general-purpose inputs that may be read by system software. They should be tied to a valid logic level.

- FWH pin 7 (WP#) enables write protection for main block sectors when it is pulled low. If pulled high, hardware write protection is disabled. FWH pin 8 (TBL#) enables write protection for the top block sector when pulled low.

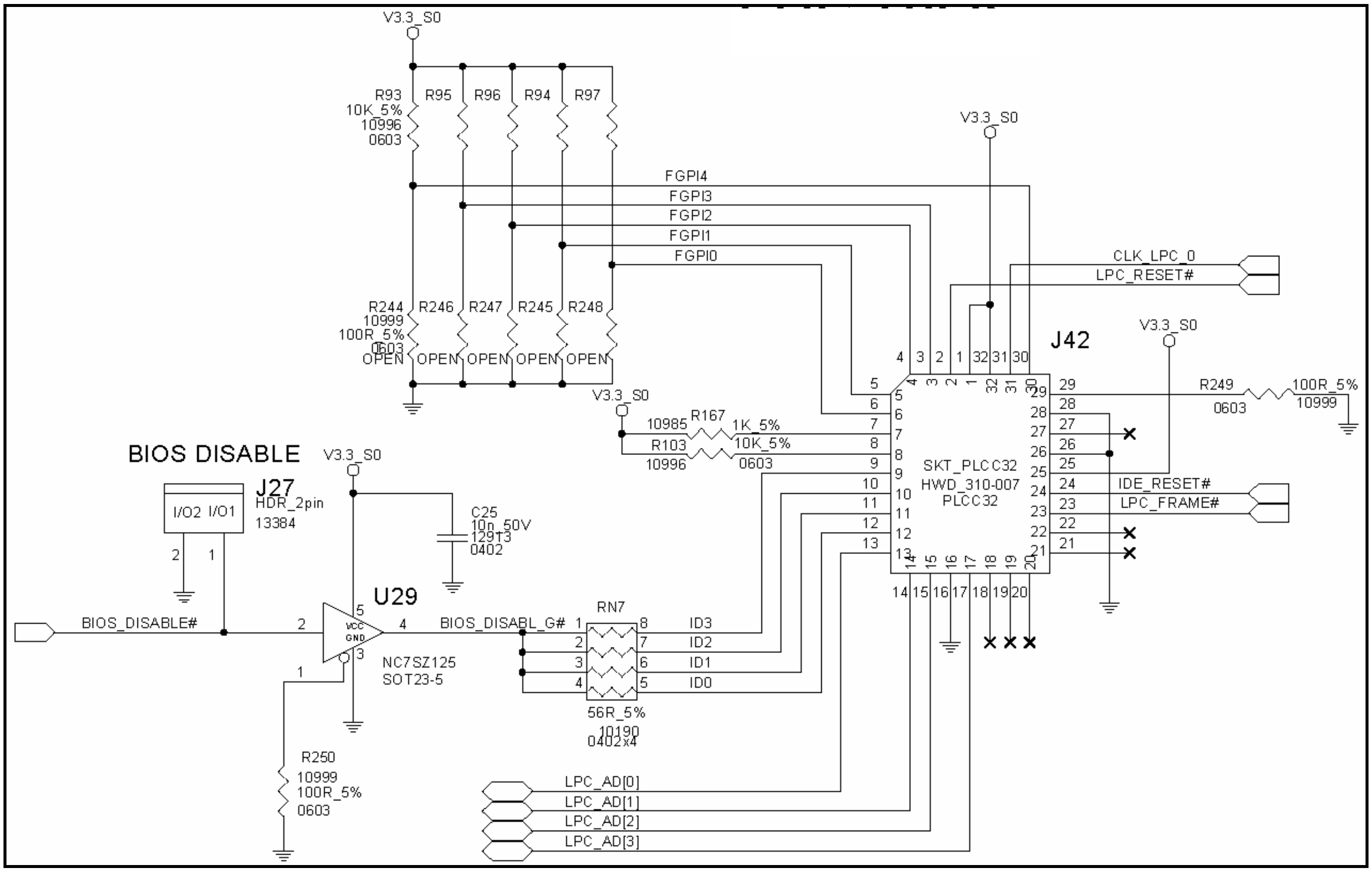
- FWH pins 12,11,10, 9 (ID[0:3]) are ID pins that allow multiple FWH parts (up to 16) to be used. By convention, in Intel x86-based systems, the boot device is FWH number 0. To boot from the Carrier Board FWH, the Module BIOS_DISABLE# pin must be low (to disable the Module BIOS) and the Carrier Board FWH ID[0:3] pins (pins 12,11,10,9) must be low (to enable it as the boot device). If Jumper J27 in Figure 16-2 below is installed, the Module BIOS is disabled, and the Carrier Board FWH may be used as a boot device.

- FWH pin 29 configures the FWH into one of two modes: if high, the FWH is in the Programmer configuration. If low, it is in the Firmware Hub configuration. For normal operation on a Carrier Board, this pin should be tied low.

- FWH pin 31 is the clock input. The clock source is the LPC_CLK signal from the ETXexpress Module. The net is designated as CLK_LPC_0 after zero-delay buffering.

- FWH pin 2 – RST# supports Chip Reset. The LPC_RESET# signal from the ETXexpress Module drives the reset. The pin functions the same as INIT# above.

Figure 16-2: LPC Firmware Hub – Carrier Board BIOS Schematic



16.3 LPC Bus – Reference Schematics

A Carrier Board Super I/O implementation that uses a Winbond W83627HFJ is illustrated in the following sections. A Super I/O needs BIOS or other system software to initialize the Super I/O register set. The necessary BIOS support may be included in the Module BIOS already, or it may need to be added.

16.3.1 LPC Super I/O

These design details apply to Figure 16-3 below.

- LPC_AD[0:3] are sourced from the ETXexpress Module. Address, Data and Control Interface signals are carried over the LPC bus.
- LPC_FRAME# is sourced from the ETXexpress Module. The signal indicates the start of new cycle.
- LPC_DRQ0# is sourced from the Super I/O. This serves as a DMA Request signal to the Module. The LPC_DRQ signals cannot be shared. LPC_DRQ0# should be a two-point net.
- LPC_SERIRQ is a bidirectional signal between Module and the Super I/O. This serves as Serial IRQ input/output.
- PCI_PME# is sourced from the Super I/O. The Power Management Event input causes the system to wake when in low-power states. The Super I/O can be programmed to have events such as a keyboard press trigger the PCI_PME#.
- CLK_LPC_2 is a copy of the Module LPC_CLOCK. A zero-delay buffer is used (not shown).
- Net PCI_RESET#_B (pin LRESET#) resets the Super I/O. This is driven by PCI_RESET# from the ETXexpress Module. The signal is designated as PCI_RESET#_B after buffering. Module signal CB_RESET# also can reset LPC devices.
- The KBD_RST# signal is sourced by the keyboard controller in the Super I/O. This signal is a relic of the PC-AT architecture. The signal is pulled high on the ETXexpress Module.
- KBD_A20GATE signal input goes to the ETXexpress Module. The signal is pulled high on the ETXexpress Module. (There is an error in the COM Express™ Specification, Rev. 1, which states that this signal is pulled low on the Module. The error is corrected in Rev 1.1 of the specification).
- KCLK and KDAT signals are for Keyboard Clock and Data respectively.
- MCLK and MDAT signals are for the Mouse Clock and Data respectively.
- PWRBTN# input to the ETXexpress Module from Super I/O pin PSOUT# wakes the system from Suspend State 5. See Figure 19.1 below for Power-Sequencing details.
- The schematic shows option resistors that allow the Module PWRBTN# input to be driven directly by net PWRBTN# _EXT. In this case, the Super I/O is bypassed.
  The PWRBTN_EXT# net is pulled to ground by a button press (switch not shown here).
  This drives PWRBTN# input to the ETXexpress Module to wake the system from Suspend State 5. Implement the bypass by stuffing 0Ω resistor R1 and removing R43.

- PSIN is driven low by a pressing the power button. The PSIN signal causes the Super I/O to drive PSOUT#. This results in PWRBTN# input to the ETXexpress Module. The Super I/O may be programmed to have other events such as keyboard or mouse activity bring the system out of suspend.

- V_BAT is connected to a 3.3V standby battery (usually thru a diode and resistor to meet U.L. requirements). This provides a power source to the Super I/O to monitor events in the absence of other power sources.

- IRTX and IRRX are serial-port signals used with an infra-red transceiver.

- RSMRST# (Resume Reset, active low) is an output from the Super I/O. The Super I/O has an internal voltage monitor that monitors the +5V standby rail (V5.0_S5) and generates an active-low-reset pulse if the rail is below the monitor's threshold. Resume reset is only needed for devices that need to know about a loss of the +5V standby rail. Such devices include the circuitry that monitors the power button. Such circuitry exists in the Super I/O and in the Module chipset. However, there is no COM Express pin allocated to resume reset, and the function is performed internally to the Module. (The Module has its own resume reset monitor that looks at the +5V standby rail). In this schematic example, RSMRST# goes off page to a latch that is used to monitor the watchdog output, and the latch is reset when there is a complete AC power cycle. Most Carrier Board designs will not need to make use of the Super I/O resume reset output.

- Net PWR_OK is sourced form the ATX Power Supply input to Super I/O pin PWROK\GP32. The signal indicates the availability of stable power on all rails from the power supply.

- Net SIO_PSON# is sourced from the Super I/O (pin 72, PWRCTL#\GP31). This net can control the ATX power supply PS_ON# pin (pin 16 on the ATX power-supply header, not shown in this figure). However, the ATX power supply PS_ON# also can be controlled by the suspend status signal from the Module – specifically, Module signal SUS_S5#. The SUS_S5# signal needs to be inverted before connecting to the ATX PS_ON# pin. Use an open-drain driver, with a pull-up to the +5V standby rail. Then the PS_ON# pin can be forced low with a jumper to force the power supply on. This can be useful in debug situations.

- The Module signal SUS_S5# indicates that the Module is in the S5 suspend mode. This signal is input to the Super I/O, to the SLP_SX#\ (GP30) pin. The Super I/O uses the SUS_S5# to factor into logic that controls how the SIO_PSON# pin behaves after a complete power loss. The Super I/O has options that allow it to have the system-power default to either off or on after an AC power cycle.

- TX0 thru RTS0# implement signals for the serial port that is interconnected to RS232 level translators. The level translators are shown later in this section.

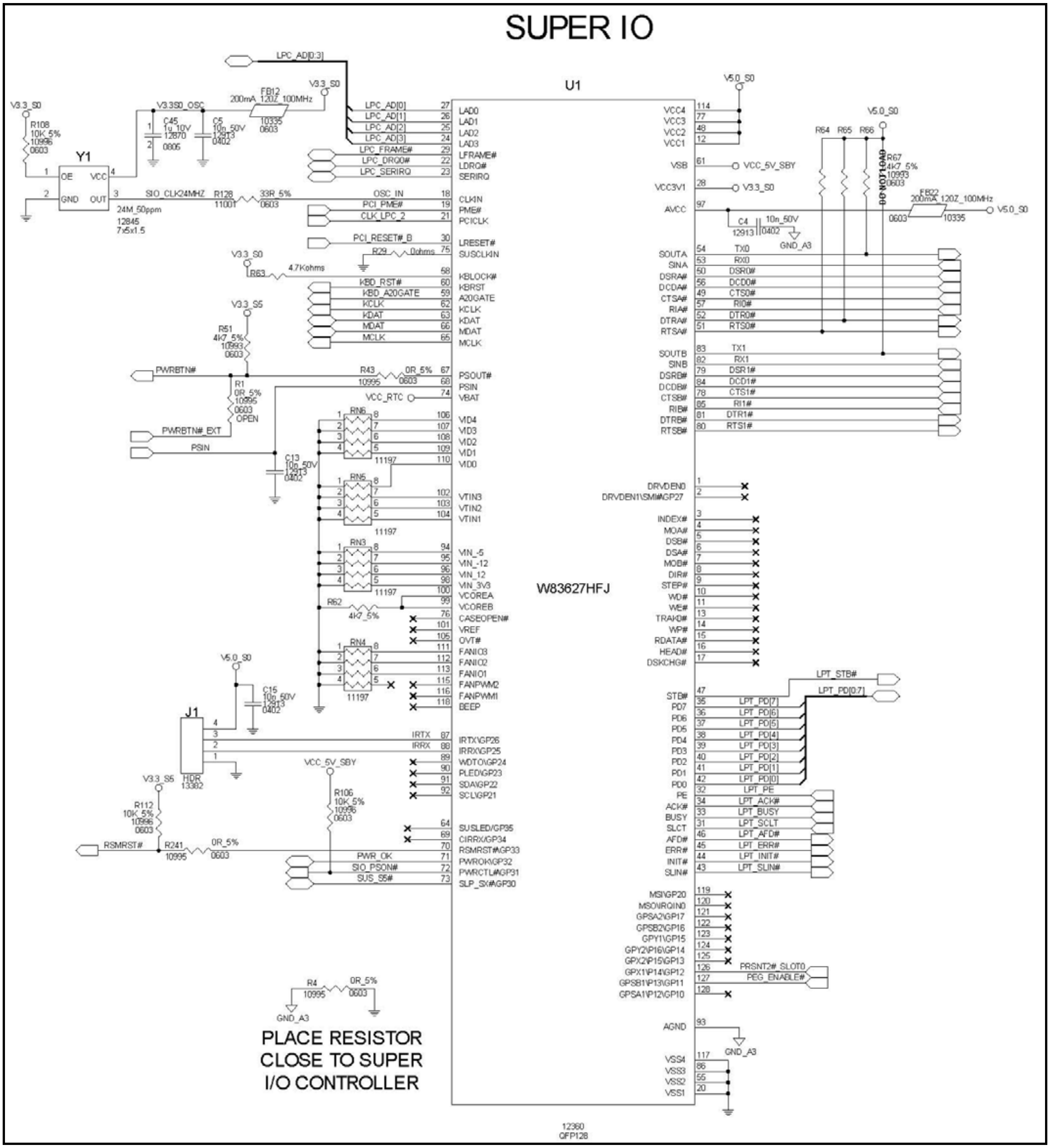
- TX1 thru RTS1# implement signals for the serial port that is interconnected to RS232 level translators. The level translators are shown later in this section.

- LPT_STB thru LPT_SLIN# implement signals for the parallel port.

- The PRSNT2#_SLOT0 input to Super I/O Pin 126 (GP12) allows system software to detect the presence of a plug-in card in the slot. In practice, the BIOS does not necessarily make use of this option. This also applies to net PRSNT2#_SLOT1.

- The PEG_ENABLE# input to Super I/O Pin 127 (GP11) allows the system software to detect the presence of a plug-in graphics card in the slot. In practice, the BIOS does not necessarily make use of this option. This also applies to net PRSNT2#_SLOT1.

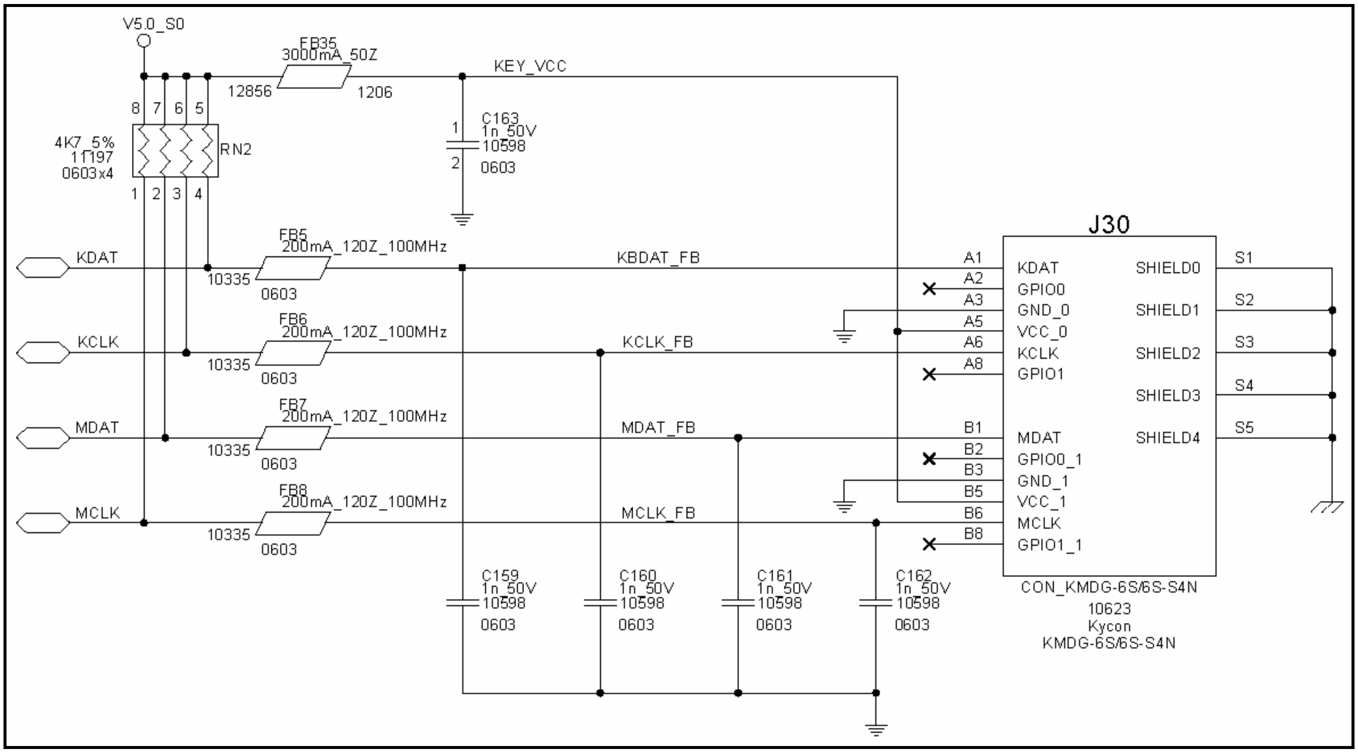
Figure 16-3: LPC Super I/O Schematic



16.3.2 LPC Super I/O – PS/2 Keyboard and Mouse

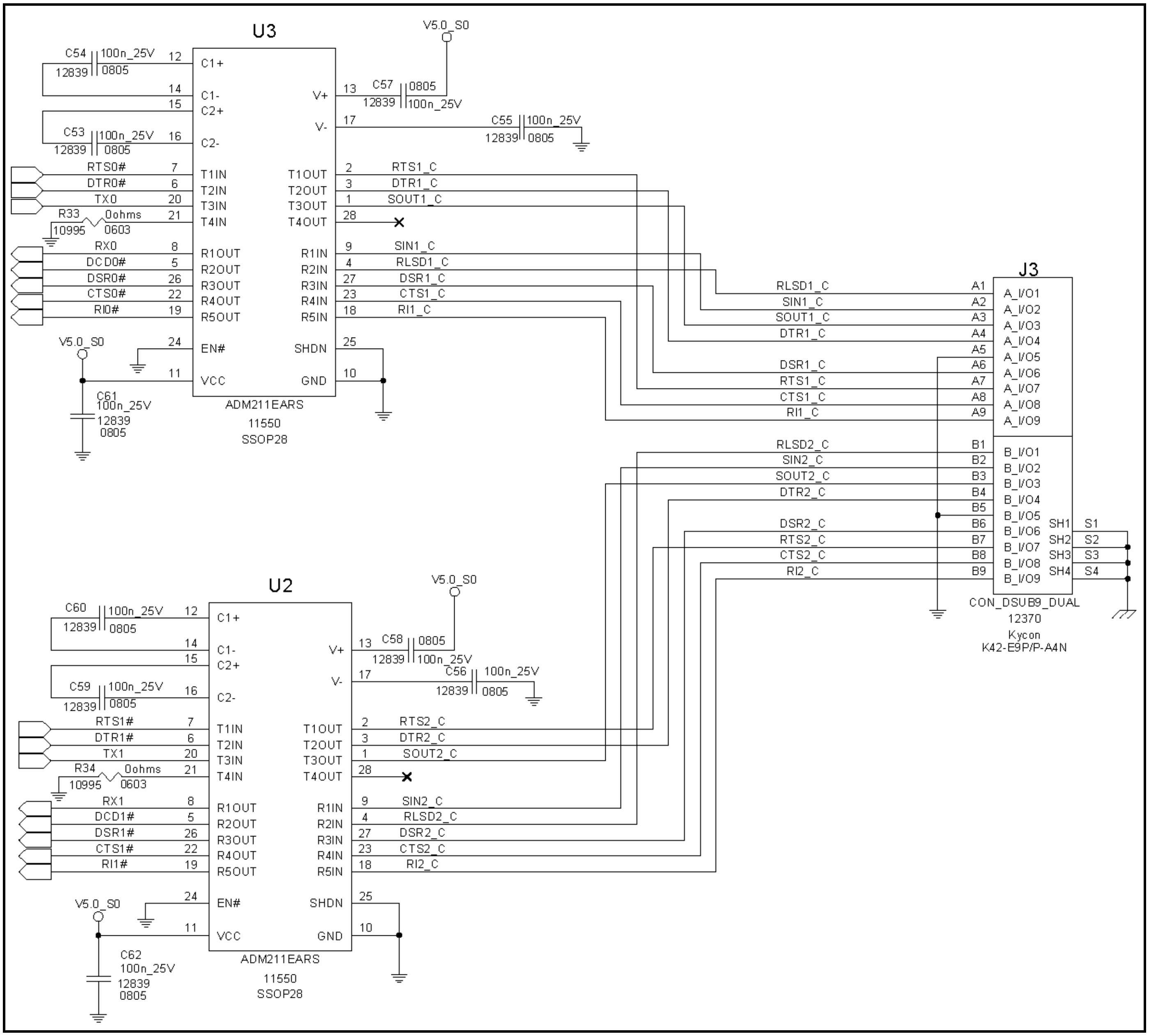
- Figure 16-4 below shows the interconnect for the PS/2 Keyboard and Mouse Combo Connector.
- Ferrite beads are incorporated to suppress noise.

Figure 16-4: LPC Super I/O – PS/2 Keyboard and Mouse Schematic



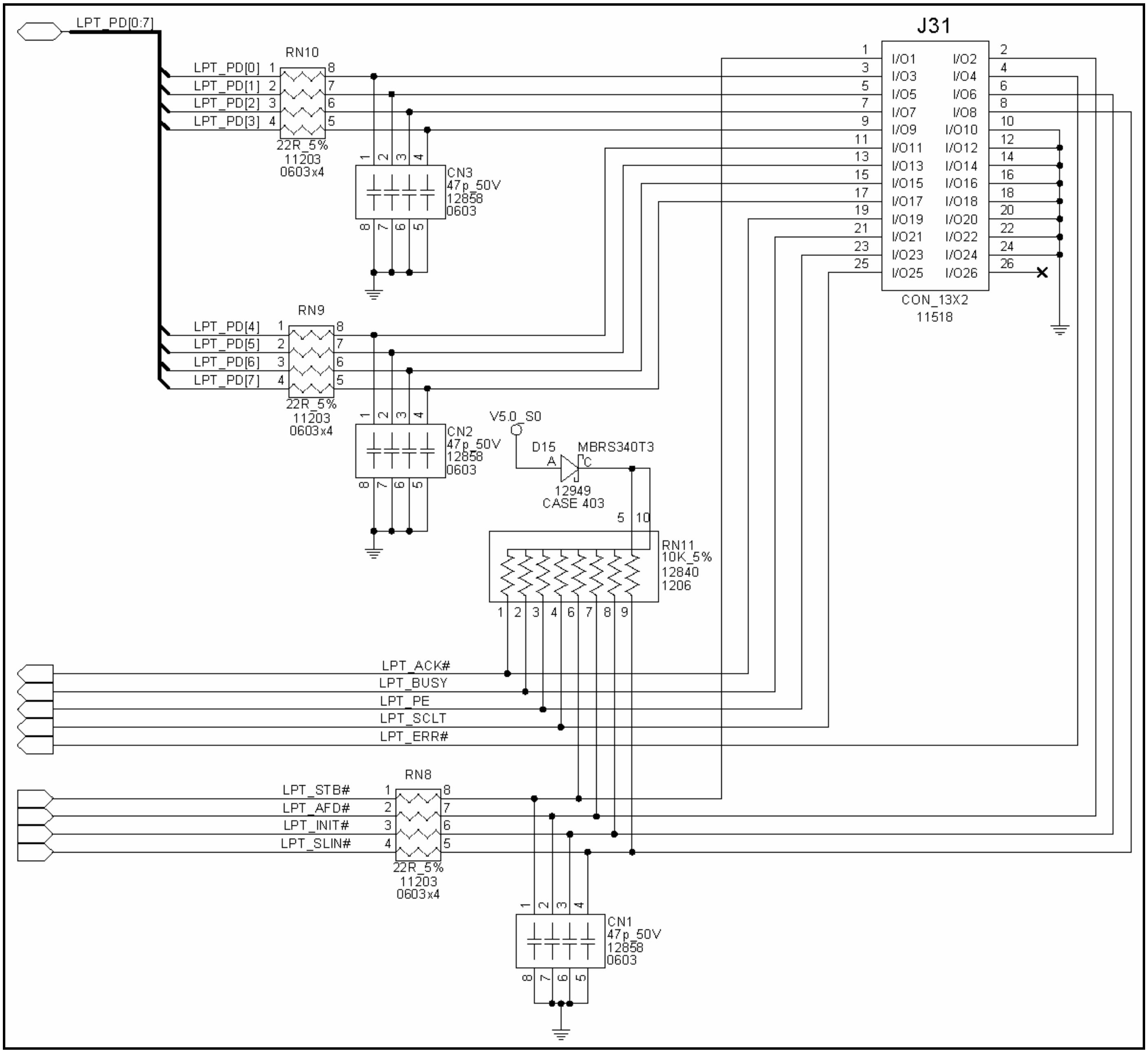
16.3.3 *LPC Super I/O Serial Port*

Figure 16-5: LPC Super I/O – COM1/COM2 Schematic



16.3.4 LPC Super I/O Parallel Port

Figure 16-6: LPC Super I/O – Parallel Port Schematic

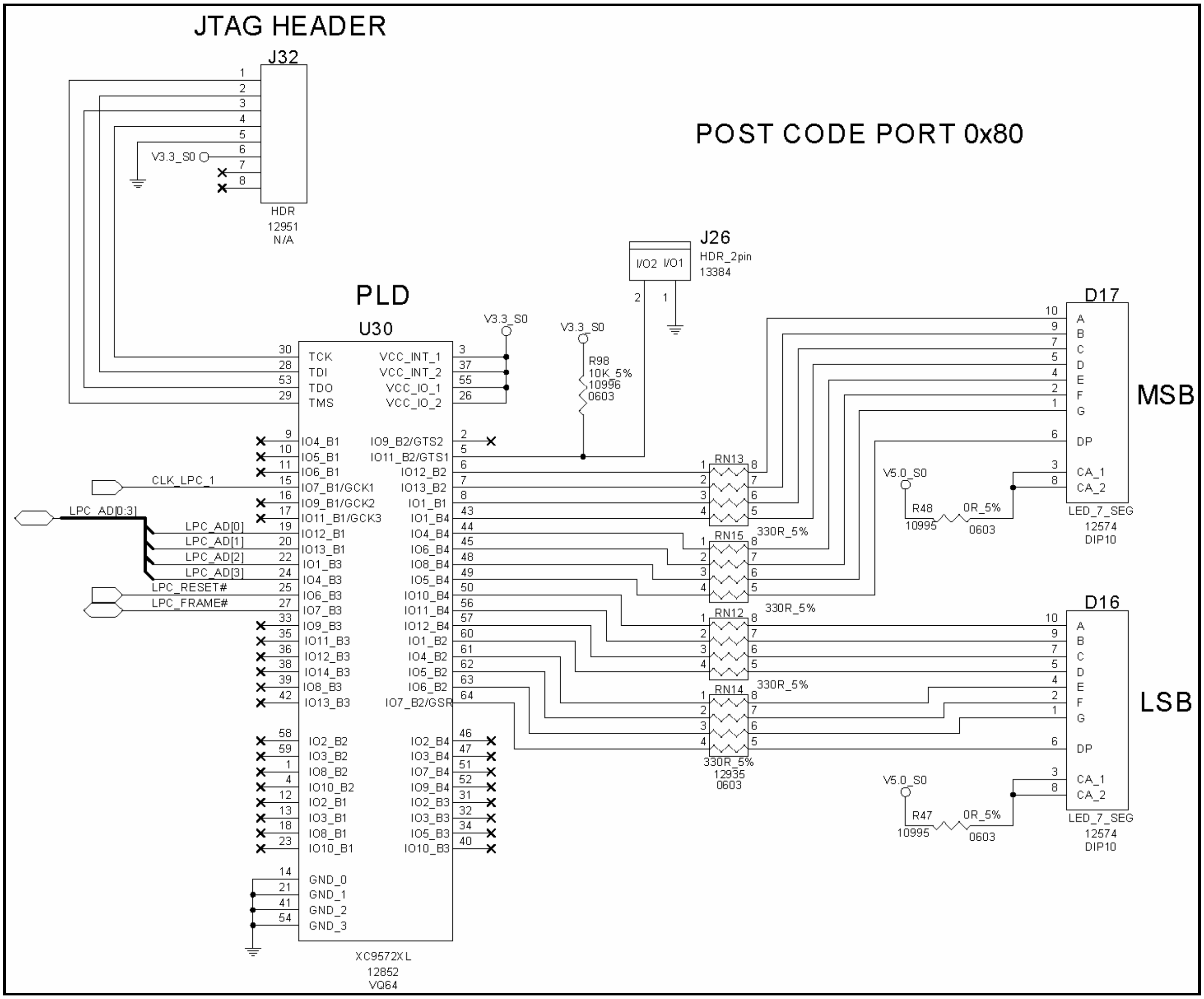


16.3.5 LPC PLD Example – Port 80 Decoder

The following applies to Figure 16-7 below.

- The JTAG header may be used to program the PLD in-circuit.
- The LPC bus is the interface to the Module host system.
- Two seven-segment LED displays show the Port 80 POST (Power On Self Test) codes. PLD outputs drive the LEDs.
- On some systems, a BIOS setting is needed to allow POST codes to be forwarded to the LPC bus.
- The VHDL PLD source code for this example is given in Appendix F.
- The LPC_RESET# in Figure 16-7 below is a buffered version of Module signal CB_RESET# or PCI_RESET#.

Figure 16-7: LPC PLD Example – Port 80 Decoder Schematic



17 I^{2}C Bus

17.1 I^{2}C Bus – Signal Definitions

The I^{2}C (Inter-Integrated Circuit) bus is a two-wire serial bus originally defined by Philips.
The bus is used for low-speed (400kbps) communication between system ICs.
The bus is often used to access small serial EEPROM memories and to set up IC registers.
A reference to the I^{2}C source specification can be found in Appendix G.

The COM Express™ Specification defines five buses that are brought to the Module connector that use the I^{2}C format and protocol. These are summarized in Table 17-1 below.

Table 17-1: COM Express I^{2}C Signal Groups

I2C Bus Function	Clock	Data
General Purpose User I^{2}C	I2C_CK	I2C_DAT
LVDS display parameters	LVDS_I2C_CK	LVDS_I2CDAT
SDVO parameters	SDVO_CK	SDVO_DATA
System Management Bus	SMB_CK	SMB_DAT
VGA display parameters	VGA_I2C_CLK	VGA_I2C_DAT

Four of the five COM Express I^{2}C buses are special-purpose buses. Carrier Board designers should take special care when connecting to the special-purpose buses. The System Management Bus (SMB) is used on the Module to collect information and controls many important Module subsystems, including DRAM SPD, system hardware monitors, and clock synthesizers and buffers. A fault introduced on the SMB could prevent the Module from functioning.

The COM Express general purpose I^{2}C pins are on the B row of the COM Express A-B connector as shown in Table 17-2 below.

Table 17-2: User I2C Signals

Module Pin	Signal Name
B33	I2C_CK
B34	I2C_DAT

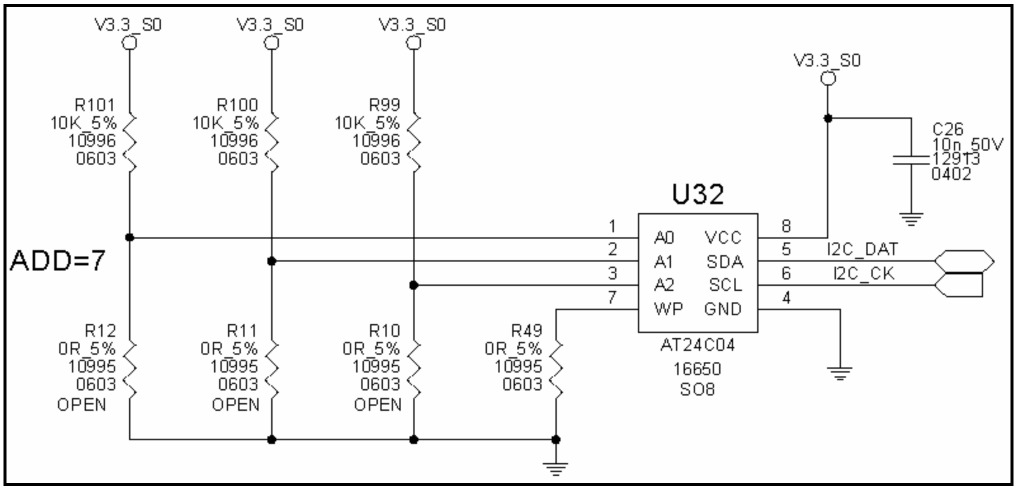
The ETXexpress general purpose I^{2}C interface is supported in the BIOS supplied by Kontron. The JIDA interface allows I^{2}C access.

17.2 I²C Bus EEPROM – Reference Schematics

The following notes apply to Figure 17-1 below.

- The EEPROM stores configuration information for the system of the Carrier Board. The data structure used is defined in the COM Express™ Specification. The Specification recommends but does not require the use of this system configuration EEPROM. The Module BIOS may check the Carrier Board configuration EEPROM but is not required to do so by the Specification.
- The Atmel AT24C04 with 4Kb organized as 512 x 8 is a suitable device in an 8-pin SOIC package.
- For applications that require additional ROM or memory capacity such as 8Kb (1K x 8) or 16Kb (2K x 8), an Atmel AT24C08A or AT24C16A may be used.
- The COM Express™ Specification requires a minimum capacity of 2Kb.
  The Atmel AT24C02 meets the minimum capacity.
- Net I2C_DAT is sourced from ETXexpress Module pin B34.
- Net I2C_CK is sourced from ETXexpress Module pin B33.
- Address inputs A0, A1, A2 are pulled high. This creates an I²C Address A7 (hex), which is required by the COM Express™ Specification. EEPROM devices internally set I2C address lines A6, A5, A4, A3 to binary value 1010.
- WP (write protect) is pulled low for normal read/write.

Figure 17-1: I²C Bus EEPROM Schematic



18 Miscellaneous Functions

18.1 SPKR Out

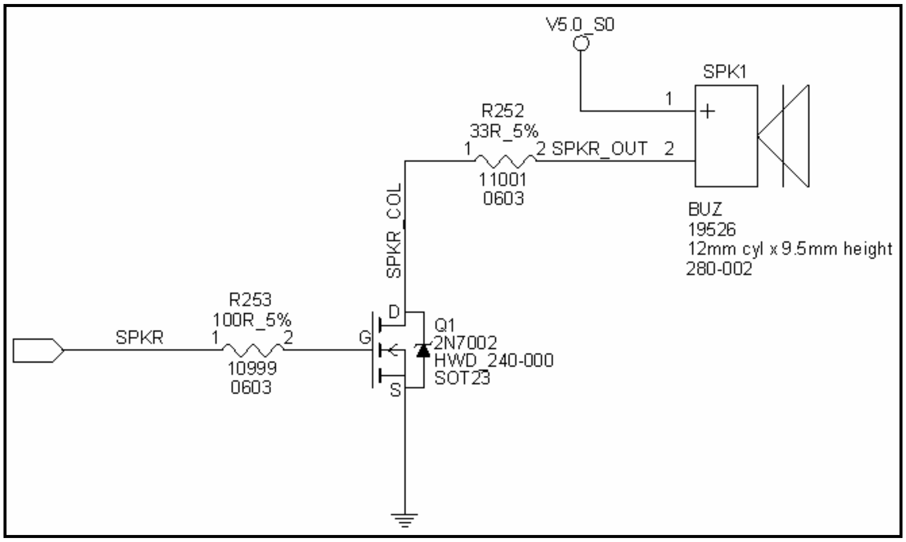
The PC-AT architecture provides a speaker signal that creates beeps and chirps. The signal is a digital-logic signal that is created from system timers within the core chipset. The speaker provides feedback to the user that an error has occurred. The system BIOS usually drives the speaker line with a set of beep codes to indicate hardware problems such as a memory test failure, a missing video device, or a missing keyboard. Application software often uses the PC-AT speaker to flag an error such as an invalid key press.

This speaker signal should not be confused with the analog-audio signals produced by the audio CODEC. In many systems, the PC-AT speaker signal is fed into one of the audio CODEC inputs, allowing it to be mixed with other audio signals and heard on the audio transducer (speakers and headphones) that the CODEC drives.

The PC-AT audio transducer that is used for error messages is usually a small, low-cost loudspeaker or piezo-electric buzzer. Buffering such as a transistor or logic gate is required between the Module SPKR pin and the audio transducer.

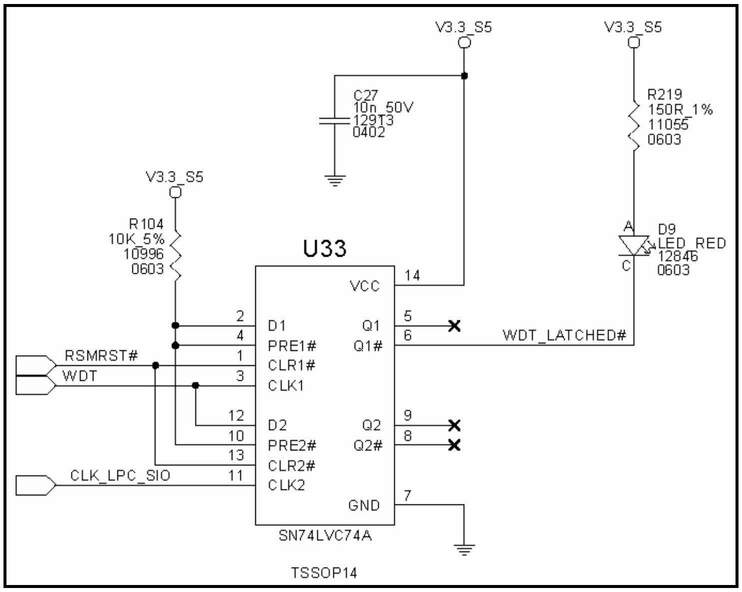
An example circuit is shown in Figure 18-1. The net SPKR is sourced from Module pin B32.

Figure 18-1: Speaker Out Schematic



18.2 Watchdog Timer

Figure 18-2: Watchdog Timer Event Latch Schematic

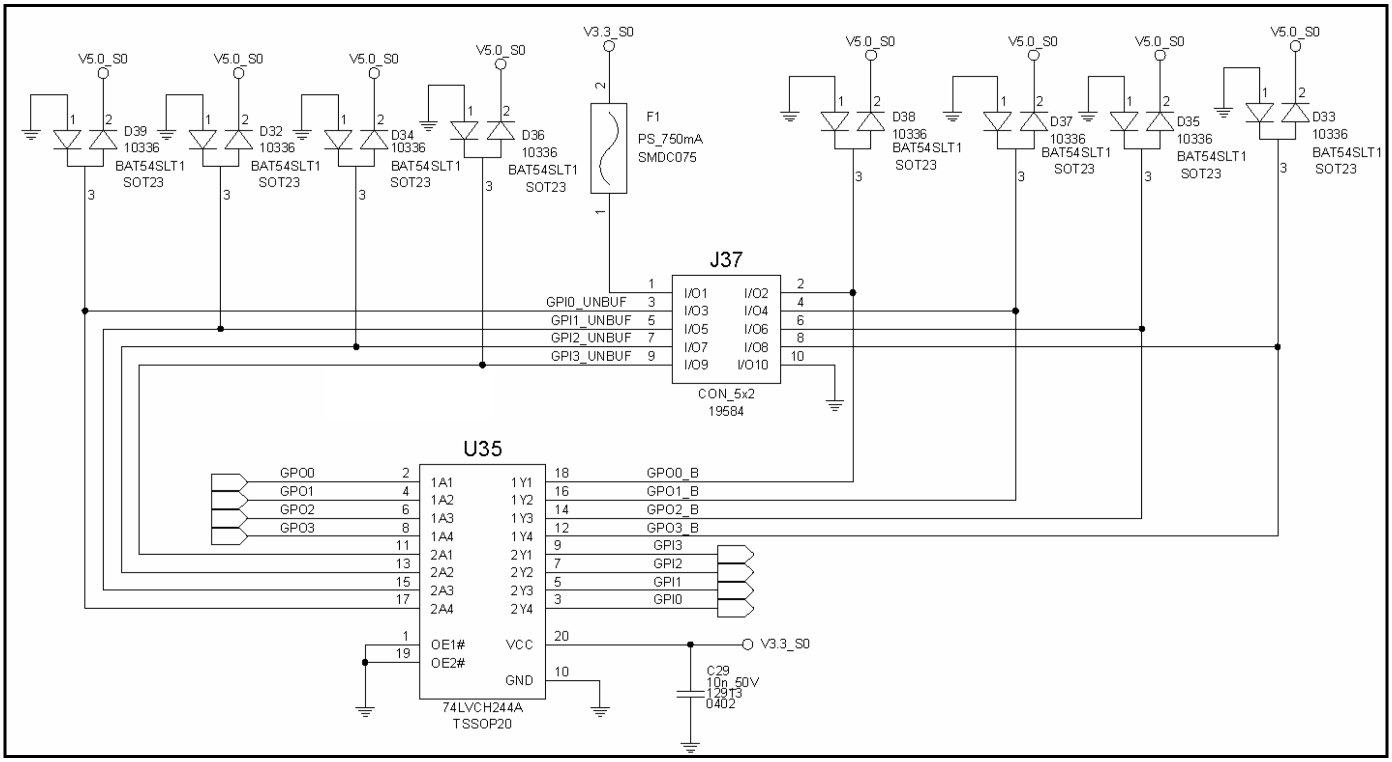


The following applies to Figure 18-2 above.

- The Watchdog Timer (WDT) event signal is provided from the ETXexpress Module. The WDT output is active-high. It is sourced from Module pin B27.
- The WDT event can cause the system to reset by making appropriate Carrier Board connections. It also may be possible to configure the Module to reset on a WDT event; check the relevant ETXexpress Module User Guide.
- If the WDT output is used to cause a system reset, the WDT output will be cleared by the system reset event.
- The WDT can be latched to drive a LED for a visual indication of an event, as shown in this example. Note that the latch is powered by a power rail that is active in all power states, including the soft-off state. The latch is only cleared by a complete power cycle. The cold power-up cycle is signaled by the RSMRST# net (Resume Reset, active low). A Carrier Board reset monitor, not shown in this figure, is required to generate the RSMRST# signal. The reset monitor should monitor the 5V or 3.3V standby power rail (V5.0_S5 or V3.3_S5).

18.3 General Purpose I/O

Figure 18-3: General Purpose I/O Loop-back Schematic



The following notes apply to Figure 18-3 above.

- There are 4 GPI (General Purpose Inputs) and 4 GPO (General Purpose Outputs) pins in Figure 18-3 above.
- The signals drive switch inputs such as Lamps, Relays, and Sensors.
- GPI signals from a header are shown with protection diodes. The signals are connected for input to the ETXexpress Module.
- GPO signals from the ETXexpress Module are shown buffered. The signals are connected to the header with protection diodes.

19 Power and Reset

19.1 Power, Power State and Reset – Signal Definitions

Power is delivered to an ETXexpress Module through a set of +12V power input pins. For Type 2,3,4 and 5 modules, there are 33 pins dedicated to +12V power in, and there are 64 ground return pins. This ensures that adequate power for very high-performance systems can be brought into the Module – up to 188W.

For Type 1 modules, there are fewer pins available for power input, but there is still plenty of capacity. A Type 1 module allocates 21 pins for +12V in and 27 ground return pins. This allows up to 120W of power to be delivered to the Type 1 Module.
Refer to the COM Express™ Specification, Section 7.2, for more details.

In addition to the +12V power-input pins, the COM Express™ Specification allocates four pins for +5V standby power, and one pin for RTC / CMOS parameter RAM battery power for all Modules.

The intent of the COM Express™ specification is for all Modules to run from +12V only, except for standby and RTC / CMOS backup functions. If standby functions are not required, then the +5V standby input should not be needed. In practice, some early Module implementations may not start up correctly without the presence of the +5V standby input. Check the relevant ETXexpress Module User Guide and / or with a Kontron FAE.

A number of other signals are involved in power delivery to the Module. These include the suspend-status outputs from the Module, SUS_S5#, SUS_S4# , SUS_S3# and SUS_STAT# ; external power status input to the Module, PWR_OK ; a reset-input signal to the Module, SYSRESET# ; various reset outputs from the Module, including CB_RESET#, PCI_RESET# and IDE_RESET# ; and a PWRBTN# input to the Module to allow “soft” power control.

The BATLOW# input signal may be supported on the Module to signal a low-battery condition to the Module, and the SM Bus is available for support functions such as a Smart Battery interface. Finally, the THRM# signal is an optional Module input that signals a Carrier Board over temperature condition to the Module. The THRMTRIP# Module output indicates a thermal fault condition on the Module to hardware on the Carrier Board.

The pin-out information for these signals can be found in Table 19-1 below, as well as in the COM Express™ Specification. The table shows all signals for a Type 2 Module. The majority of the signals discussed in this section are present in all Module Types. The use of most of these signals is illustrated in various examples below.

Table 19-1: Power, Power State and Reset Signals (Bold)

Row A		Row B		Row C		Row D	
A1	**GND (FIXED)**	**B1**	**GND (FIXED)**	**C1**	**GND (FIXED)**	**D1**	**GND (FIXED)**
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	IDE_D7	D2	IDE_D5
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	IDE_D6	D3	IDE_D10
A4	GBE0_LINK100#	B4	LPC_AD0	C4	IDE_D3	D4	IDE_D11
A5	GBE0_LINK1000#	B5	LPC_AD1	C5	IDE_D15	D5	IDE_D12
A6	GBE0_MDI2-	B6	LPC_AD2	C6	IDE_D8	D6	IDE_D4
A7	GBE0_MDI2+	B7	LPC_AD3	C7	IDE_D9	D7	IDE_D0
A8	GBE0_LINK#	B8	LPC_DRQ0#	C8	IDE_D2	D8	IDE_REQ
A9	GBE0_MDI1-	B9	LPC_DRQ1#	C9	IDE_D13	D9	IDE_IOW#
A10	GBE0_MDI1+	B10	LPC_CLK	C10	IDE_D1	D10	IDE_ACK#
A11	**GND (FIXED)**	**B11**	**GND (FIXED)**	**C11**	**GND (FIXED)**	**D11**	**GND (FIXED)**
A12	GBE0_MDI0-	**B12**	**PWRBTN#**	C12	IDE_D14	D12	IDE_IRQ
A13	GBE0_MDI0+	**B13**	**SMB_CK**	C13	IDE_IORDY	D13	IDE_A0
A14	GBE0_CTREF	**B14**	**SMB_DAT**	C14	IDE_IOR#	D14	IDE_A1
A15	**SUS_S3#**	**B15**	**SMB_ALERT#**	C15	PCI_PME#	D15	IDE_A2
A16	SATA0_TX+	B16	SATA1_TX+	C16	PCI_GNT2#	D16	IDE_CS1#
A17	SATA0_TX-	B17	SATA1_TX-	C17	PCI_REQ2#	D17	IDE_CS3#
A18	**SUS_S4#**	**B18**	**SUS_STAT#**	C18	PCI_GNT1#	**D18**	**IDE_RESET#**
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCI_REQ1#	D19	PCI_GNT3#
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCI_GNT0#	D20	PCI_REQ3#
A21	**GND (FIXED)**	**B21**	**GND (FIXED)**	**C21**	**GND (FIXED)**	**D21**	**GND (FIXED)**
A22	SATA2_TX+	B22	SATA3_TX+	C22	PCI_REQ0#	D22	PCI_AD1
A23	SATA2_TX-	B23	SATA3_TX-	**C23**	**PCI_RESET#**	D23	PCI_AD3
A24	**SUS_S5#**	**B24**	**PWR_OK**	C24	PCI_AD0	D24	PCI_AD5
A25	SATA2_RX+	B25	SATA3_RX+	C25	PCI_AD2	D25	PCI_AD7
A26	SATA2_RX-	B26	SATA3_RX-	C26	PCI_AD4	D26	PCI_C/BE0#
A27	**BATLOW#**	B27	WDT	C27	PCI_AD6	D27	PCI_AD9
A28	ATA_ACT#	B28	AC_SDIN2	C28	PCI_AD8	D28	PCI_AD11
A29	AC_SYNC	B29	AC_SDIN1	C29	PCI_AD10	D29	PCI_AD13
A30	AC_RST#	B30	AC_SDIN0	C30	PCI_AD12	D30	PCI_AD15
A31	**GND (FIXED)**	**B31**	**GND (FIXED)**	**C31**	**GND (FIXED)**	**D31**	**GND (FIXED)**
A32	AC_BITCLK	B32	SPKR	C32	PCI_AD14	D32	PCI_PAR
A33	AC_SDOUT	B33	I2C_CK	C33	PCI_C/BE1#	D33	PCI_SERR#
A34	BIOS_DISABLE#	B34	I2C_DAT	C34	PCI_PERR#	D34	PCI_STOP#
A35	**THRMTRIP#**	**B35**	**THRM#**	C35	PCI_LOCK#	D35	PCI_TRDY#
A36	USB6-	B36	USB7-	C36	PCI_DEVSEL#	D36	PCI_FRAME#
A37	USB6+	B37	USB7+	C37	PCI_IRDY#	D37	PCI_AD16
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	PCI_C/BE2#	D38	PCI_AD18
A39	USB4-	B39	USB5-	C39	PCI_AD17	D39	PCI_AD20
A40	USB4+	B40	USB5+	C40	PCI_AD19	D40	PCI_AD22
A41	**GND (FIXED)**	**B41**	**GND (FIXED)**	**C41**	**GND (FIXED)**	**D41**	**GND (FIXED)**
A42	USB2-	B42	USB3-	C42	PCI_AD21	D42	PCI_AD24
A43	USB2+	B43	USB3+	C43	PCI_AD23	D43	PCI_AD26
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	PCI_C/BE3#	D44	PCI_AD28
A45	USB0-	B45	USB1-	C45	PCI_AD25	D45	PCI_AD30
A46	USB0+	B46	USB1+	C46	PCI_AD27	D46	PCI_IRQC#
A47	**VCC_RTC**	**B47**	**EXCD1_PERST#**	C47	PCI_AD29	D47	PCI_IRQD#
A48	**EXCD0_PERST#**	B48	EXCD1_CPPE#	C48	PCI_AD31	D48	PCI_CLKRUN#
A49	EXCD0_CPPE#	**B49**	**SYS_RESET#**	C49	PCI_IRQA#	D49	PCI_M66EN
A50	LPC_SERIRQ	**B50**	**CB_RESET#**	C50	PCI_IRQB#	D50	PCI_CLK
A51	**GND (FIXED)**	**B51**	**GND (FIXED)**	**C51**	**GND (FIXED)**	**D51**	**GND (FIXED)**
A52	PCIE_TX5+	B52	PCIE_RX5+	C52	PEG_RX0+	D52	PEG_TX0+
A53	PCIE_TX5-	B53	PCIE_RX5-	C53	PEG_RX0-	D53	PEG_TX0-
A54	GPI0	B54	GPO1	**C54**	**TYPE0#**	D54	PEG_LANE_RV#
A55	PCIE_TX4+	B55	PCIE_RX4+	C55	PEG_RX1+	D55	PEG_TX1+

Row A			Row B			Row C			Row D	
A56	PCIE_TX4-		B56	PCIE_RX4-		C56	PEG_RX1-		D56	PEG_TX1-
A57	**GND**		B57	GPO2		**C57**	**TYPE1#**		**D57**	**TYPE2#**
A58	PCIE_TX3+		B58	PCIE_RX3+		C58	PEG_RX2+		D58	PEG_TX2+
A59	PCIE_TX3-		B59	PCIE_RX3-		C59	PEG_RX2-		D59	PEG_TX2-
A60	**GND (FIXED)**		**B60**	**GND (FIXED)**		**C60**	**GND (FIXED)**		**D60**	**GND (FIXED)**
A61	PCIE_TX2+		B61	PCIE_RX2+		C61	PEG_RX3+		D61	PEG_TX3+
A62	PCIE_TX2-		B62	PCIE_RX2-		C62	PEG_RX3-		D62	PEG_TX3-
A63	GPI1		B63	GPO3		C63	RSVD		D63	RSVD
A64	PCIE_TX1+		B64	PCIE_RX1+		C64	RSVD		D64	RSVD
A65	PCIE_TX1-		B65	PCIE_RX1-		C65	PEG_RX4+		D65	PEG_TX4+
A66	**GND**		B66	WAKE0#		C66	PEG_RX4-		D66	PEG_TX4-
A67	GPI2		B67	WAKE1#		C67	RSVD		**D67**	**GND**
A68	PCIE_TX0+		B68	PCIE_RX0+		C68	PEG_RX5+		D68	PEG_TX5+
A69	PCIE_TX0-		B69	PCIE_RX0-		C69	PEG_RX5-		D69	PEG_TX5-
A70	**GND (FIXED)**		**B70**	**GND (FIXED)**		**C70**	**GND (FIXED)**		**D70**	**GND (FIXED)**
A71	LVDS_A0+		B71	LVDS_B0+		C71	PEG_RX6+		D71	PEG_TX6+
A72	LVDS_A0-		B72	LVDS_B0-		C72	PEG_RX6-		D72	PEG_TX6-
A73	LVDS_A1+		B73	LVDS_B1+		C73	SDVO_DATA		D73	SDVO_CLK
A74	LVDS_A1-		B74	LVDS_B1-		C74	PEG_RX7+		D74	PEG_TX7+
A75	LVDS_A2+		B75	LVDS_B2+		C75	PEG_RX7-		D75	PEG_TX7-
A76	LVDS_A2-		B76	LVDS_B2-		**C76**	**GND**		**D76**	**GND**
A77	LVDS_VDD_EN		B77	LVDS_B3+		C77	RSVD		D77	IDE_CBLID#
A78	LVDS_A3+		B78	LVDS_B3-		C78	PEG_RX8+		D78	PEG_TX8+
A79	LVDS_A3-		B79	LVDS_BKLT_EN		C79	PEG_RX8-		D79	PEG_TX8-
A80	**GND (FIXED)**		**B80**	**GND (FIXED)**		**C80**	**GND (FIXED)**		**D80**	**GND (FIXED)**
A81	LVDS_A_CK+		B81	LVDS_B_CK+		C81	PEG_RX9+		D81	PEG_TX9+
A82	LVDS_A_CK-		B82	LVDS_B_CK-		C82	PEG_RX9-		D82	PEG_TX9-
A83	LVDS_I2C_CK		B83	LVDS_BKLT_CTRL		C83	RSVD		D83	RSVD
A84	LVDS_I2C_DAT		**B84**	**VCC_5V_SBY**		**C84**	**GND**		**D84**	**GND**
A85	GPI3		**B85**	**VCC_5V_SBY**		C85	PEG_RX10+		D85	PEG_TX10+
A86	KBD_RST#		**B86**	**VCC_5V_SBY**		C86	PEG_RX10-		D86	PEG_TX10-
A87	KBD_A20GATE		**B87**	**VCC_5V_SBY**		**C87**	**GND**		**D87**	**GND**
A88	PCIE0_CK_REF+		B88	RSVD		C88	PEG_RX11+		D88	PEG_TX11+
A89	PCIE0_CK_REF-		B89	VGA_RED		C89	PEG_RX11-		D89	PEG_TX11-
A90	**GND (FIXED)**		**B90**	**GND (FIXED)**		**C90**	**GND (FIXED)**		**D90**	**GND (FIXED)**
A91	RSVD		B91	VGA_GRN		C91	PEG_RX12+		D91	PEG_TX12+
A92	RSVD		B92	VGA_BLU		C92	PEG_RX12-		D92	PEG_TX12-
A93	GPO0		B93	VGA_HSYNC		**C93**	**GND**		**D93**	**GND**
A94	RSVD		B94	VGA_VSYNC		C94	PEG_RX13+		D94	PEG_TX13+
A95	RSVD		B95	VGA_I2C_CK		C95	PEG_RX13-		D95	PEG_TX13-
A96	**GND**		B96	VGA_I2C_DAT		**C96**	**GND**		**D96**	**GND**
A97	**VCC_12V**		B97	TV_DAC_A		C97	RSVD		D97	PEG_ENABLE#
A98	**VCC_12V**		B98	TV_DAC_B		C98	PEG_RX14+		D98	PEG_TX14+
A99	**VCC_12V**		B99	TV_DAC_C		C99	PEG_RX14-		D99	PEG_TX14-
A100	**GND (FIXED)**		**B100**	**GND (FIXED)**		**C100**	**GND (FIXED)**		**D100**	**GND (FIXED)**
A101	**VCC_12V**		**B101**	**VCC_12V**		C101	PEG_RX15+		D101	PEG_TX15+
A102	**VCC_12V**		**B102**	**VCC_12V**		C102	PEG_RX15-		D102	PEG_TX15-
A103	**VCC_12V**		**B103**	**VCC_12V**		**C103**	**GND**		**D103**	**GND**
A104	**VCC_12V**		**B104**	**VCC_12V**		**C104**	**VCC_12V**		**D104**	**VCC_12V**
A105	**VCC_12V**		**B105**	**VCC_12V**		**C105**	**VCC_12V**		**D105**	**VCC_12V**
A106	**VCC_12V**		**B106**	**VCC_12V**		**C106**	**VCC_12V**		**D106**	**VCC_12V**
A107	**VCC_12V**		**B107**	**VCC_12V**		**C107**	**VCC_12V**		**D107**	**VCC_12V**
A108	**VCC_12V**		**B108**	**VCC_12V**		**C108**	**VCC_12V**		**D108**	**VCC_12V**
A109	**VCC_12V**		**B109**	**VCC_12V**		**C109**	**VCC_12V**		**D109**	**VCC_12V**
A110	**GND (FIXED)**		**B110**	**GND (FIXED)**		**C110**	**GND (FIXED)**		**D110**	**GND (FIXED)**

19.2 Power, Power State and Reset – Routing Considerations

19.2.1 VCC_12V and GND

The primary consideration for the +12V power input (VCC_12V) to the Module is that the trace be wide enough to handle the maximum expected load, with plenty of margin. A power plane may be used for VCC_12V but is not recommended; VCC_12V should not be used as a reference for high-speed signals, such as PCIe, USB, or even PCI, because there may be switching noise present on VCC_12V.

A 40W CPU Module can draw over 3A on the VCC_12V pins. Sizing the VCC_12V delivery trace to handle at least twice the expected load is recommended for good design margin. It is best to keep the Carrier Board VCC_12 trace short, wide, and away from other parts of the Carrier Board. See the following section for advice on how to size the trace.

If there are layer transitions in the power delivery path, use redundant “power” vias – vias that are sized with larger holes and pads than default vias.

For the GND return, it is best to use a solid, continuous plane, or multiple planes, using the heaviest possible copper.

It is very important to connect all available power and ground pins available on the ETXexpress Module to the Carrier Board.

19.2.2 Copper Trace Sizing and Current Capacity

The current capacity of a PCB trace is proportional to the trace's cross-sectional area – the product of the trace width and thickness. The trace thickness is proportional to the "weight" of copper used. The copper weight is expressed in ounces per square foot in the United States. Usually people will omit the "per square foot" and just use "ounce" to describe the copper. Copper weights of ½ ounce and sometimes 1 ounce are common for inner layer traces. A copper weight of 1 ounce is common for power planes. A copper weight of ½ ounce results in a thickness of approximately 0.0007 inches, and 1 ounce copper yields approximately 0.0014 inches. Outer layer traces are usually built with ½ ounce copper, but then are "plated up" with additional conductive material, often yielding an effective copper weight of about 1 ounce. The effective weight of outer layer traces may vary with different PCB processes. Check with your PCB vendor, or play it safe and make conservative assumptions.

Consult sources such as the IPC-2221 (see Appendix G for reference) for charts that relate copper weight, trace width and trace-current capacity at a given temperature rise to the current capability. It is best to assume a conservative trace temperature rise, such as 10 °C maximum, when making trace-width decisions. Per the IPC charts, external layer traces can carry significantly more current than internal layer traces, assuming the same base copper weight and the same temperature rise. Approximate current handling capabilities of selected trace widths read off of the IPC-2221 charts are shown in Table 19-2 below.

Table 19-2: Approximate Copper Trace Current Capability per IPC-2221 Charts

Trace Type	Max Current with 10 °C Rise	Max Current With 20 °C Rise
100 mil wide internal trace ½ ounce base copper	1.3 A	1.8 A
200 mil wide internal trace ½ ounce base copper	2.0 A	3.0 A
400 mil wide internal trace ½ ounce base copper	3.5 A	5.0 A
100 mil wide internal trace 1 ounce base copper	2.1 A	3.0 A
200 mil wide internal trace 1 ounce base copper	3.5 A	5.2 A
400 mil wide internal trace 1 ounce base copper	6.0 A	8.0 A
100 mil wide external trace ½ ounce base copper	2.4 A	3.4 A
200 mil wide external trace ½ ounce base copper	4.0 A	5.5 A
400 mil wide external trace ½ ounce base copper	7.0 A	10 A

19.2.3 VCC5_SBY Routing

The +5V standby power rail, if used, should be sized to handle 2A. Most, but not all, Modules will use considerably less than 2A for this power rail. Modules with multiple Ethernet channels and wake-on-LAN capability will use more current. The COM Express™ Specification allows up to 2A on this rail.

19.2.4 VCC_RTC_Routing

The current requirements for VCC_RTC are very modest (usually well under 20 microamperes), so trace width is not an issue. However, sometimes leakage is an issue, and it is a good idea to have generous spacing between components in the path between the RTC backup battery and the Module VCC_RTC pins.

19.2.5 Power State and Reset Signal Routing

Power state and reset signals are single-ended signals that do not have any particular routing constraints. The routing guidelines for single-ended signals in Appendix B may be used.

19.3 ATX Power Supplies

19.3.1 ATX Power Supply

ATX power supplies are used in millions of desktop PCs and are often used in OEM equipment as well. They are cheap and are readily available. An ATX power supply provides more power rails (two separate +12V rails, +5V, +3.3V, -12V and +5V standby) than are required by an ETXexpress Module, but often the Carrier Board and other system components make use of the additional rails. ATX power-supply specifications are fully described in an Intel document titled *ATX12V Power Supply Design Guide*. This document is easily obtained from the www.formfactors.org Web site. If you are using an ATX power supply, it is worthwhile to obtain this document.

Table 19-3: ATX Power Supply Signal Summary

ATX Signal Name	Description
PS_ON#	Active-low, TTL-level input to ATX supply that, when low, enables all power rails. If high or floating, all ATX power rails are disabled except for the +5V standby rail.
PWR_OK	Active-high, TTL-level output signal from the ATX supply that indicates that the +12V, +3.3V and +5V outputs are all present and OK to use.
+12V1DC	+12V power rail for use by all system components except for the CPU, controlled by PS_ON#
+12V2DC	+12V power rail for use by the CPU, controlled by PS_ON#. This power rail appears on a separate 2x2 connector for CPU use only.
+5VDC	+5V power rail, controlled by PS_ON#
+3.3VDC	+3.3V power rail, controlled by PS_ON#
-12VDC	-12V power rail, controlled by PS_ON#
+5VSB	+5V standby power rail, present whenever the ATX supply is connected to its AC power input source.
COM	Common return path – usually referred to as “ground” or GND.

ATX signals are summarized in Table 19-3 above. Note that there are two separate +12V outputs, +12V1DC and +12V2DC. These are independent +12V sources. Each source is limited to 240W maximum output to meet U.L. safety requirements. The +12V2DC output is intended for CPU use.

Contemporary ATX supplies have two power connectors on the motherboard:

- A 24-pin connector in a 2x12 array that includes all signals in Table 19-2 except for +12V2DC.
- A 4-pin connector in a 2x2 array for CPU power that includes +12V2DC and COM only.

Earlier ATX supplies used a 2x10 connector instead of a 2x12. The two connector versions have compatible pin-outs. The 2x10 cable plug may be used with a 2x12 motherboard receptacle as long as pin 1 of the 2x10 cable plug mates with pin 1 of the 2x12 Carrier Board receptacle.

Very early ATX supplies had a single +12V rail, on a 2x10 connector. The 2x2 CPU connector was not present.

ATX power supplies are designed for desktop systems, which often have power-hungry CPUs and peripherals. CPUs that require 80W are common. Most Modules use lower-power CPUs, and the ATX supply capacity may be overkill. In particular, two +12V supplies are not necessary for many ETXexpress Modules. The Brownsville ETXexpress eval Carrier Board uses two +12V supplies and has a resistor option to allow a single +12V supply if desired.

19.3.2 ATX Supply Minimum Loads

ATX supplies may not start up if the loading on the +12V, +5V and +3.3V rails is too light. The ***ATX12V Power Supply Design Guide*** shows suggested minimum loads in various configurations but does not specify what the minimum loads shall be. The minimum loads required may vary with different power supply vendors.

Experience has shown that a dummy load on the order of at least 400 mA is required on the +5V line in ETXexpress Carrier Boards that use little or no +5V and are powered from ATX supplies.

19.4 Power, Power State and Reset – Reference Schematics

19.4.1 ATX Power Connector

The ATX 2x12 Main Power Connector is diagrammed in Figure 19-1 below. The ATX 2x2 CPU (Auxiliary) Power Connector is shown in Figure 19-2 below. Three options control the power:

- The most straightforward control method is to invert Module signal SUS_S5# through an open drain buffer, with a pull-up to VCC5_SBY (standby +5V), and connect this to the ATX PS_ON# pin (pin 4 on the ATX 2x12 connector).
  - If R23 is installed and R24 is open in Figure 19-1, then net WM_PSON# from a discrete logic source controls the power supply. This net is created from one or more of the following Module signals: SUS_S5#, SUS_S4#, SUS_S3#, TYPE2#, TYPE1# or TYPE0#.
  - The use of an open drain buffer is advised because it allows you to force the ATX PS_ON# pin low for debug purposes.
- Sometimes the ATX PS_ON# pin is driven by the Super I/O to facilitate features such as wake on PS2 keyboard or mouse activity. In this case, the Module suspend state (SUS_S5#, SUS_S4# or SUS_S3#) is factored into the logic, usually as a Super I/O input designated for this purpose.
  - If R24 is installed and R23 is open in Figure 19-1, then SIO_PSON# from the Super I/O controls the power supply. (See also the Super I/O drawing in Figure 16-3).
- The ATX PS_ON# pin can be tied low to always enable the ATX supply. This is a jumper option in Figure 19-1.
  - This results in the soft turn-on not being used.
  - The AC power input starts the power supply.
  - This is useful for system debug.
- The ATX PWR_OK signal may be routed to the Module PWR_OK signal (Module pin B24).

Figure 19-2 below illustrates the 2x2 ATX connector used for +12V power to the ETXexpress Module. The option resistors in the figure, R256 and R257, are usually left open. If an older ATX supply provides only a single +12V source, then the resistors can be loaded to connect the separate +12V nets into a single net.

Figure 19-1: ATX 2x12 Main Power Connector Schematic

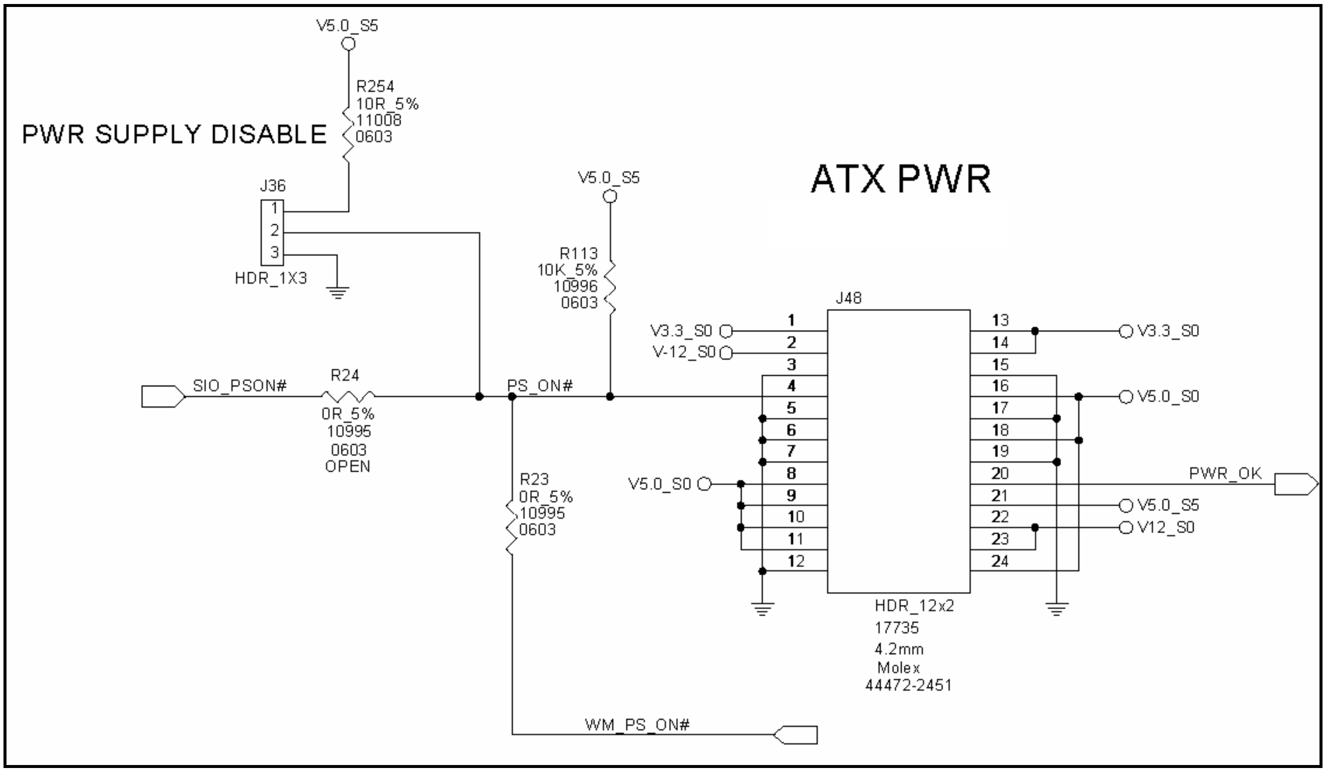
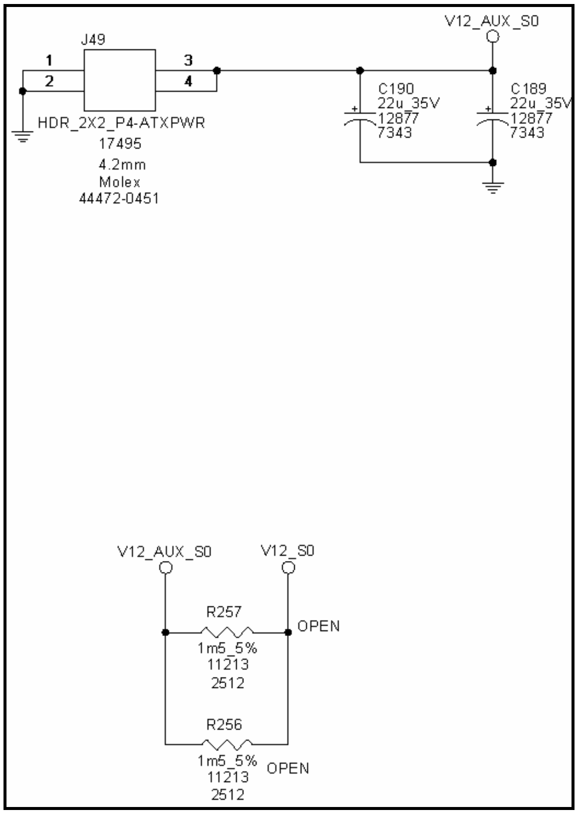


Figure 19-2: AUX 2x2 CPU (Auxiliary) Power Connector Schematic



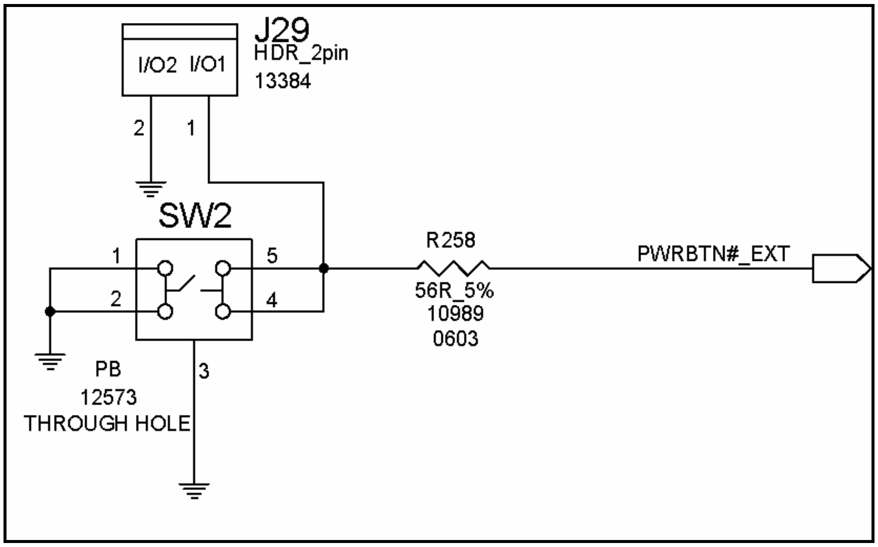
19.4.2 System PWR ON/OFF

Module pin B12, with signal name PWRBTN#, is intended for direct connection to a power button switch, as shown in Figure 19-3 below. Switch SW2 is mounted on the PCB. Header J29 allows a connection to a panel-mounted switch.

The Module PWRBTN# pin also may be driven by a logic signal from a Super I/O or another source.

On the Module, the PWRBTN# signal is routed to chipset logic that is powered by the standby power rail, VCC5_SBY. A low pulse on the PWRBTN# causes transitions in and out of the soft-off state (S5).

Figure 19-3: System PWR ON/OFF Schematic



19.4.3 Module-Type Detection

The COM Express™ Specification includes three Module pins that signal the Module pin-out Type to the Carrier Board. The Type2#, Type1#, and Type0# pins are either left open or are strapped to GND on the Module, per Table 19-4 below.

A Carrier Board may optionally decode the Module Type pins and delay powering up the Carrier Board and Module if the Module Type does not match the Type expected by the Carrier Board.

Table 19-4: Module-Type Encoding

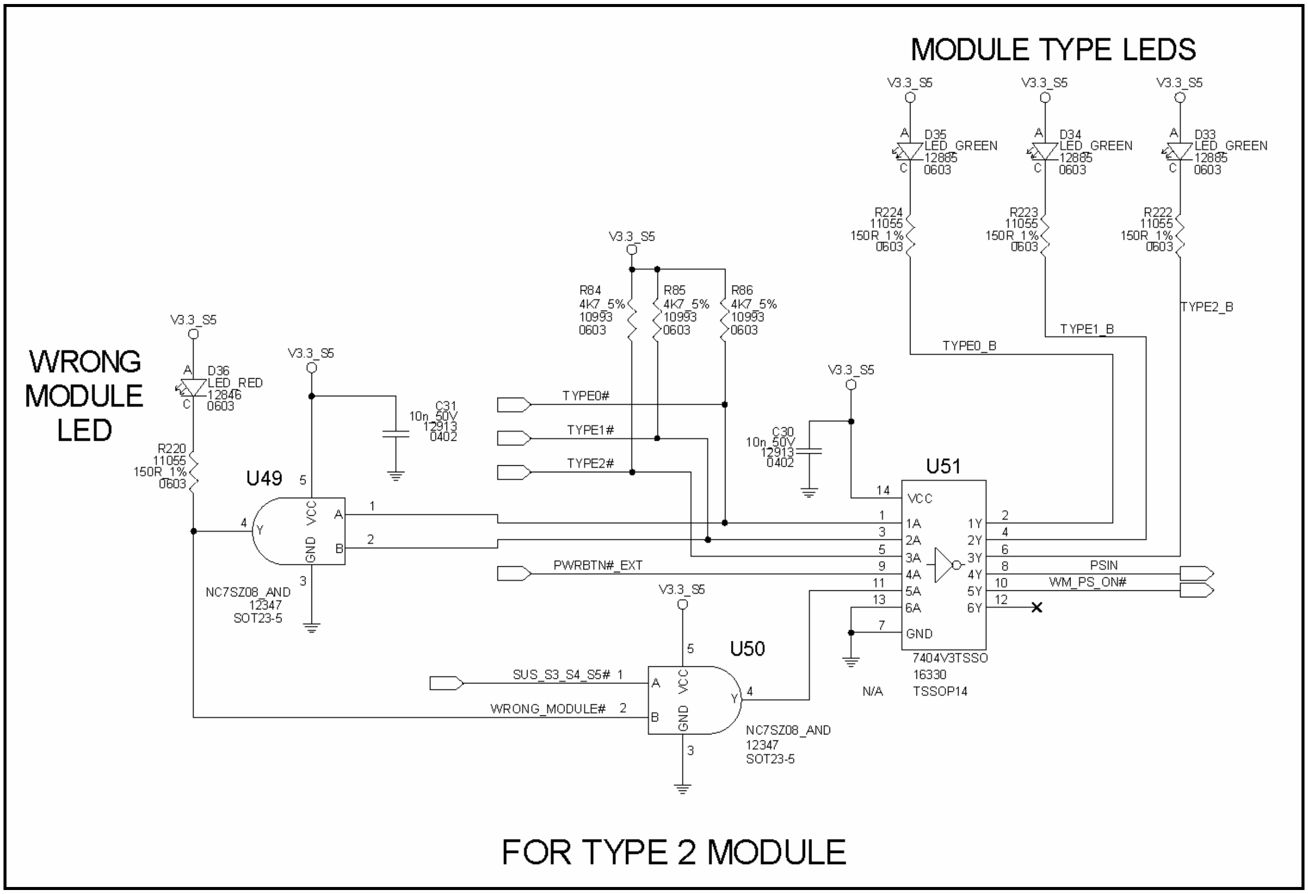
X ='s "Don't Care"

TYPE2# Pins	TYPE1# Pins	TYPE0# Pins	Pin-out Type
X	X	X	Pin-out Type 1
NC	NC	NC	Pin-out Type 2
NC	NC	GND	Pin-out Type 3 (no IDE)
NC	GND	NC	Pin-out Type 4 (no PCI)
NC	GND	GND	Pin-out Type 5 (no IDE or PCI)

A sample schematic for a Carrier Board, Module-Type detection implementation is shown in Figure 19-4 below.

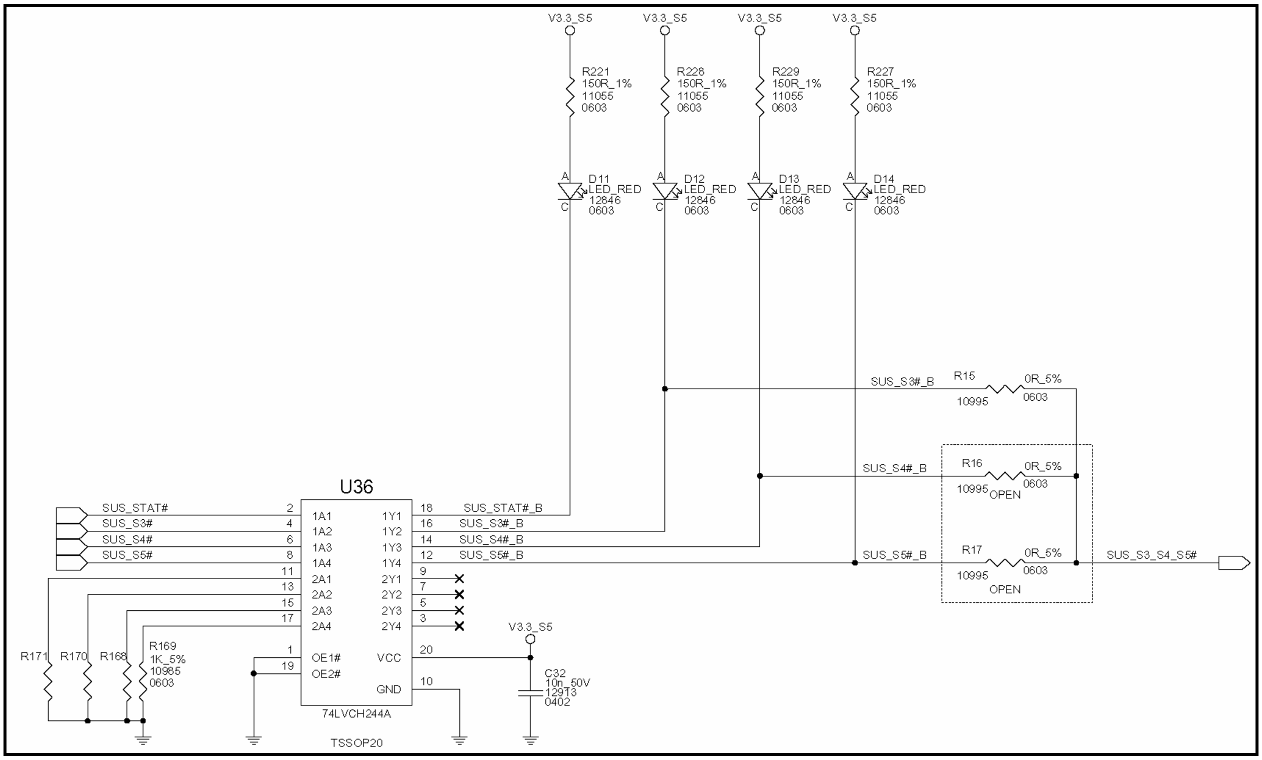
- TYPE[0:2]# are sourced from ETXexpress Module pins C54, C57, D57 respectively.
- The TYPE signals are given pull-ups to V3.3_S5 (standby +3.3V power rail) in this example. They are routed to type detection logic (U49) and to an inverter (U51) that drives LEDs to indicate signal status.
- The TYPE pins could alternatively be pulled up to V5.0_S5 (standby +5V power rail, direct from ATX supply) if the Carrier Board logic can tolerate it. The Module does not care as the TYPE pins are tied either to GND or are left NC on the Module.
- The following example shows what occurs when a Type 2 Module is inserted into an ETXexpress Carrier Board.
  - Signals TYPE0# and TYPE1# are AND'd (U49) to produce a high output for Type 2.
  - This High enables SUS_S3_S4_S5# (U50) and causes a high output that is inverted (U51).
  - This then produces WM_PS_ON#, which eventually turns on the power supply.
  - WM_PS_ON# is inhibited for any other encoded states of TYPE signals, preventing the power supply from turning on.

Figure 19-4: Module-Detection Circuit Schematic



19.4.4 Sleep-State LEDs

Figure 19-5: Sleep-State LEDs Schematic



The following applies to Figure 19-5 above.

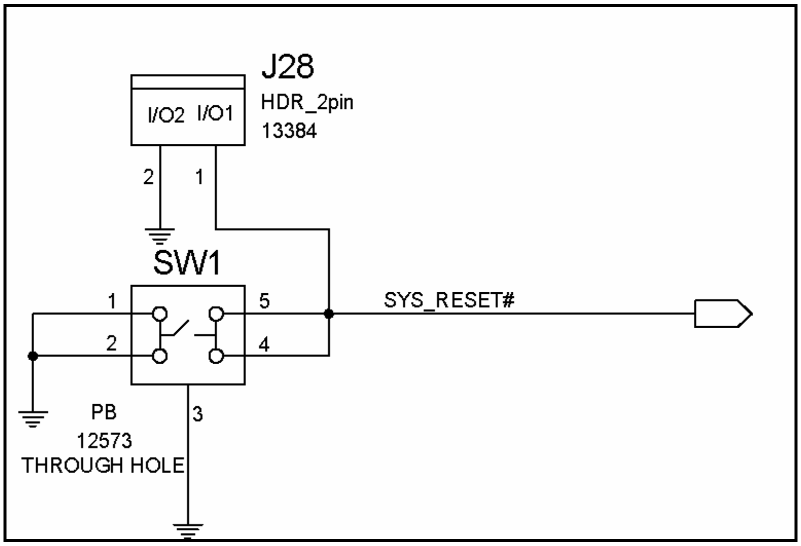
- Status LEDS are driven by Suspend State signals from the Module after buffering.
- Resistors R15, R16 and R17 allow options in picking which suspend state controls the ATX soft-off function. Only one of the 3 resistors should be loaded for a given build.
- Using SUS_S3# to control the ATX supply as shown in the figure is recommended.

19.4.5 System-Reset Input

The COM Express™ Specification allows for a system-reset input, named SYS_RESET# (Module pin B49), that may be connected to a Carrier Board reset switch, as shown in Figure 19-6 below. Header J28 in the figure allows for a connection to a panel-mount-reset switch.

Open drain Carrier Board logic also may drive this net. For example, the Module watchdog timer output could be inverted through an open drain buffer and tied into this net to cause a system reset on a watchdog timeout.

Figure 19-6: System-Reset Schematic



19.4.6 Module-Reset Outputs

The COM Express™ Specification defines five reset outputs from the Module. They are summarized in Table 19-5 below.

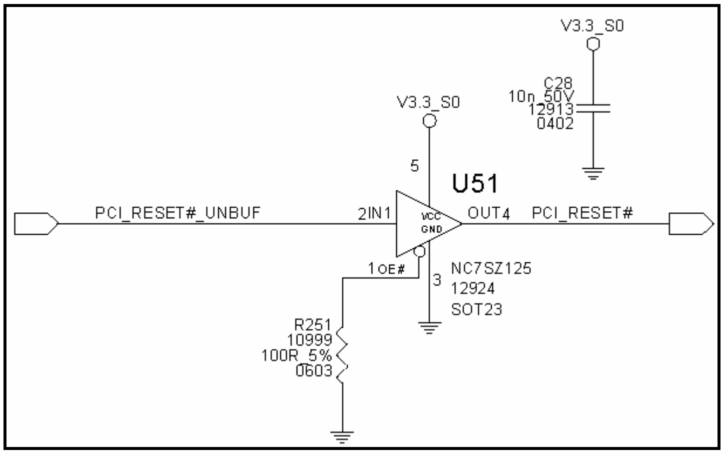
The CB_RESET# is the general-purpose reset output that exists for all Module Types. In some Modules, including the Kontron ETXexpress-PM module, CB_RESET# and PCI_RESET# are the same signal on the Module.

If the Module reset output drives many Carrier Board devices, it should be buffered. An example is shown in Figure 19-7 below.

Table 19-5: Module-Reset Outputs

Module Signal Name	Module Pin	Function	Module Types
CB_RESET#	B50	General purpose active low reset signal from the Module to the Carrier Board. May be used for LPC and other devices.	All Types
IDE_RESET#	D18	Active low reset signal from the Module to Carrier Board IDE devices.	Types 2,4
PCI_RESET#	C23	Active low reset signal from the Module to Carrier Board PCI devices. May also be used for LPC devices.	Types 2,3
EXCD0_PERST#	A48	Active low reset signal from the Module to an Carrier Board Express Card slot 0.	All Types
EXCD1_PERST#	B47	Active low reset signal from the Module to an Carrier Board Express Card slot 1.	All Types

Figure 19-7: PCI Reset Buffer Schematic



19.4.7 RTC / CMOS Parameter Backup Battery

The COM Express™ Specification provides a pin for a +3.0V Carrier Board backup battery. The Module signal name is VCC_RTC, on Module pin A47. The battery provides backup power to the Module's RTC (real-time clock) and to the Module's CMOS parameter RAM that stores system setup and configuration in the absence of other power. Per the COM Express™ Specification, the allowed input voltage range of the battery, at the Module pin, is +2.0V to +3.3V.

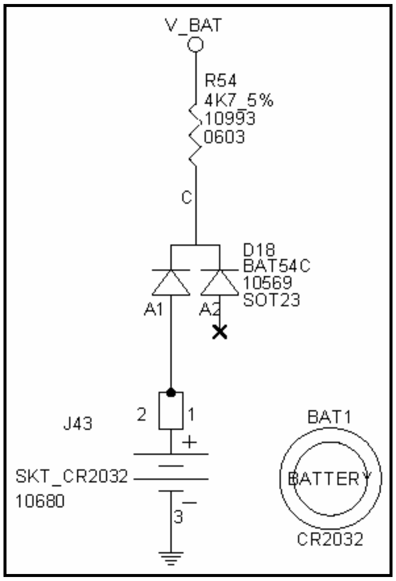
The type of battery used for the backup function is implementation-specific. The Module VCC_RTC current draw is usually very small, on the order of 20 μA or less. (Refer to the specific ETXexpress Module data sheet or ETXexpress Module chipset data sheet for an actual value). Typically a lithium coin cell battery is used. When this type of battery is used, the Carrier Board should implement protection components that prevent current from flowing into the lithium battery, as there is a safety concern. Per U.L. requirements, lithium batteries used for this type of application must be protected with either a series diode and a series resistor, or a pair of series diodes. The voltage drop across the protection components needs to be considered in the selection process.

An example of an implementation of an RTC backup battery on a Carrier Board, with protection components that are U.L. compliant, is shown below in Figure 19-8. The battery used in this example is a CR2032 lithium coin cell type, available from Panasonic and others. This device has a nominal output voltage of 3.0V and a capacity of 220 mAH. Assuming a Module has a VCC_RTC current draw of 10 μA, one can expect the RTC battery life to be about 22000 hours (220 mAH / 0.010 mA) or 2.5 years. Cells with larger capacities are available.

Not shown in the figure, but often advisable to include, is a jumper or other mechanism to ensure that the battery is not drained during storage on a warehouse shelf. This can be as simple as a series jumper that is in the open position during storage, or can rely on ICs that implement a "freshness seal" – a circuit that isolates the battery before its initial use. Circuits that incorporate the "freshness seal" often have the U.L. protective measures built into the IC.
Such devices are available from Maxim Semiconductor.

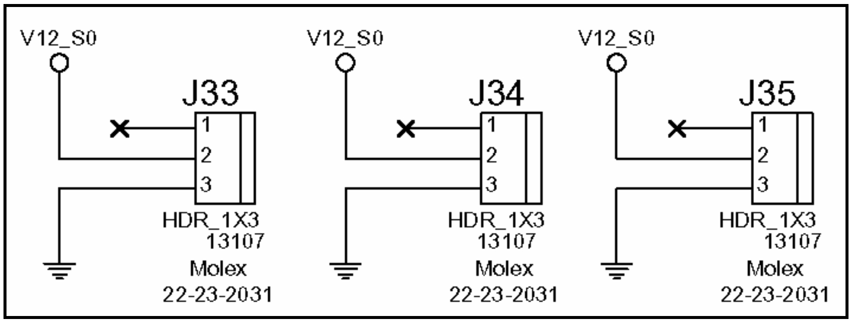
The backup battery may also be routed to other loads, such as a subsection of a Carrier Board Super I/O. These loads must be factored in when calculating the battery life.

Figure 19-8: Battery Schematic



19.4.8 Fan Header

Figure 19-9: Fan-Header Schematic



Connectors and connections typical for +12V cooling fans are shown in Figure 19-9 above. Pin 1 is often used for a fan-tachometer signal. There are no COM Express pins dedicated for use with fan-tachometer signals. Many Super I/Os provide support to read fan-tachometer signals. Smaller monitoring ICs from vendors such as National Semiconductor and Analog Devices are available to support fan-tachometer readings. The power to the fan is often gated through a FET to turn off the fan, in conjunction with a thermal sensor.

Some Module implementations that use small form factors have fan connectors to allow direct connection and control to cool the Module.

19.4.9 SM Bus

The SM (System Management) Bus is available on the Module A-B connector. The SM Bus should be approached with caution because it is used on the Module to set up and control many critical system functions, such as the Module clock synthesizer(s), the memory SPD (Serial Presence Detect), and thermal and voltage monitors. A Carrier Board fault on the SM Bus could prevent the Module from functioning. SM Bus support is a mandatory COM Express feature.

The SM Bus is essentially a dedicated I^2C bus, although unlike most I^2C buses, the SM Bus has an additional pin associated with it – an interrupt pin named SMB_ALERT#. This pin may be used to notify the system of critical events such as a low battery or an over-temperature condition.

The SM Bus is an integral part of the Smart Battery specification. References to the SM Bus, I^2C Bus, and Smart Battery source specifications may be found in Appendix G.

20 BIOS Considerations

20.1 Legacy Vs. Legacy Free

The COM Express™ Specification was formulated as a legacy-free specification; there is no requirement for a PS2 mouse or keyboard controller on an ETXexpress Module. However, a surprising body of older application code and some operating systems require access to a keyboard controller. If you are building a legacy-free system (a system without a PS2 keyboard or mouse controller on the Carrier Board or Module,) then it is important that the Module BIOS support legacy-free operation. In a legacy-free BIOS, accesses to the keyboard controller are intercepted and an appropriate response is emulated. A given Module may have a BIOS that can detect and adjust to the presence or absence of a keyboard controller. It is more likely that there are separate BIOS versions for legacy and legacy-free operation. Check the relevant ETXexpress Module User Guide and with your Kontron FAE.

There are a few hardware provisions in the COM Express™ Specification to support Carrier Board-based controllers for keyboards; Module signals KBD_RST# (pin A86) and KBD_A20GATE (pin A87) are Module inputs that allow an optional Carrier Board keyboard controller to interface to a Module. These Carrier Board keyboard controllers are most often integrated into a Super I/O.

20.2 Carrier Board Super I/O Support

A Carrier Board Super I/O implementation usually requires BIOS customization to support the Super I/O. If the Carrier Board uses the same Super I/O as the Kontron reference boards, then it may be possible to use the standard legacy BIOS that goes with the particular Module. One Super I/O that is supported in several Kontron ETXexpress BIOS implementations is the Winbond W83627HFJ. Check the relevant ETXexpress User Guide and with your Kontron FAE.

20.3 CMOS / Serial EEPROM Parameter Backup

Kontron Modules have on-Module serial EEPROMs that keep a non-volatile copy of the CMOS parameter RAM contents. All setup screen parameters except for the current date and time can be backed up in the serial EEPROM. The serial EEPROM can usually be accessed through the BIOS JIDA and JIDA32 interfaces. (See the JIDA and JIDA32 discussion below).

20.4 LVDS Display Parameters

There are four ways in which LVDS flat-panel display parameters can be retrieved:

- The BIOS setup screen may have a list of supported panel types. The selected panel is part of the CMOS / Serial EEPROM configuration parameter record.
- If the JILI option is supported and is selected in the BIOS setup screen and the appropriate JILI hardware is in place, then the BIOS can read the LVDS display parameters from the JILI EEPROM by using the LVDS I^2C interface.
- If the Module BIOS and the LVDS panel support EDID or E-EDID, and the EDID or E-EDID option is selected in the BIOS setup screen, then the BIOS can read the LVDS display parameters form the EDID or E-EDID EEPROM using the LVDS I^2C interface.
- The BIOS may be hard-coded in a custom variant to support a specific display type.

20.5 Standardized BIOS Calls and API: JIDA and JIDA32

JIDA (Jumptec Intelligent Device Architecture) is a BIOS abstraction that lets hardware-specific features such as GPIO pins, watchdog timers, and on-Module serial EEPROM memories to be accessed through a standard set of BIOS calls. JIDA32 is the extension of this to a 32-bit, protected-mode environment. High-level applications may access Module hardware through the JIDA32 API (Application Programming Interface). References to the JIDA and JIDA32 technical documents can be found in Appendix G.

21 Appendix A – Differential Signal Routing Constraints

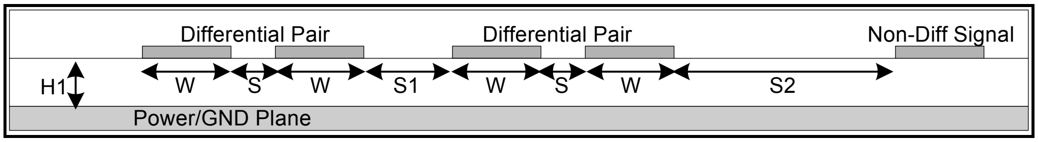
Table 21-1: Differential Pair Signal Routing Constraints – General Rules

Coupling Considerations	
Use 0402 size capacitors over 0603; a smaller package reduces series inductance and saves real estate.	
Use minimum pad size to minimize parasitics.	
Use same capacitor package size for each differential signal.	
Breakout into and out of capacitors should be symmetrical for both signal lines in a differential pair.	
Breakout as close as possible to the capacitors to maximize the amount of coupling within the pair.	
On COM Express Module, the PCIe transmit signals are AC-coupled.	
On COM Express Module, the PCIe receive signals are DC-coupled.	
On Carrier Board, for device-down, the device's PCIe transmit signals (Module receive signals) should be AC-coupled.	
On Carrier Board, for device-down, the device's receive signals (Module transmit signals) should be DC-coupled.	
For Carrier Board slot, the slot card device's transmit signals are AC-coupled on the card.	
For Carrier Board slot, the slot card device's receive signals are DC-coupled on the card.	
Signal Routing Priority	
1. PEG x16, SDVO (differential pairs)	6. LVDS A, B (differential pairs)
2. PCIe 0 – 31 (differential pairs)	7. IDE
3. LAN 0 – 2 (differential pairs)	8. VGA
4. USB 0- 7 (differential pairs)	9. TV – Out
5. SATA 0 – 3 (differential pairs)	10. AC'97
Notes Applicable to all Differential Signals	
GND plane reference for differential signals is preferred. Routing on a single GND referenced layer is best.	
If GND plane reference is not possible, prioritize the signals per the above list and give the higher priority signals a GND plane reference. Signals that can not be referenced to ground should be referenced to a continuous power plane with generous bypassing between the power plane and the GND plane.	
Place stitching caps within 100 mils of transition from GND plane to Power plane and vice versa.	
Minimum 1 stitching cap per 4 differential pairs as long as all pairs are within 100 mils distance requirement stated.	
If possible, use a single reference plane for the entire length of the trace route.	
For transition between 2 GND reference planes, use stitching vias to tie the two GND planes together. Stitching vias should be close to and in symmetry with each signal via to minimize return path discontinuities.	
Use as few vias as possible – impacts overall loss and jitter budget.	
Drop thru via immediately from ETXexpress Module connector and route to device or slot in the inner layer – two vias total.	
Remove isolated via pads from internal layers to minimize excess via capacitance.	
Vias for differential pairs must match in quantity and relative location.	
Trace length before and after via transition must match within 5 mils delta.	
Minimize use of bends – introduces common mode noise affecting signal integrity of differential pairs. If needed, must be 45-degree or smaller – no 90-degree bends or turns.	
Match number of left turn bends with right – minimizes skew due to length differences between each signal of differential pair.	
Alternate between left and right turn bends, which minimizes the amount of skew between rising and falling edges. That in turn minimizes the differential to common-mode conversion.	
Match segments / traces as close as possible at the point of segment / trace length variation.	
Match and balance all signals in the same group.	
Match number of vias, bends for all signals in the same group.	
Maintain routing symmetry with consistent separation and exactly the same lengths and physical dimensions such as width.	
Keep trace lengths as short as possible.	
Increased spacing to other differential traces and signals helps minimize crosstalk and increases margins.	
All ground vias should be connected to all ground planes.	
All power vias should be connected to all power planes at same potential to reduce inductance.	
Avoid routing over voids and plane splits.	
Avoid trace stubs. All differential signals should be point-to-point. (Each trace has only two nodes – the source and the destination).	
Avoid traces under crystals, oscillators, clock synthesizers, magnetic devices, or devices with high transient currents such as switching power supply components.	

Table 21-2: Differential Pair Signal Routing Constraints – Group-Specific Rules

Parameters	Units	PEG	PCIe	SDVO	LAN	USB 2.0	SATA 1.5	LVDS
Transfer Rate (max)	Gb/s	2.5	2.5		1.0	0.48	1.5	
Single Ended Impedance	Ω	55 ± 15%	55 ± 15%	55 ± 15%	55 ± 15%	45 ± 15%	55 ± 15%	55 ± 15%
Differential Impedance	Ω	100 ± 20%	100 ± 20%	100 ± 20%	100 ± 20%	90 ± 15%	100 ± 20%	100 ± 20%
Nominal Microstrip Trace Width (W)	Mils	5	5	5	5	5	5	5
Nominal Microstrip Trace Height (H1)	Mils	3.3	3.3	3.3	3.3	3.3	3.3	3.3
Nominal Microstrip Intra-Pair Spacing (S)	Mils	7	7	7	7	6	7	7
Nominal Stripline Trace Width (W)	Mils	4	4	4	4	4	4	4
Nominal Stripline Trace Height (H1) (H2 >> H1)	Mils	4	4	4	4	4	4	4
Nominal Stripline Intra-Pair Spacing (S)	Mils	7	7	7	7	5	7	7
Differential Pair to Pair Spacing (S1)	Mils	20	20	20	100	20	20	20
Min. Spacing to Non-Differential Signals (S2)	Mils	20	20	20	300	50	20	20
Spacing from Edge of Plane	Mils	40	40	40	40	40	40	40
Module to End Device-down – max	Mils	5000	15850	5000	5000	14000	7200	30000
Module to Slot / Cable Connector Length - max	Mils	4000	9000	4000		10000		4
Length Matching Intra-Pair	Mils	5	5	5	7	75	20	200
Length Matching Inter Pair	Mils	7000	7000	7000		N/A	7000	10000
Segment to Segment Matching	Mils	Required	Required	Required				
Diff Signal to Diff Clock Matching	Mils	N/A	N/A	5	N/A	N/A	N/A	10
Channel to Channel Matching	Mils	N/A	N/A		N/A	N/A	N/A	
AC Coupling Capacitor (if required)	uF	0.1 (dev TX)	0.1 (dev TX)	0.1 (dev TX)	N/A	N/A	On Module	N/A
TX Differential Pair Trace Length from Device-down to AC Capacitor –max	Mils	5000	5000	2500	N/A	N/A	N/A	N/A
AC Capacitor Placement Differential Pair Trace Length Matching	mils	5	5	5	N/A	N/A	N/A	N/A
Via Usage TX Trace – max	Qty.	4	4	2	2	2	2	3
Via Usage RX Trace – max	Qty.	2	2	2	2	2	2	3
Differential Pair Route Grouping	N/A	TX together RX together	TX and RX Paired	TX together RX together	TX and RX Paired	N/A	TX and RX Paired	
Magnetics to RJ45 – max (primary)	Mils	N/A	N/A	N/A	1000	N/A	N/A	N/A
Magnetics to Module – max (secondary)	Mils	N/A	N/A	N/A	1000	N/A	N/A	N/A

Figure 21-1: Differential Pair Stack-up Cross Section



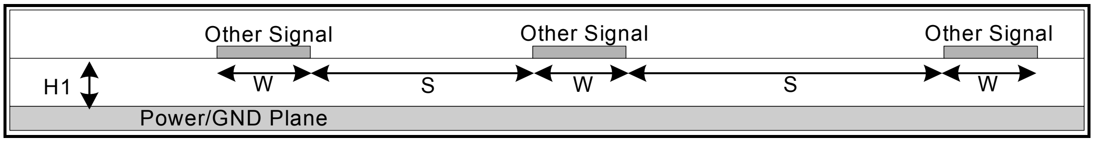
22 Appendix B – Single-Ended (SE) Signal Routing Constraints

Table 22-1: Single-Ended Signal Routing Constraints

Parameters	Units	PATA	VGA	TV-Out	AC'97	PCI BUS	General SE
Signal Group		IDE_xx	VGA_xx	TV_DAC_x	AC_xxxx	PCI_xxxx	Misc.
Transfer Rate (up to)	MB/s	100				211	
Trace Impedance	Ω	55 ± 15%	75 ± 15%	75 ± 15%	55 ± 15%	55 ± 15%	55 ± 15%
Nominal Microstrip Trace Width (W)	Mils	5	4.5	4.5	5	5	5
Nominal Microstrip Trace Height (H1)	Mils	3.3	3.3	3.3	3.3	3.3	3.3
Nominal Microstrip Inter-Signal Spacing (S)	Mils	7	20	40	7	7	7
Nominal Stripline Trace Width (W)	Mis	4	3.5	3.5	4	4	4
Nominal Stripline Trace Height (H1)	Mils	4	4	4	4	4	4
Nominal Stripline Inter-Signal Spacing (S)	Mils	7	20	20	7	7	7
Module to Connector Length - max	Mils	7000	10000	8000	N/A	10000	7000
Length Matching – signals	Mils	200	200	200	200	200	200
Datelines to Strobe/CLK Matching	Mils	450	N/A	N/A	N/A	N/A	450
IOR and IOW Strobe/CLK Matching	Mils	100	N/A	N/A	N/A	N/A	100
PCI Clock Matching to all Loads	Mils	N/A	N/A	N/A	N/A	250	N/A
Signal Route Grouping – on same layer			All Signals same layer				
Termination Resistor to Ground	Ω	N/A	150 ± 10%	150 ± 10%	N/A	N/A	N/A
Termination Resistor to Connector Length - max	Mils	N/A	1000	1000	N/A	N/A	N/A
ESD Diodes to Connector Length - max	inches	N/A	1000	1000	N/A	N/A	N/A
Series Terminating Resistor	Ω	N/A	N/A	N/A	51	N/A	N/A
Series Terminating Resistor to Controller Length - max	Mils	N/A	N/A	N/A	1000	N/A	N/A

Notes Applicable to All Signals	
Ground reference is always preferred	Keep layer changes to a minimum.
Avoid traces directly under crystals, oscillators, clock synthesizers and clock buffers. (Traces on inner layers separated by GND / PWR planes may be OK)	Avoid introducing trace stubs. PCI Bus may have stubs up to 2.0 inches.
Avoid traces under Magnetic Devices.	

Figure 22-1: Single-Ended, Signal Stack-up Cross Section



23 Appendix C – PCIe Lane Overview

The fundamental PCI Express (PCIe) Link consists of two low-voltage differentially driven pairs of signals such as a transmit pair and a receive pair that are configured as a point to point interconnect between two devices. Clocking information is embedded into the data stream using 8b/10b encoding. The characteristic impedance of the Link is 100Ω differential (nominal), while single-ended DC common mode impedance is 55Ω.

The 10-bit symbol transmission encoding scheme achieves equal number of 1s and 0s over time, which results in DC-balanced transmission and eliminates the 2.5GHz clock signal over the Link. Expanding the 8-bit character into 10-bit symbols degrades transmission performance by 20% but achieves reliable Link operation.

The specified Link speed is 2.5Gtransfers/sec/direction, which results in 250MB/sec/direction raw data throughput that is based on 10-bit symbols incorporating 8-bit data. See Figure 23-1 below.

PCIe Links consist of a varying number of Lanes(x1, x2, x4, x8, x16 and x32) where each numeral represents the number of Lanes resulting in 1, 2, 4, 8, 16 and 32 transmit and receive interfaces per device supporting throughputs of 250, 500, 1000, 2000, 4000 and 8000 MB/sec/direction respectively.

When a Link has more than 1 Lane, Byte Striping is implemented. Each consecutive outbound character in a character stream is multiplexed onto consecutive Lanes. See Figure 23-1 below.

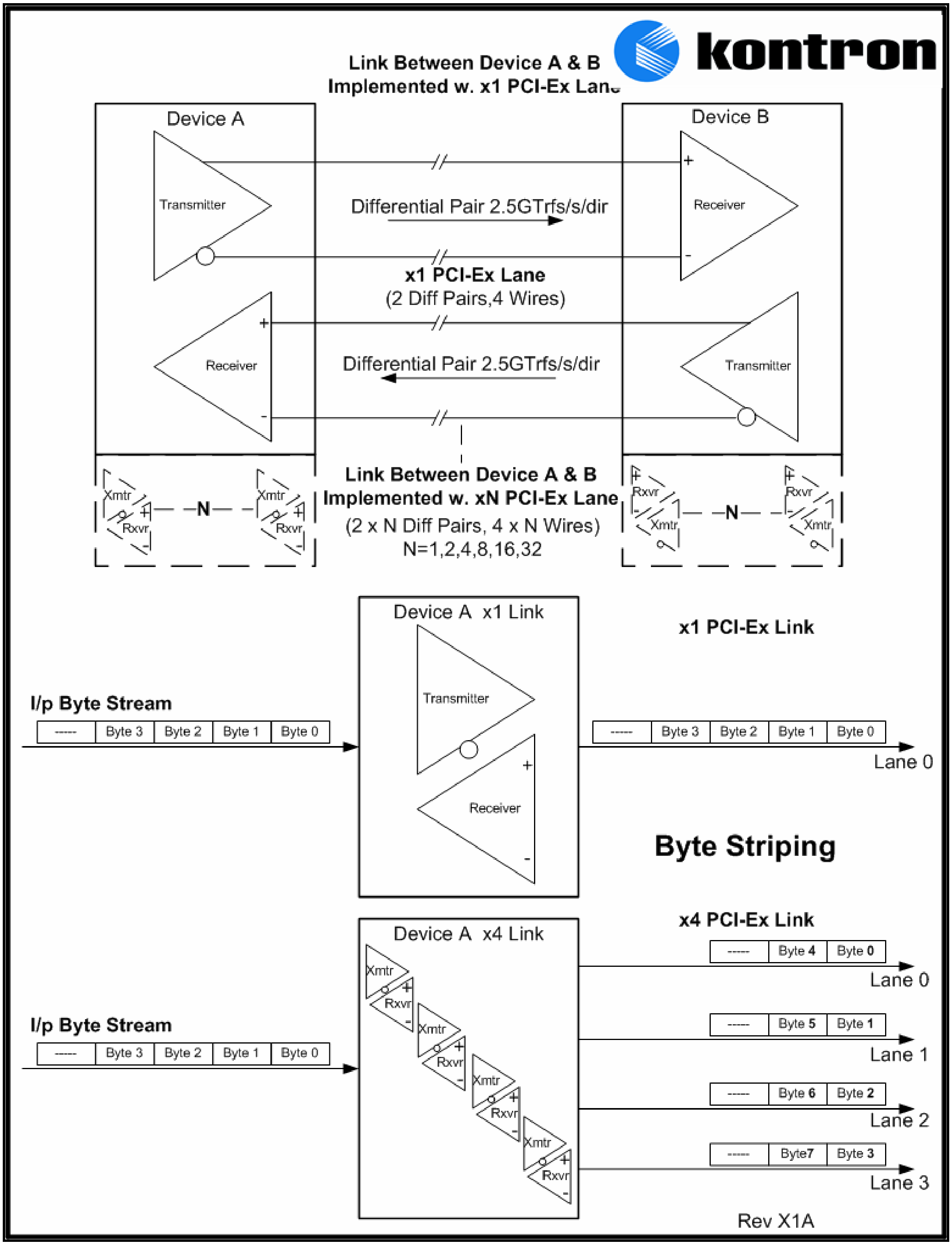
The PCI Express™ Specification requires polarity inversion to be supported independently by all receivers across the link. The lane performs polarity inversion during initial training sequence if the receiver detects polarity discrepancies. The lane will function correctly even if a positive (TX+) signal from a transmitter is connected to the negative (RX-) signal of a receiver.

Lane Reversal involves reversing the mapping of lanes in an x2 or greater link. The typical interconnect for example in an x4 link is TX0, TX1, and TX2, TX3 connected to RX0, RX1, RX2, and RX3 respectively. In a link that supports lane reversal, mapping can be reversed such that TX0, TX1, TX2, TX3 is connected to RX3, RX2, RX1, RX0 respectively and mapped to RX0, RX1, RX2, RX3 respectively under the control of a hardware signal typically activated via a strapping option. The Lane Reversal feature is an optional feature of the PCI Express™ Specification.

Polarity Inversion or Lane Reversal does not imply direction inversion or reversal. The TX differential pair from an upstream device must still connect to the RX differential pair on the downstream device.

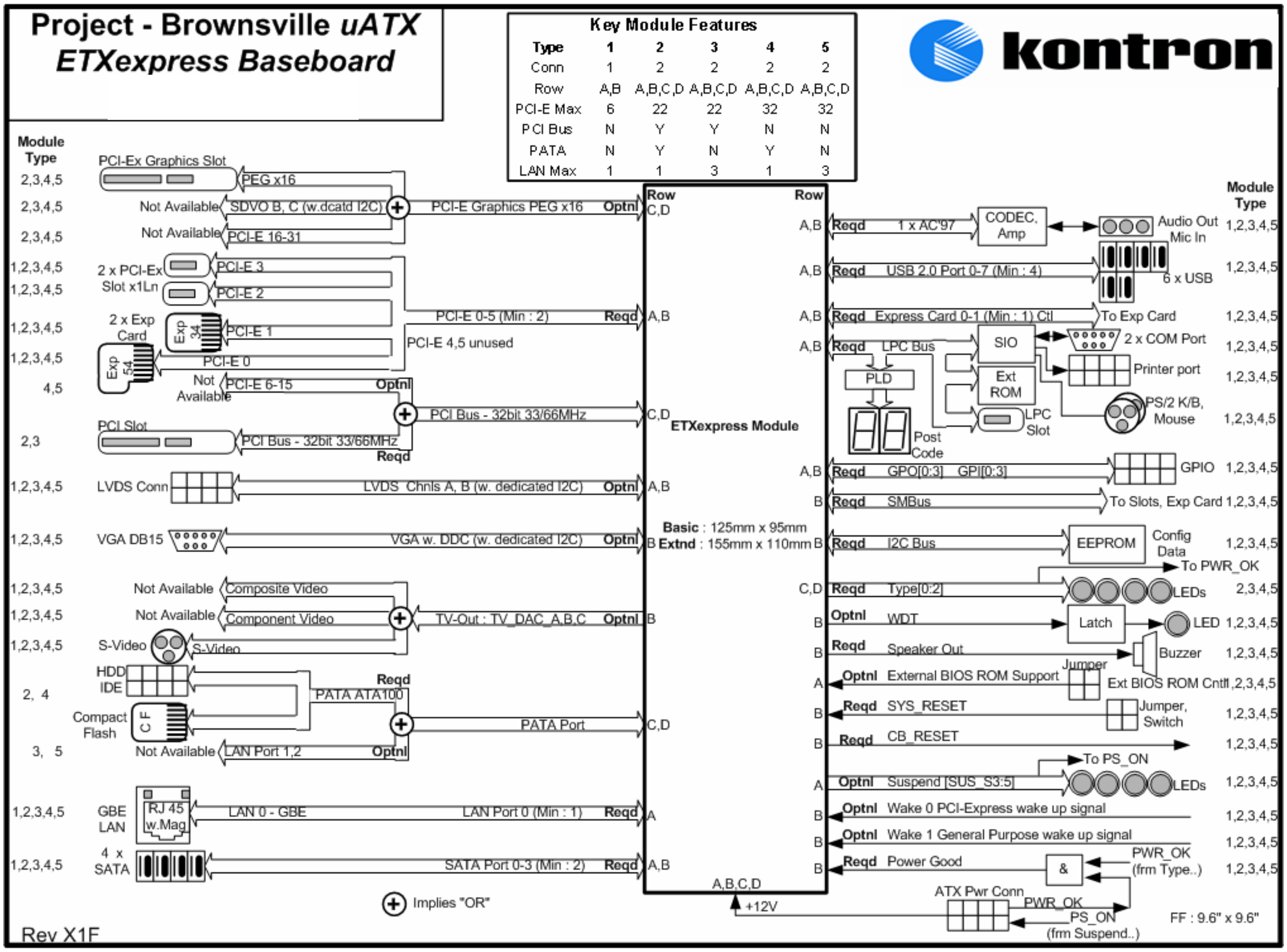
Each device in a link can support multiple lane widths. The two devices negotiate a width that both devices can support during the link-training phase. The PCI Express™ Specification requires that all devices be capable of forming an x1 link as well as their maximum link size.

Figure 23-1: PCIe Lane Links



24 Appendix D – ETXexpress Carrier Board Overview

Figure 24-1: ETXexpress Carrier Board Summary



24.1 Features Matrix

Table 24-1: ETXexpress Carrier Board Features Matrix

Feature	Description	Options
Preliminary	Project Brownsville ETXexpress Carrier Board	
Revision	X1B, March 31, 2005	
ETXexpress Module Support	COM Express™ Modules Type 1 & 2 Support COM Express Connectors Rows A,B,C,D	
Form factor – Carrier Board	9.6in x 9.6in – MicroATX FF Support uATX Mounting Hole Pattern Provide Mechanical mounting for Basic & Extended Modules	
PCIe Graphics PEG x16	PCIe Graphics Slot	Type 2 only
PCIe 0-5	PCIe0 : x1 PCIe Slot 0 PCIe1 : x1 PCIe Slot 1 PCIe2 : Express Card 34 PCIe3 : Express Card 54 PCIe4 : Unused PCIe5 : Unused	
PCI Bus 32bit 33MHz	1 x PCI 32/33 Slot	Type 2 only
LVDS Channels A,B	Connected to 40 pin x1 0.5mm connector	
VGA Port	Connected to female DB15 connector – mounted in ATX I/O zone	
TV-Out : TV_DAC A,B,C	Connected to 4 pin Mini DIN connector – mounted in ATX I/O zone	
PATA Port	PATA Port supporting: IDE connected to 20 pin x2 2.54mm connector CF connected to 25 pin x2 vertical connector	Type 2 only
LAN Port 0	GBE Port 0 connected to RJ45 combo w. USB connector – mounted in ATX I/O zone	
SATA Port	SATA Ports 0-3 connected to 4 x vertical SATA connector	
AC '97	Connected to 3.5mm Triple Stacked Jack – mounted in ATX I/O zone supporting : Line-In – Blue R/L Speaker Out 6W/Chnl – Green Mic In - Pink	
USB 2.0 Ports	Port 0 & 1 connected to RJ45 combo w. USB connector – mounted in ATX I/O zone Port 2,3,4,5 connected to 4 x USB Stacked connector– mounted in ATX I/O zone	
LPC Bus	Connected to : 1 x LPC Slot Ext BIOS ROM Support Jumper – EN/DS 2 x 7 Segment Post Code Display Super I/O supporting: 2 x COM ports w. male stacked DB9 connector – mounted in ATX I/O zone 2 x PS/2 Stacked Keyboard and Mouse connector – mounted in ATX I/O zone Printer Port connected to 13 pin x2 2.54mm connector	
GPIO	GPO 0 & GPI 0 connected to LPC slot GPO 1-3 & GPI 1-3 w. 5V & GND connected to 8 pin x1 2.54mm connector	
I2C Bus	Connected to EEPROM	
WDT (Watch Dog Timer)	Latched to drive LED	
Type (0:2)	Drive LEDs Control Power_OK Jumper to force Power_OK	Type 2 only
Speaker Out	Drive Buzzer on BB	
System Reset	Jumper – EN/DS Via Switch	

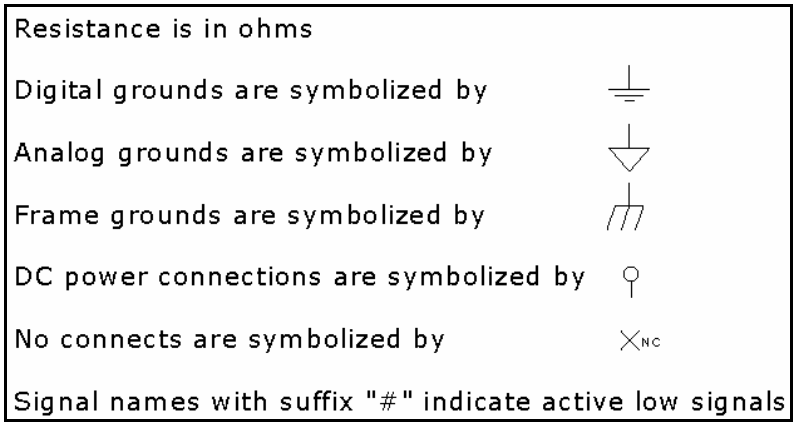
Feature	Description	Options
Suspend SUS_3:5	LEDs to indicate sleep states Control PS_ON	
Wake 0,1	Wake 0 connected to: PCI –Ex Slots Express Card Slots Wake 1 connected to: LPC Slot	
RTC Battery	Incorporate Coin Battery for RTC	
Carrier board Fan Header	Support Fan Header – 2 x 3 pin 2.54mm	
Operating Environment	Temperature: 5°C to 50°C Relative Humidity: >10% & <90% Non-Condensing	
Power Requirements	+12V & +5V ± 5%, ??A Support Standard ATX Connector	
Regulatory	FCC Class A UL xxx CSA xxx	

25 Appendix E – ETXexpress Carrier Board Schematics

25.1 Schematic Conventions

Figure 25-1 explains the symbols that are used in the following ETXexpress Carrier Board schematics. The schematics come from Kontron’s first ETXexpress Carrier Board design called Project Brownsville, or Brownsville for short.

Figure 25-1: Schematic Symbols



25.2 Table of Contents for Brownsville Schematics

Figure 25-2: Cover Sheet and Index (Sheet 1 of 21)

Brownsville

ETXexpress Motherboard

500-089

REVISION B

TABLE OF CONTENTS

Design Notes:

Resistance is in ohms

Digital grounds are symbolized by

Analog grounds are symbolized by

Frame grounds are symbolized by

DC power connections are symbolized by

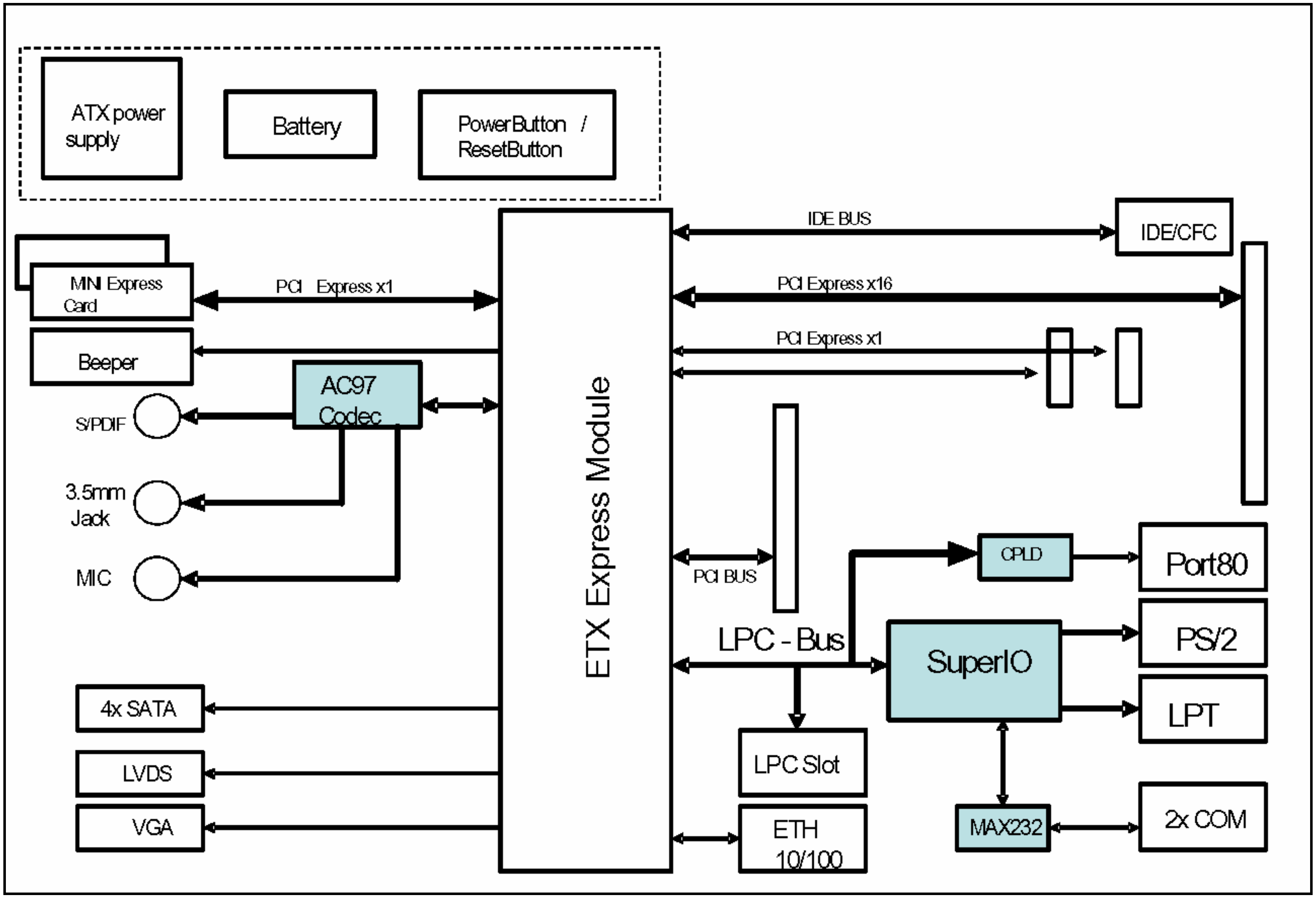
No connects are symbolized by

Signal names with suffix "#" indicate active low signals

COVER PAGE

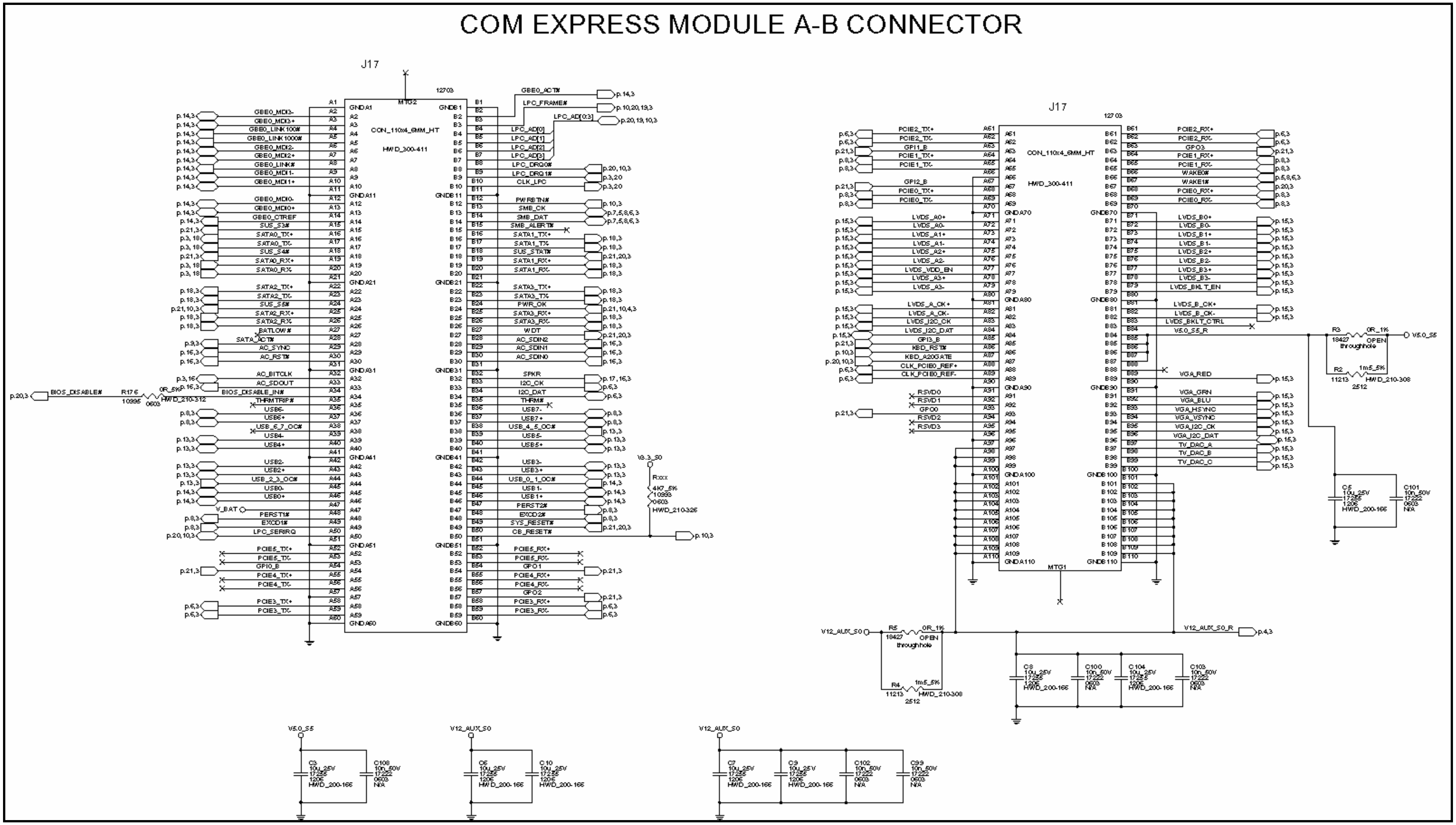
25.3 Block Diagram

Figure 25-3: Block Diagram (Sheet 2 of 21)



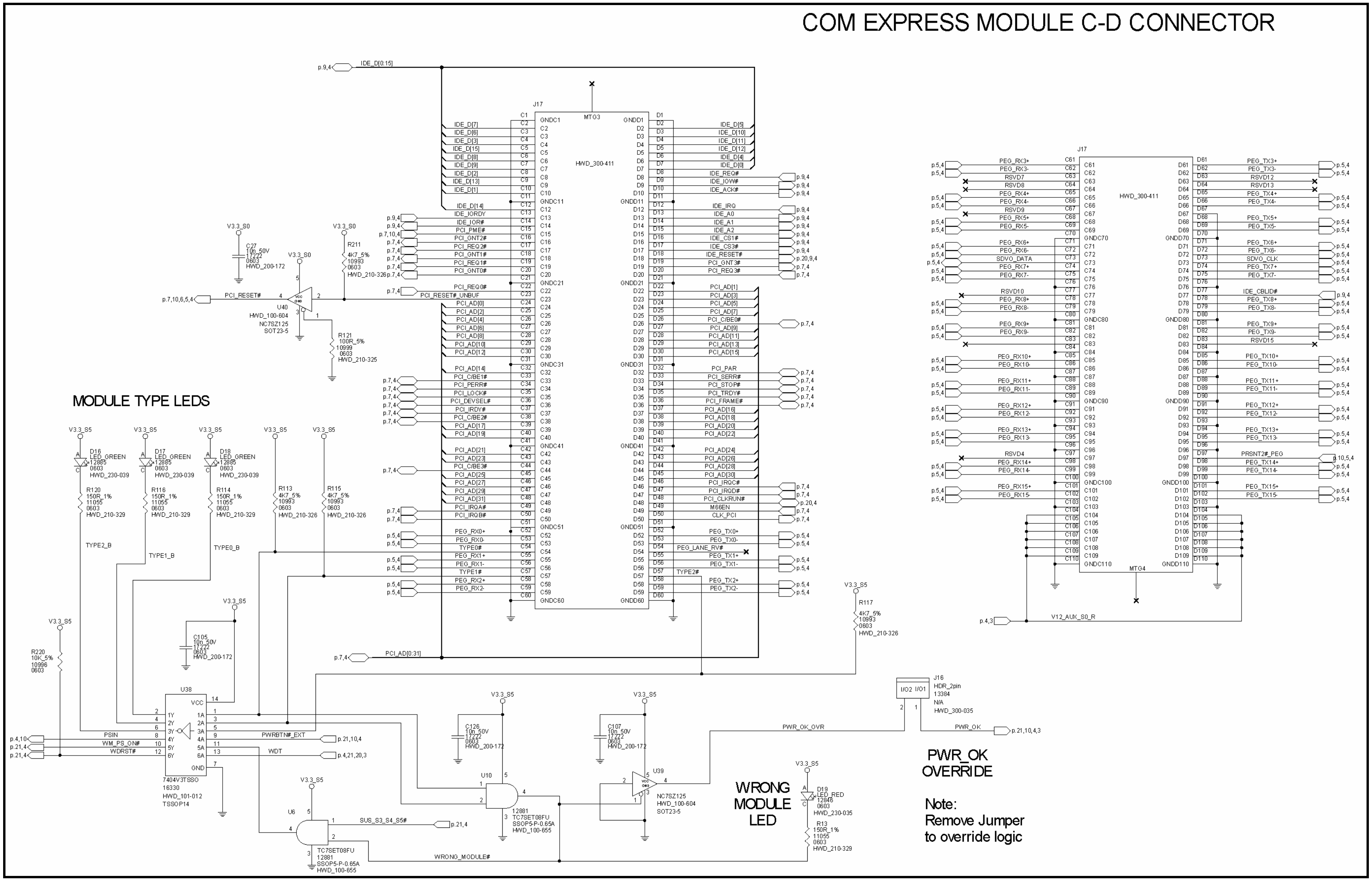
25.4 ETXexpress Connectors A and B Schematic

Figure 25-4: ETXexpress Connectors A and B (Sheet 3 of 21)



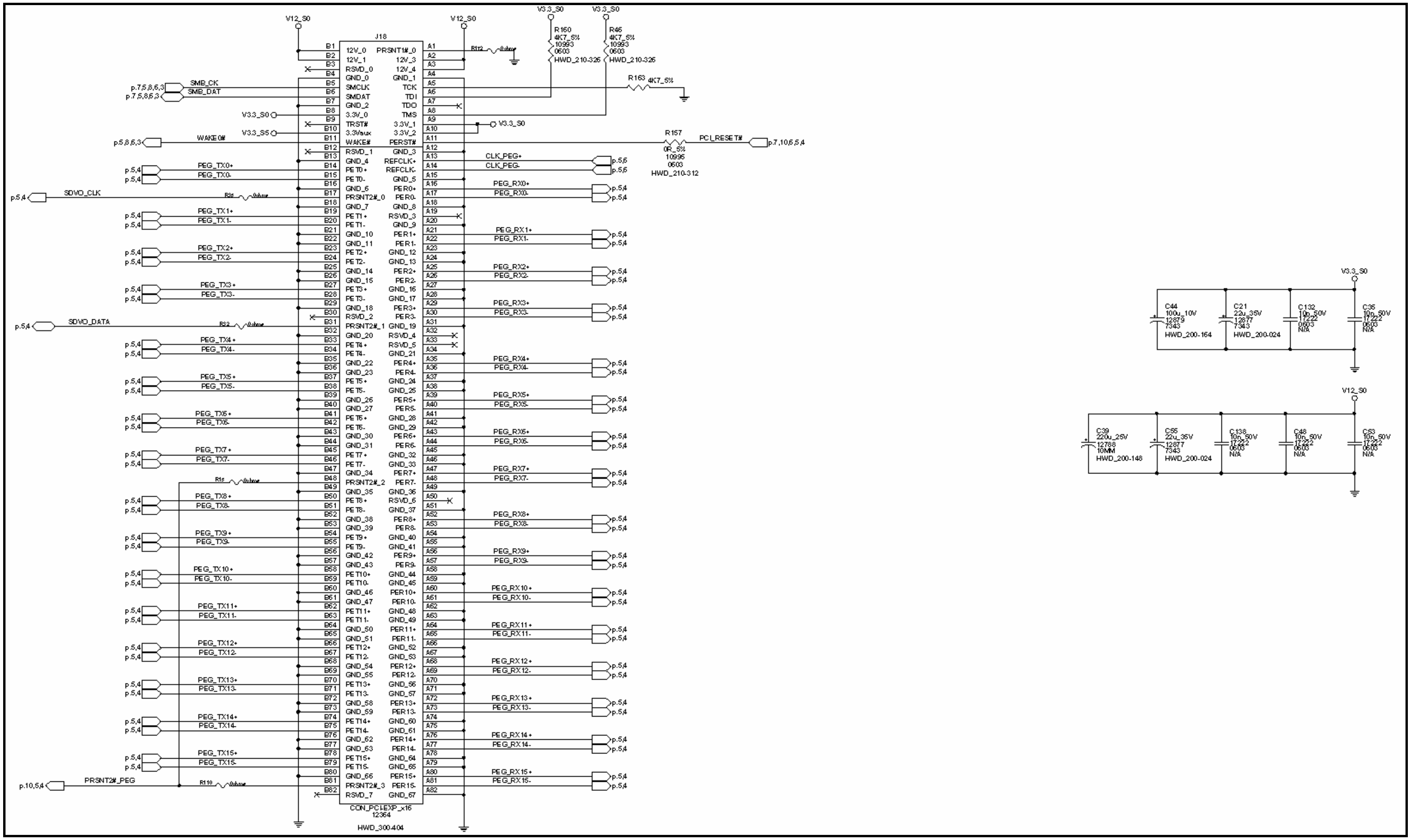
25.5 ETXexpress Connectors C and D Schematic

Figure 25-5: ETXexpress Connectors C and D (Sheet 4 of 21)



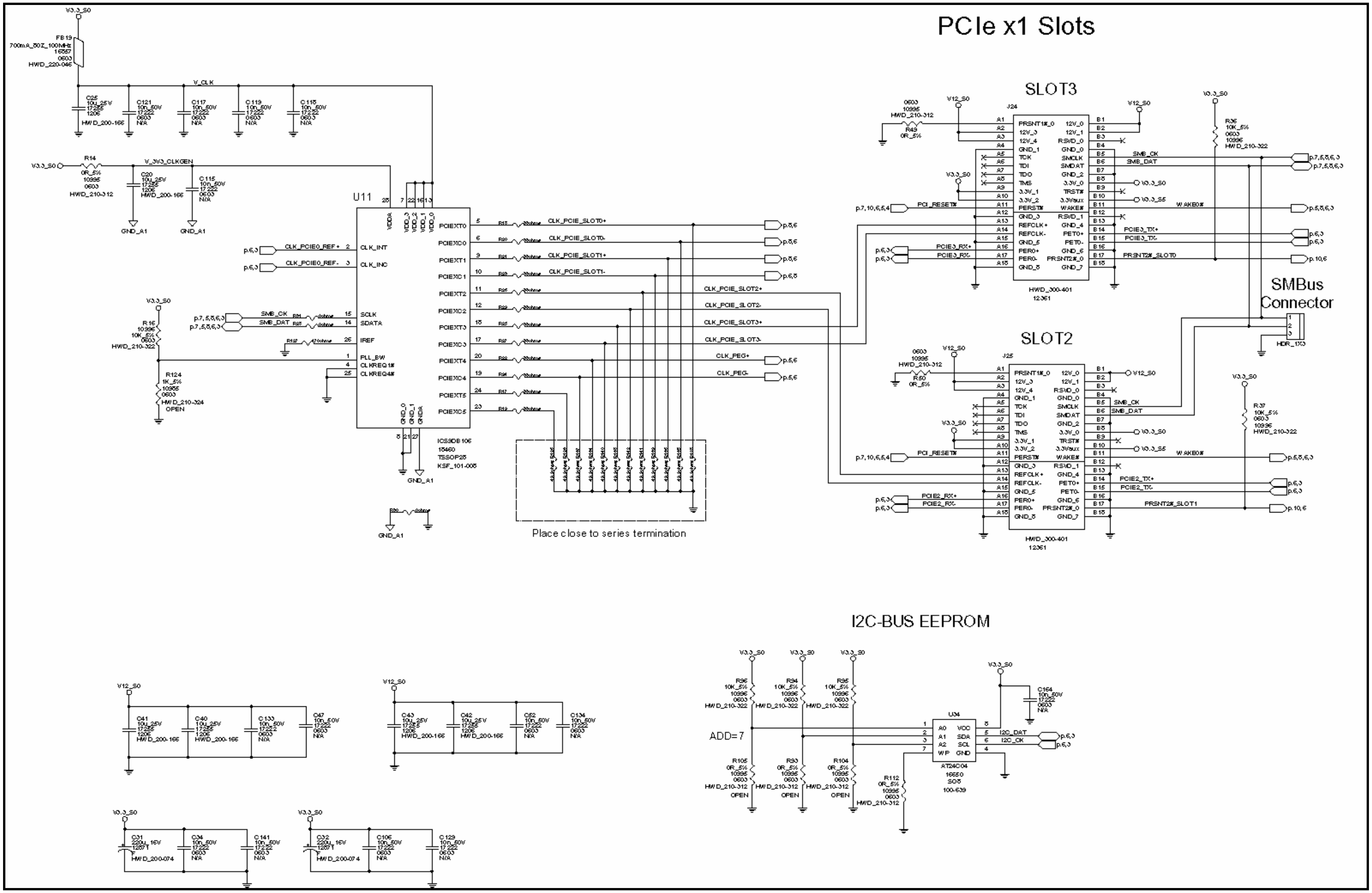
25.6 PCI Express Graphics (PEG) Schematic

Figure 25-6: PCI Express Graphics (Sheet 5 of 21)



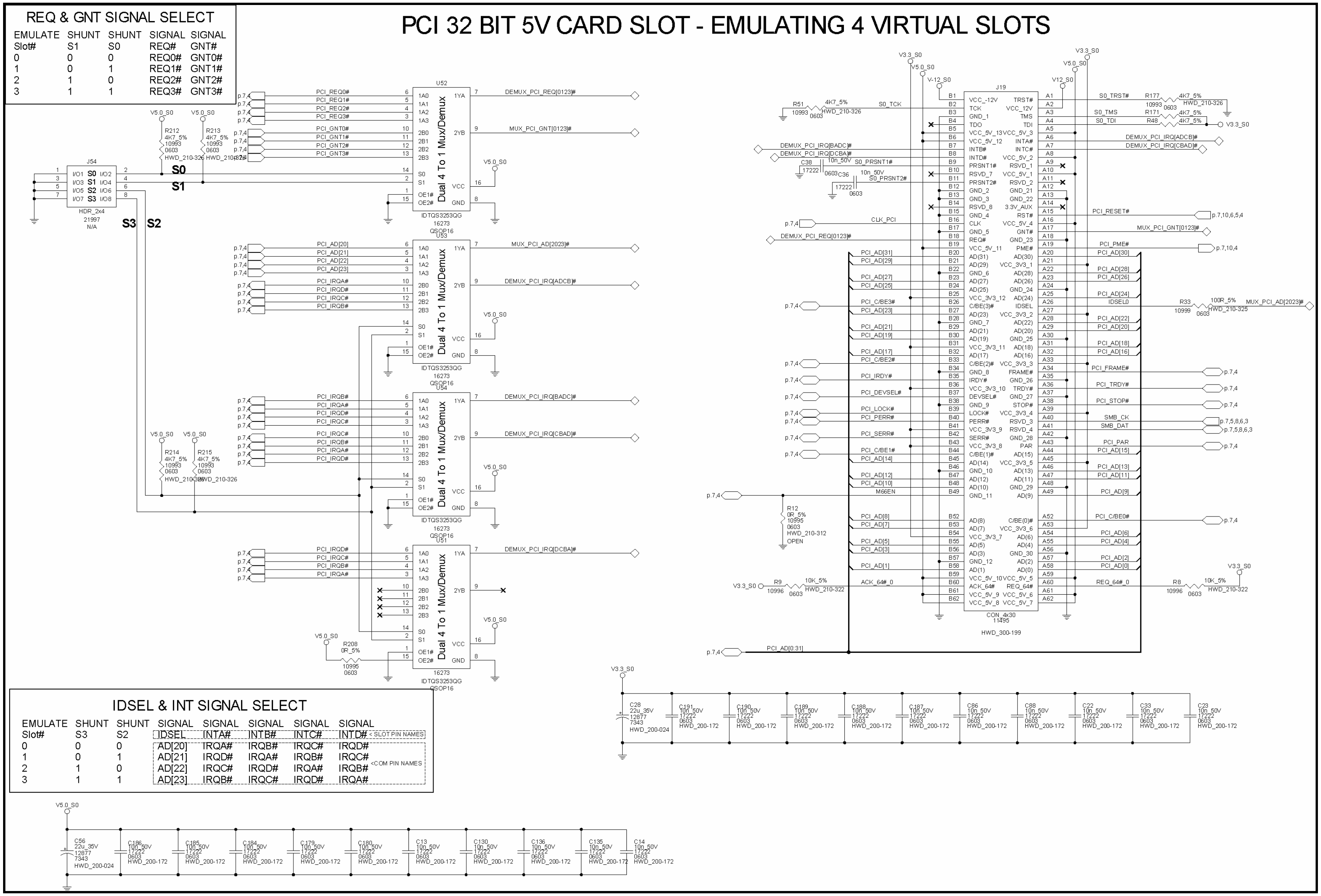
25.7 PCI Express (PCIe) Connectors Schematic

Figure 25-7: PCI Express (PCIe) Connectors (Sheet 6 of 21)



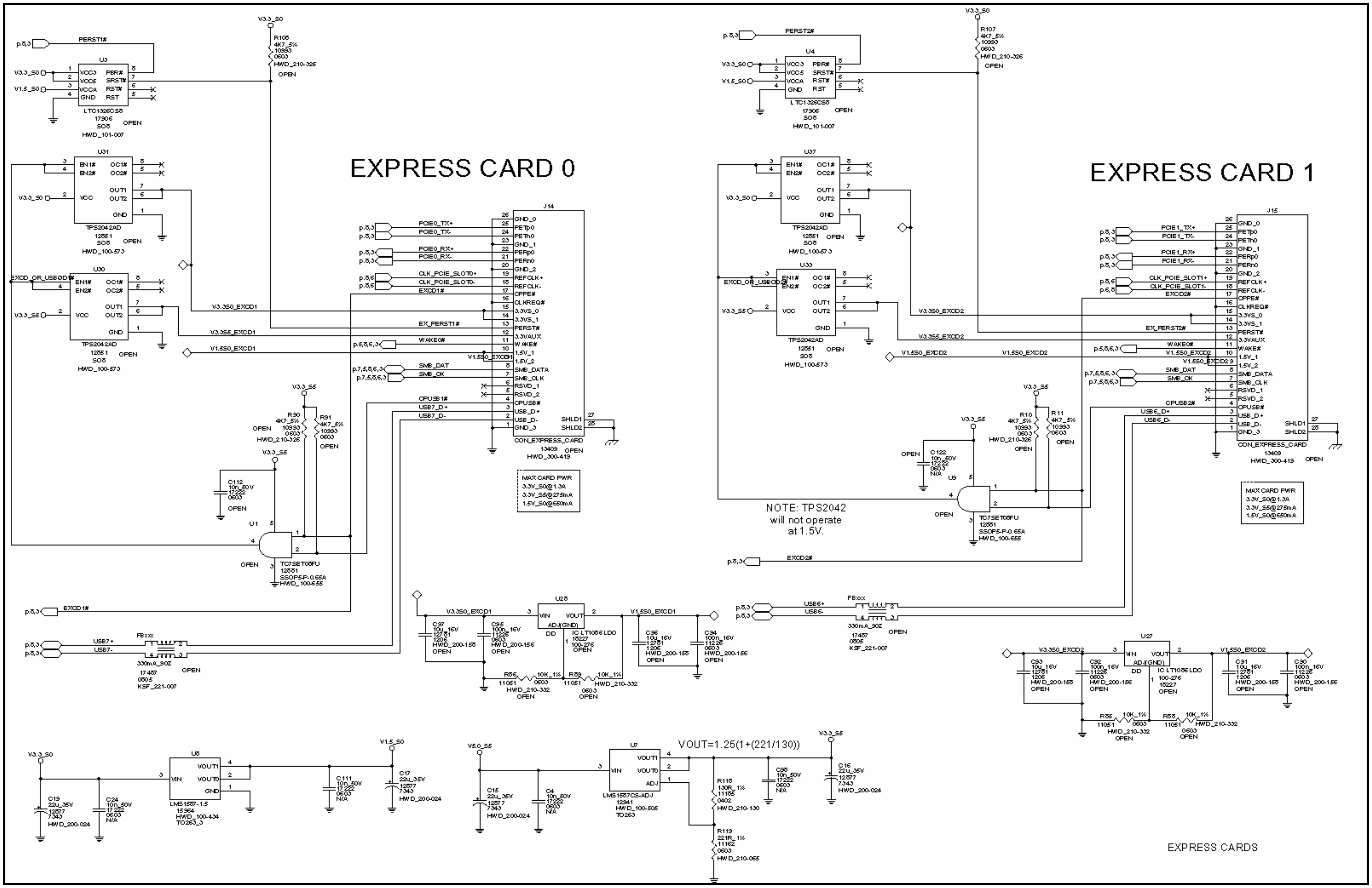
25.8 PCI Connector Schematic

Figure 25-8: PCI Connector Schematic (Sheet 7 of 21)



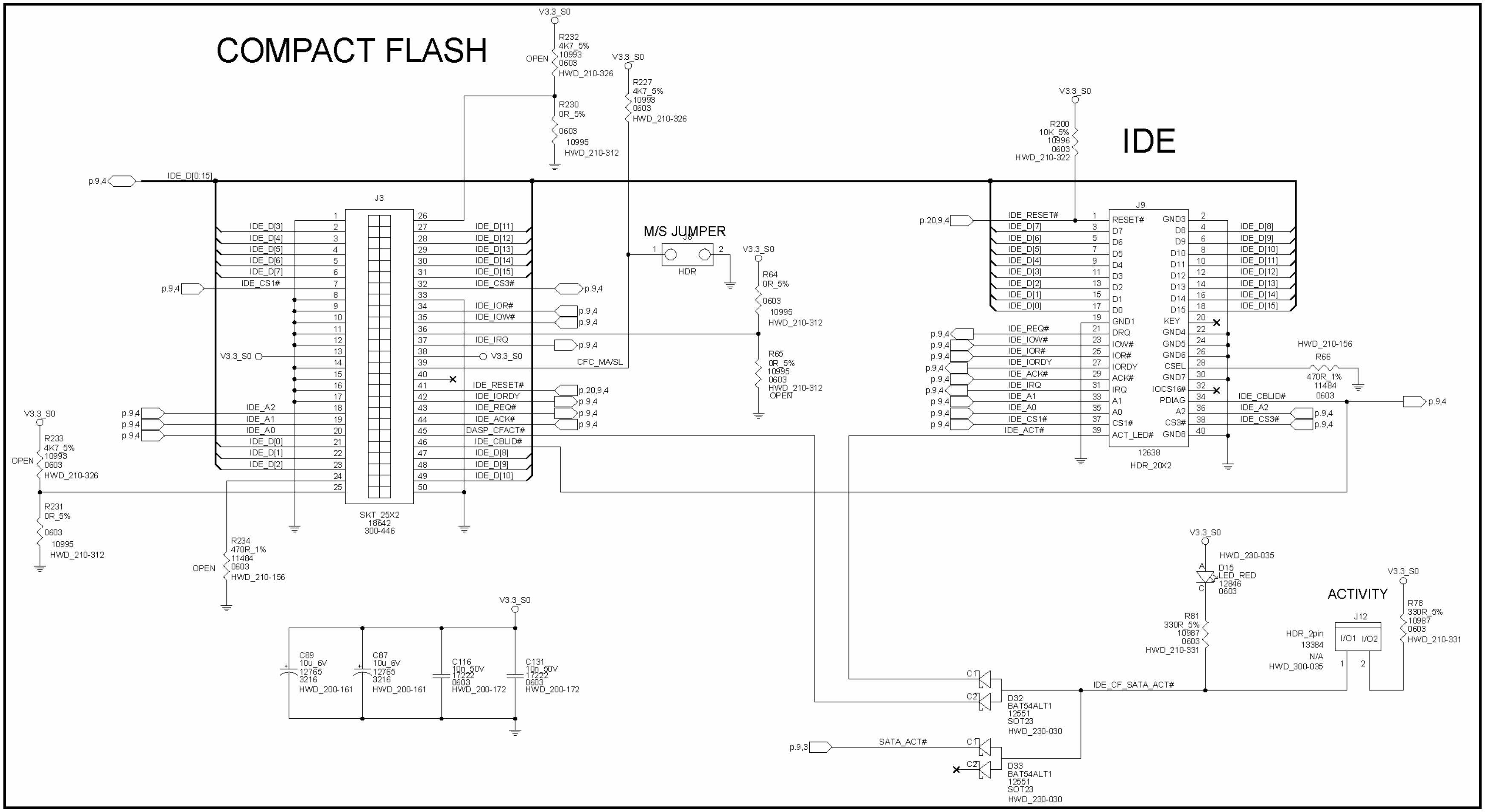
25.9 Express Card Connectors Schematic

Figure 25-9: Express Card Connectors Schematic (8 of 21)



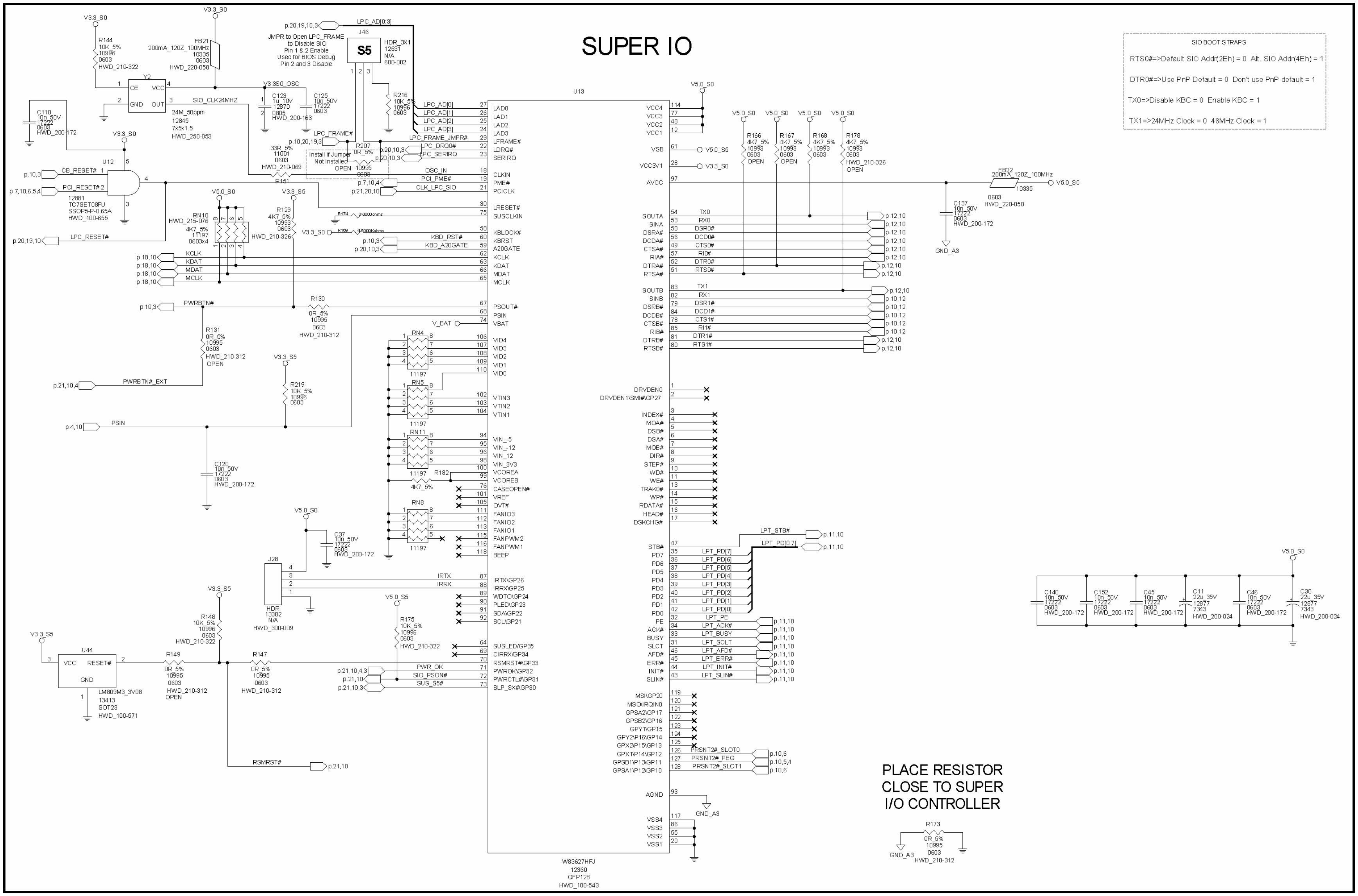
25.10 IDE and Compact Flash Schematics

Figure 25-10: IDE and Compact Flash Schematics (Sheet 9 of 21)



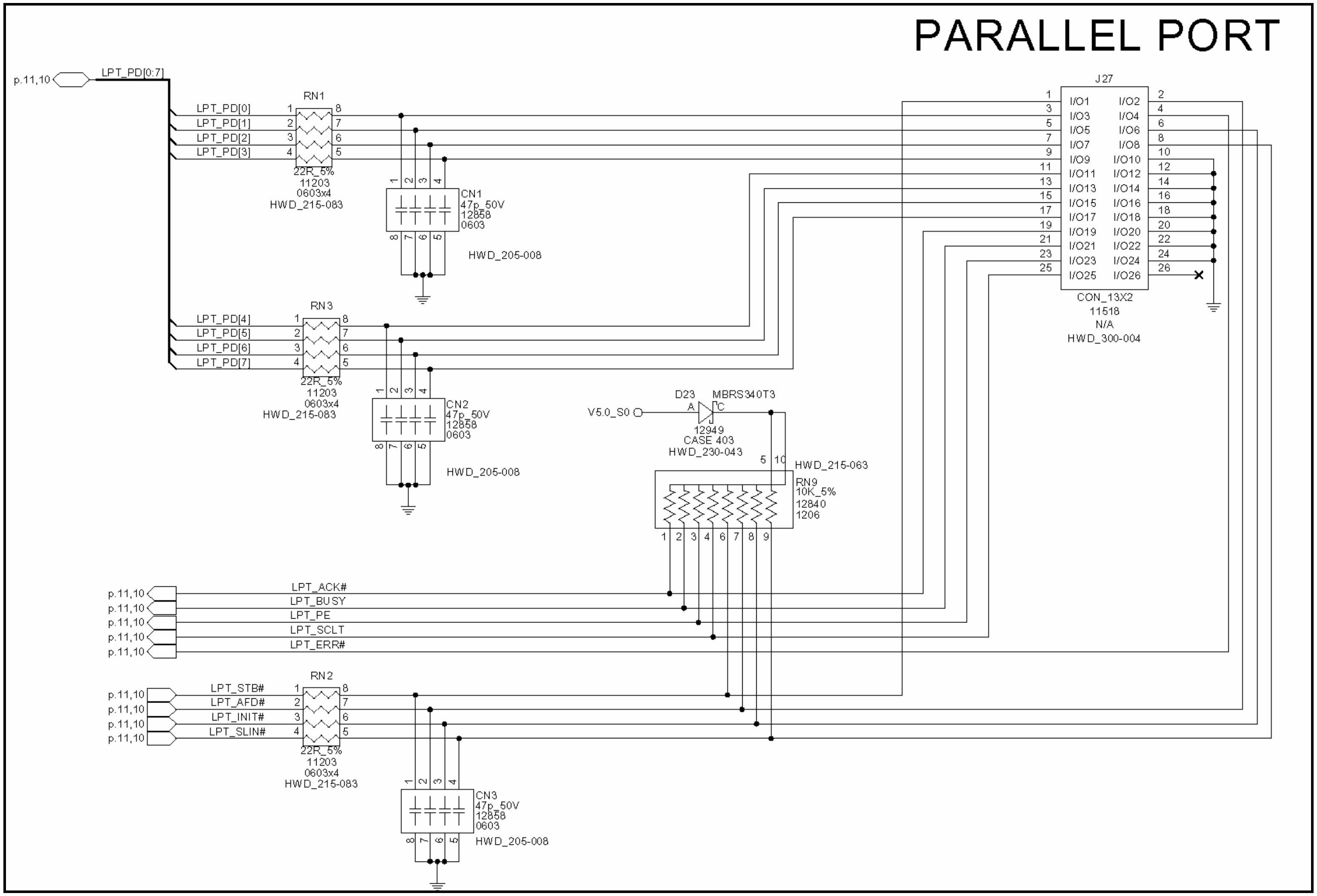
25.11 Super I/O Schematic

Figure 25-11: Super I/O Schematic (Sheet 10 of 21)



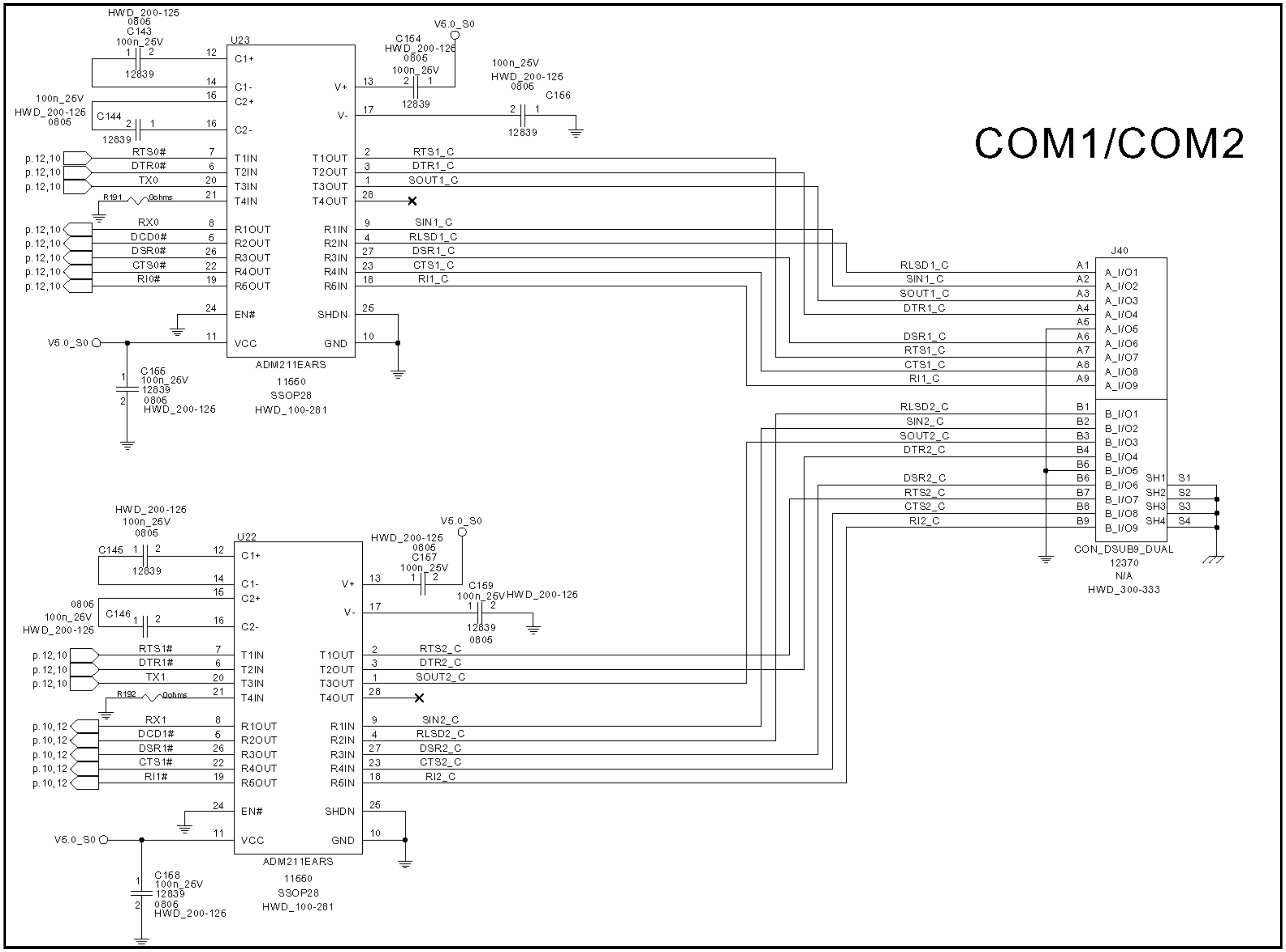
25.12 Parallel Port Schematic

Figure 25-12: Parallel Port Schematic (Sheet 11 of 21)



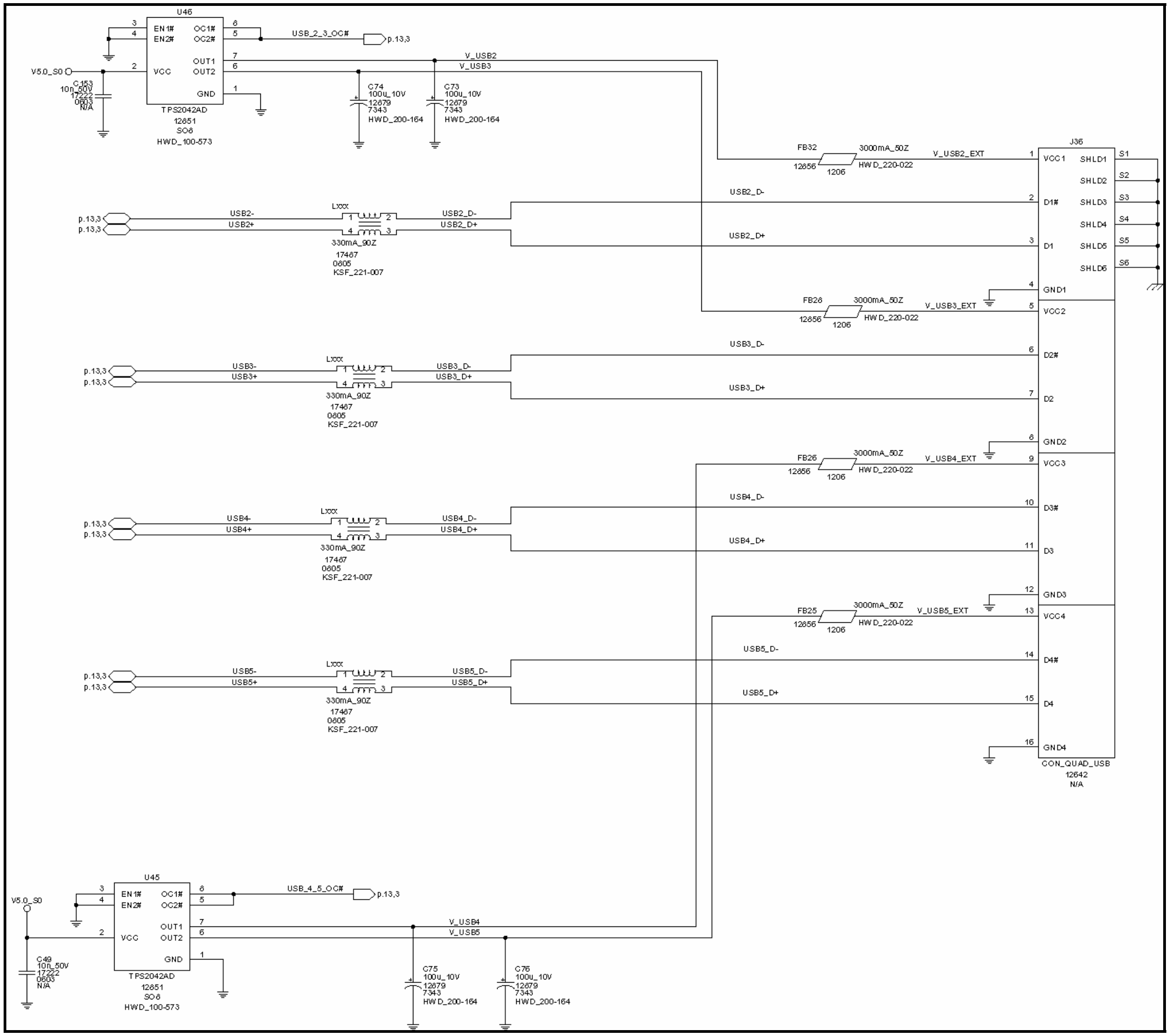
25.13 Serial Port Buffer Schematic

Figure 25-13: Serial Port Buffer Schematic (Sheet 12 of 21)



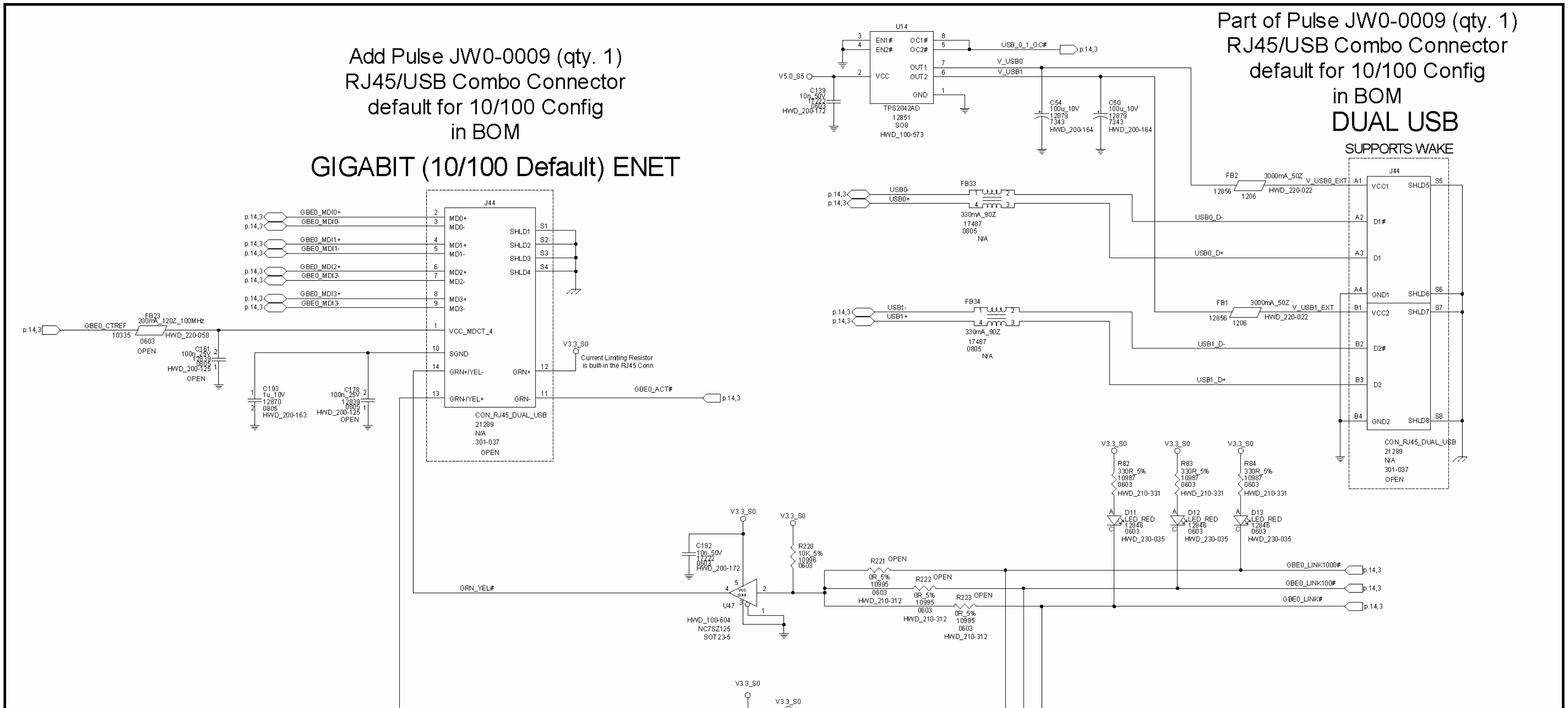
25.14 USB 2, 3, 4, and 5 Schematics

Figure 25-14: USB 2, 3, 4, and 5 Schematics (Sheet 13 of 21)



25.15 USB 0,1 and Gigabit Ethernet Schematics

Figure 25-15: USB 0,1 and Gigabit Ethernet Schematics (Sheet 14 or 21)



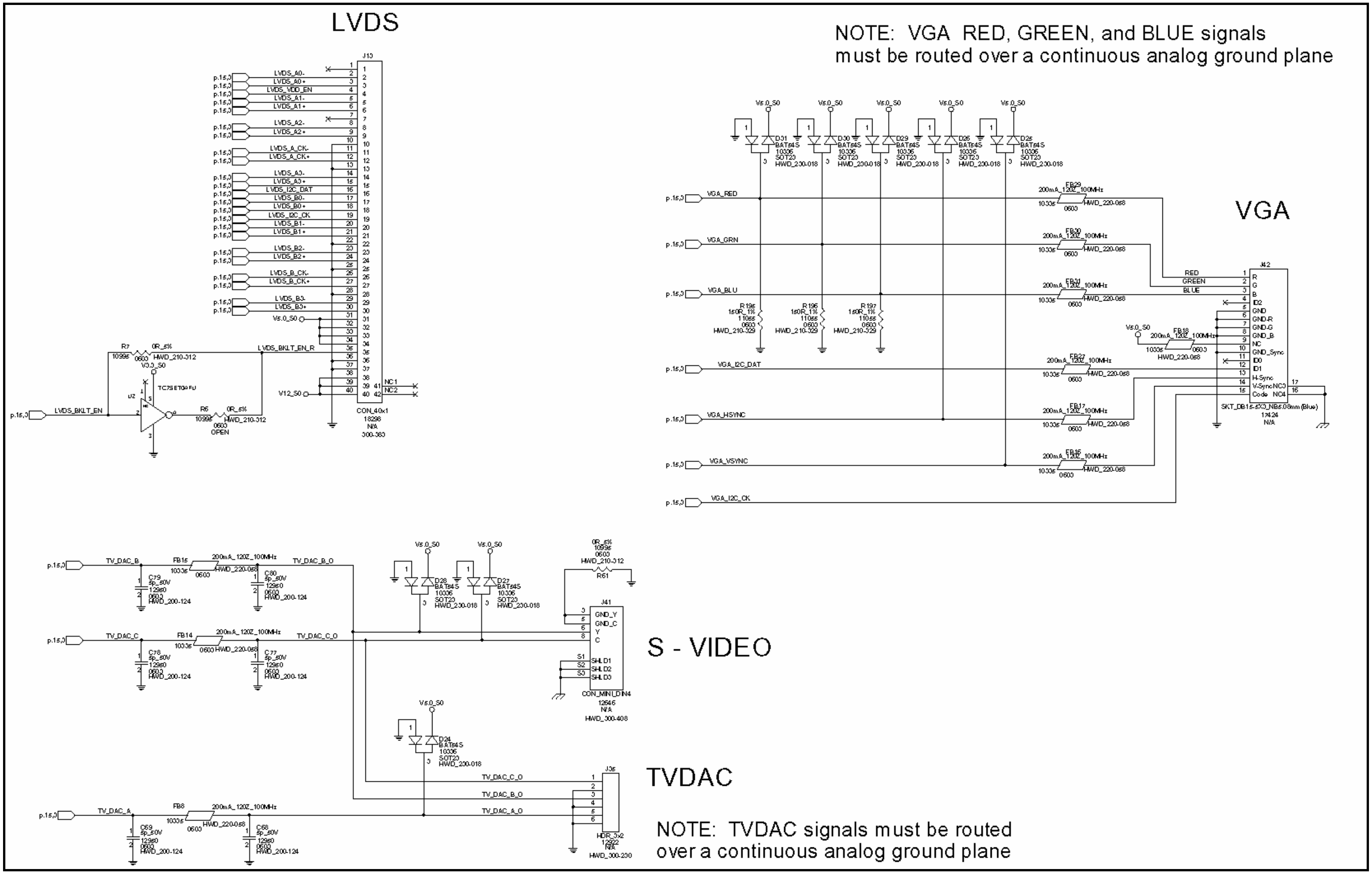
Config	LED	J44	Open	Install
10/100 Plano Default	100 - Yel (right) ACT - Grn (left)	Pulse JW0-0009	C161 C178 FB23 R222 R226	R225 C193
10/100/1000 Galveston	100 - Green (right) 1000 - Yel (right) ACT- Grn (left)	Pulse JW0-0006	R225 C193	C161 C178 FB23 R222 R226

All configurations:

Open: R221, R223, R224

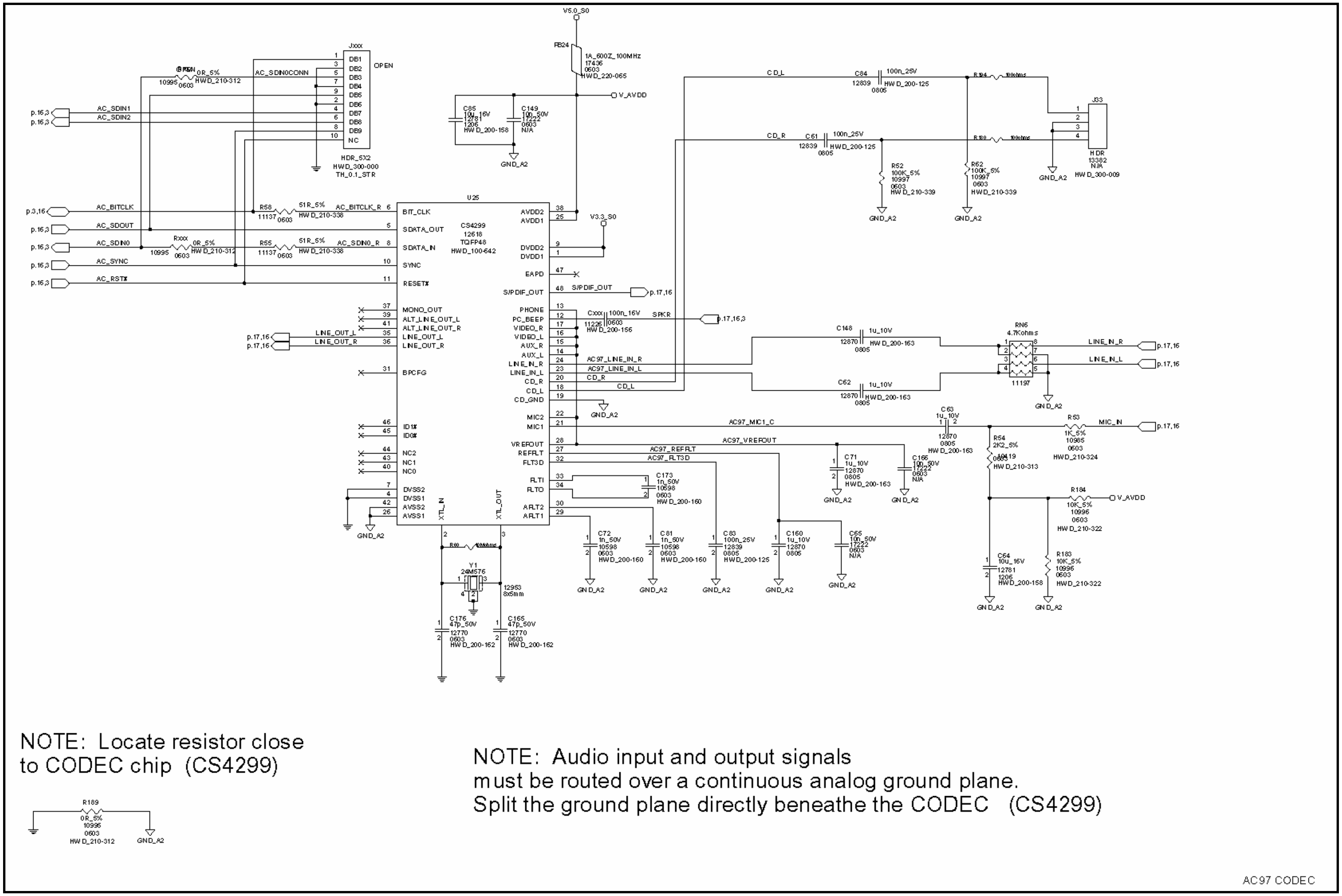
25.16 Video Schematic

Figure 25-16: Video Schematic (Sheet 15 of 21)



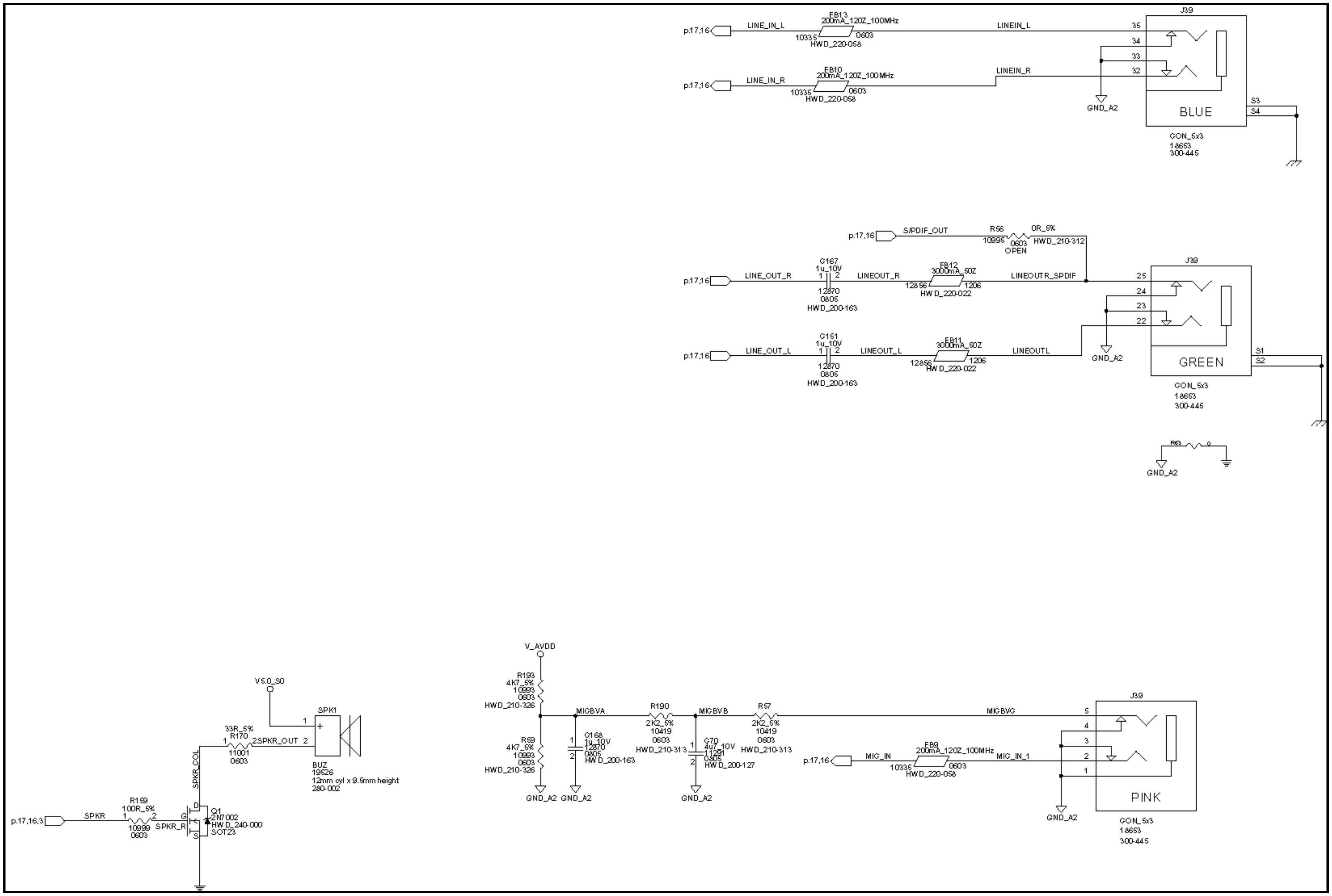
25.17 AC97 Codec Schematic

Figure 25-17: AC97 Codec Schematic (Sheet 16 of 21)



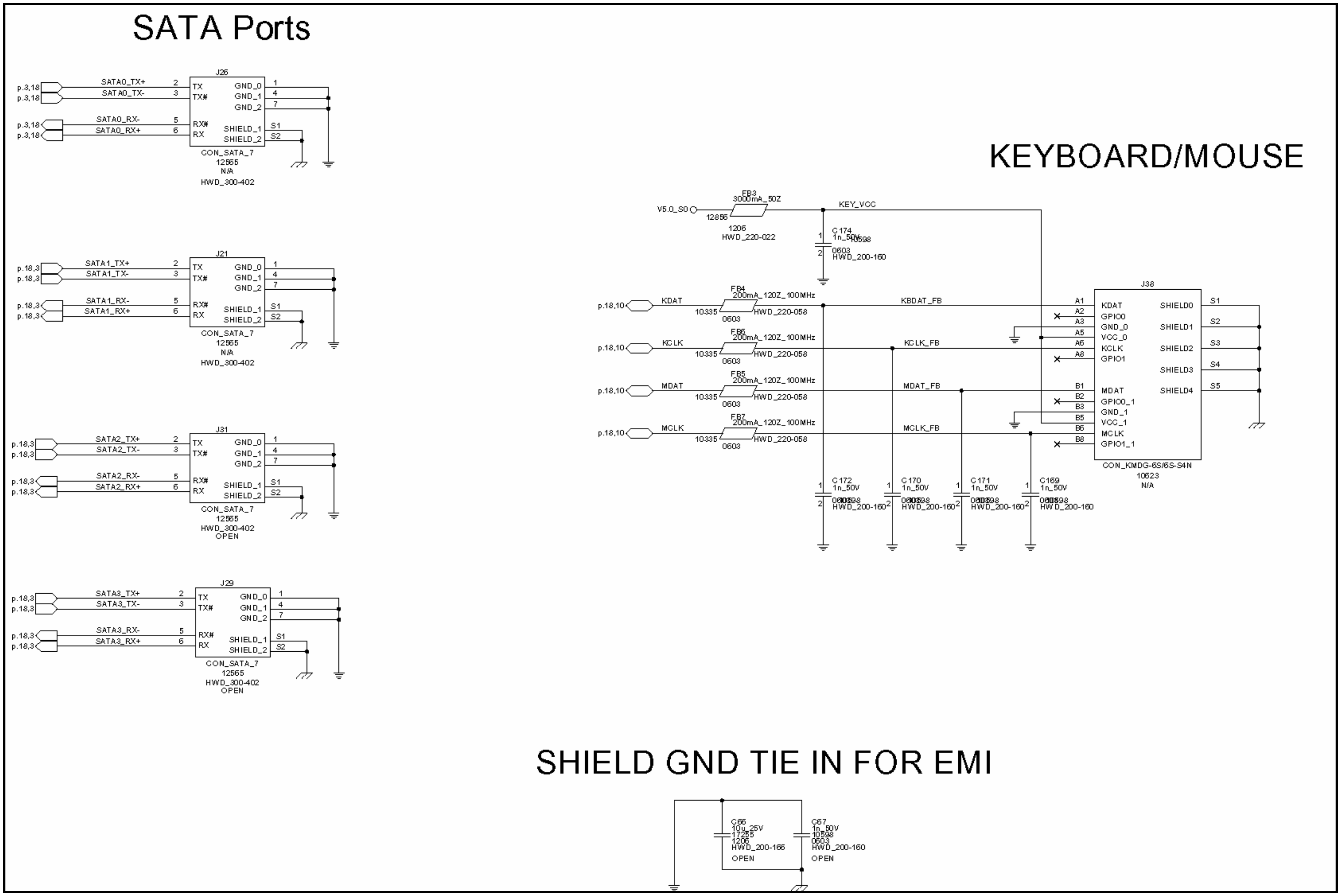
25.18 Audio Connectors Schematic

Figure 25-18: Audio Connectors Schematic (Sheet 17 of 21)



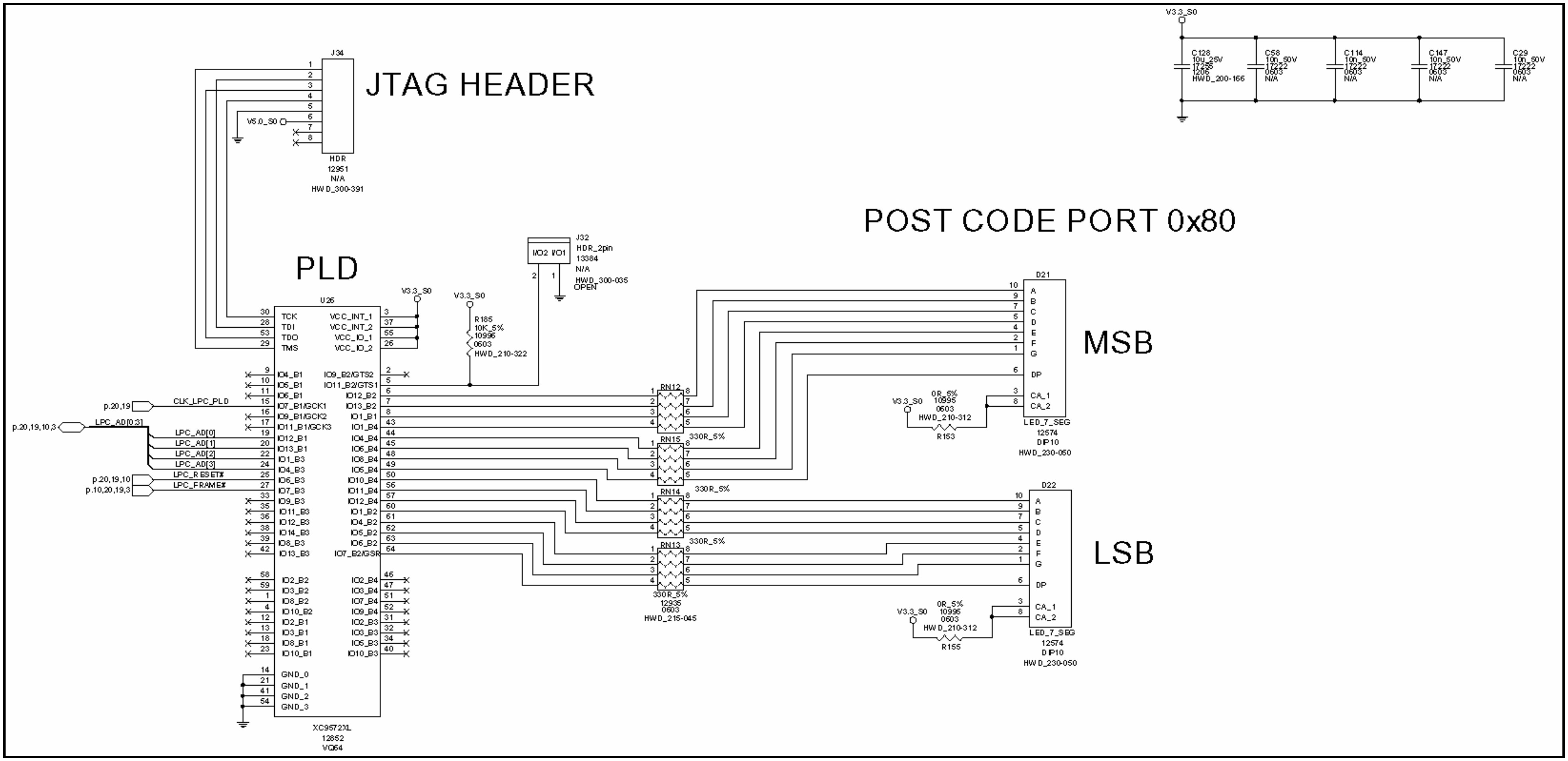
25.19 SATA, Keyboard and Mouse Schematics

Figure 25-19: SATA, Keyboard, and Mouse Schematics (Sheet 18 of 21)



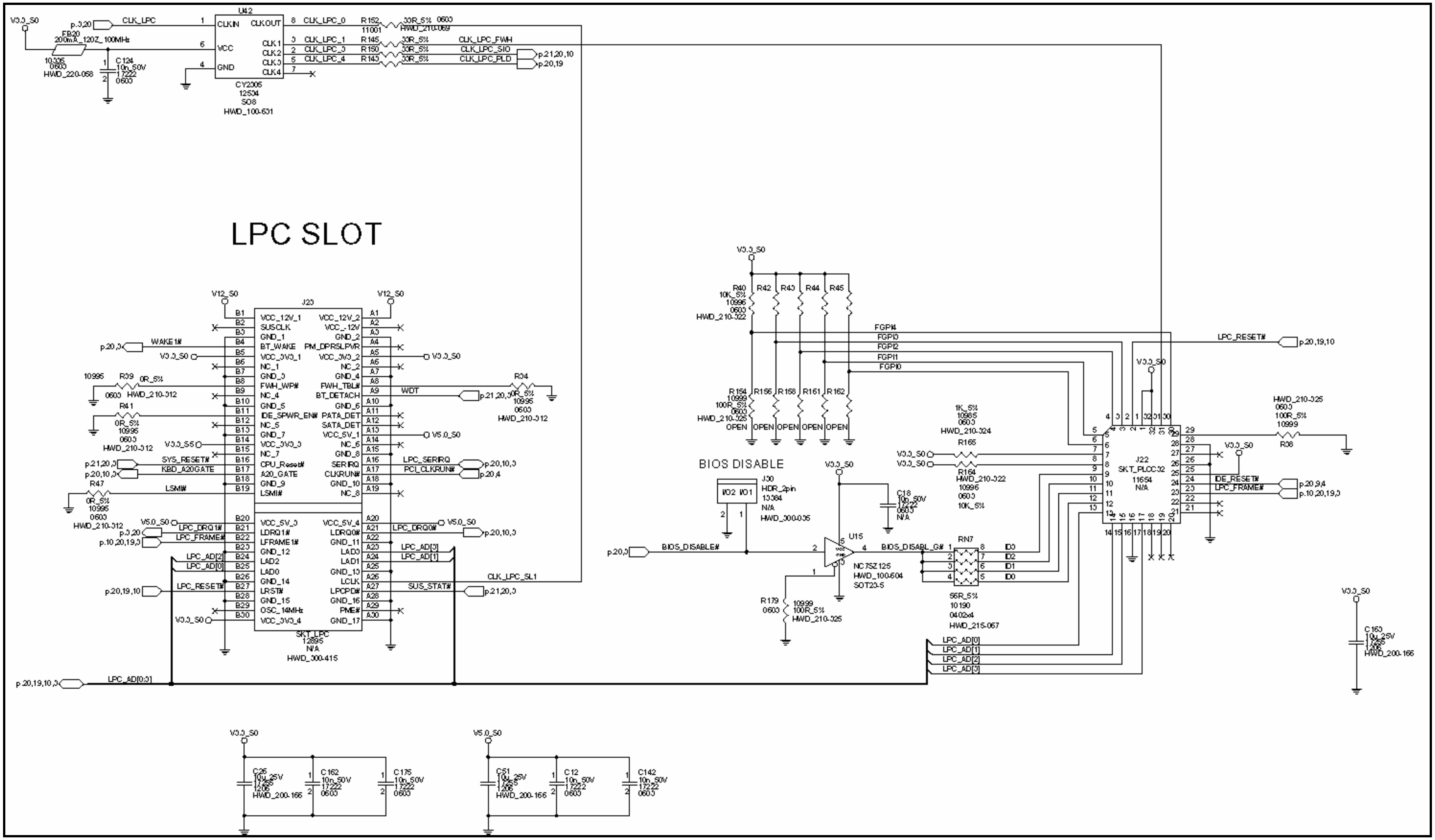
25.20 Port 80 CPLD Schematic

Figure 25-20: Port 80 CPLD Schematic (Sheet 19 of 21)



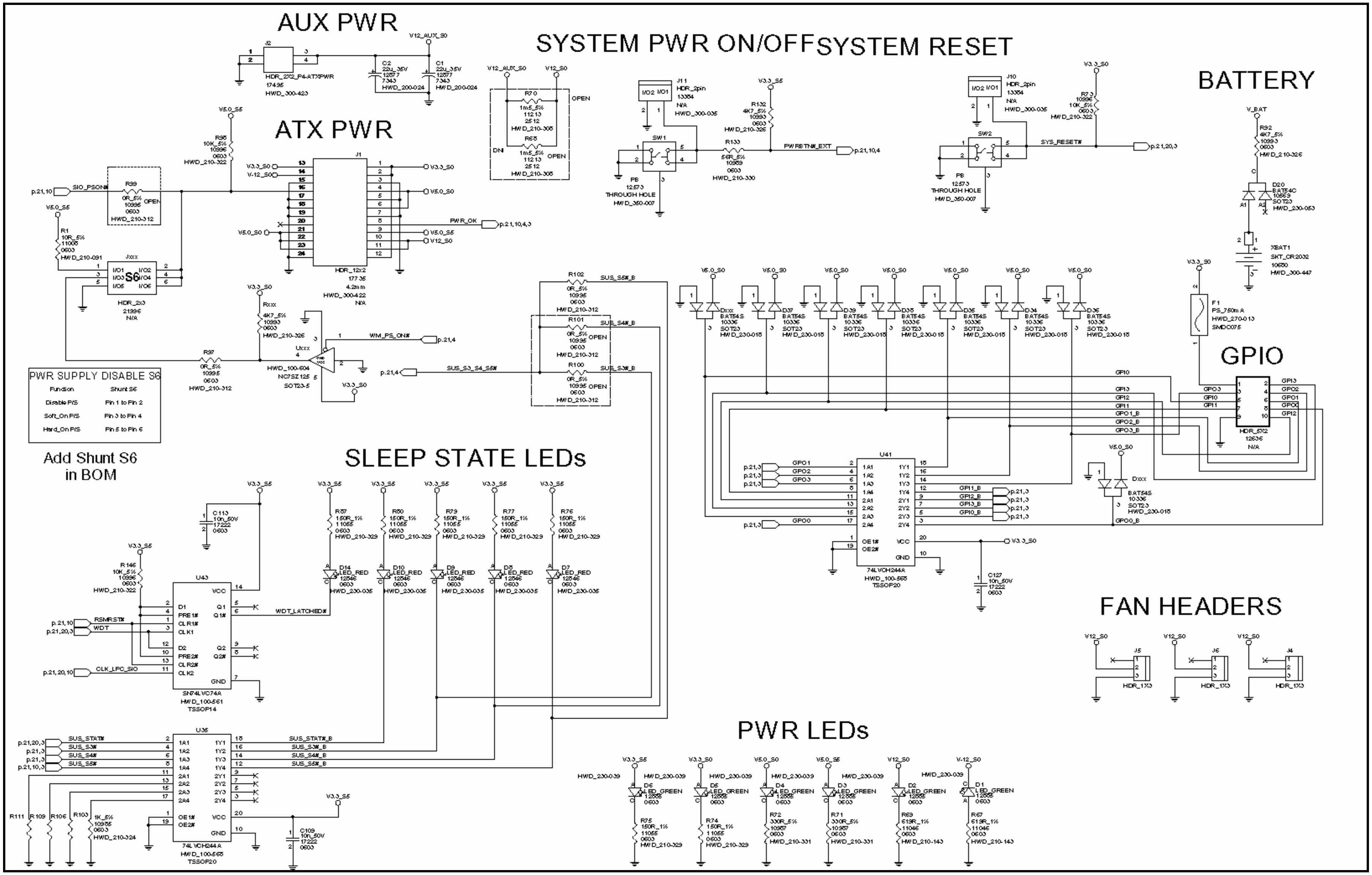
25.21 LPC Slot and Firmware Hub Schematics

Figure 25-21: Slot and Firmware Hub Schematics (Sheet 20 of 21)



25.22 Power and Miscellaneous Schematics

Figure 25-22: Power and Miscellaneous Schematics (Sheet 21 of 21)



26 Appendix F – PLD Program for Post Codes

```
--------------------------------------------------------------------------------
-- IO80 catcher for LPC bus.
--
-- File:  LPC_IOW80_1.1.VHD
-- Revision:  1.1
--
-- Author:   Eric Leonard (partially based on Nicolas Gonthier's T3001)
--           Subsequent modifications by:
--            Detlef Herbst and Travis Evans - 08/10/05
--
-- Decode only I/O writes to 80h
--
-- Features:
--    - I/O 80 access only (internally decoded)
--    - No support for read, only write.
--    - All signals synchronous to LPC clock
--
-- Notes:
--    - Unless otherwise noted, all signals are active high.
--    - Suffix "n" indicate active low logic.
--
-- Testing
--    - Successfully implemented on Brownsville baseboard with Seven Segment
--    - display P/N SA39-11 (common Anode - Low turns on segment) from Kingbright
--
-- Related documents:
--      - Low Pin Count (LPC) Interface Specification, Revision 1.0 (sept 1997)
--
--
--
--------------------------------------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.all;

entity LPC_IOW80 is port (
  lclk:        in     std_logic;                    -- LPC: 33MHz clock (rising edge)
  lframe_n:    in     std_logic;                    -- LPC: frame, active low
  lreset_n:    in     std_logic;                    -- LPC: reset, active low
  lad:         in     std_logic_vector(3 downto 0); -- LPC: multiplexed bus
  seven_seg_L: out    std_logic_vector(7 downto 0); -- SSeg Data output
  seven_seg_H: out    std_logic_vector(7 downto 0)  -- SSeg Data output
);
```

```
end LPC_IOW80;

architecture RTL of LPC_IOW80 is

        type LPC_State_Type is (
                IDLE,           -- Waiting for a start condition
                START,          -- Start condition detected
                WADDN3,         -- I/O write address nibble 3 (A15..A12)
                WADDN2,         -- I/O write address nibble 2 (A11..A8 )
                WADDN1,         -- I/O write address nibble 1 (A7..A4)
                WADDN0,         -- I/O write address nibble 0 (A3-A0)
                WDATN1,         -- I/O write data nibble 0 (D7..D4)
                WDATN0,         -- I/O write data nibble 1 (D3..D0)
                WHTAR0,         -- I/O write host turn around phase 0
                WHTAR1,         -- I/O write host turn around phase 1
                WSYNC,          -- I/O write sync
                WPTAR );        -- I/O write peripheral turn around

        signal LPC_State: LPC_State_Type;

        signal lframe_nreg:    std_logic;                           -- LPC frame register
        signal lad_rin:                std_logic_vector(lad'range);  -- LPC input registers
        signal W_Data:         std_logic_vector(7 downto 0);        -- LPC input Post Code

begin

---------------------------------------------------------------------------
-- LPC bidirectionnal pins definition.
---------------------------------------------------------------------------

-- Input register to get some timing margin
P_input_register: process(lclk)
begin
        if (lclk'event and lclk='1') then
                lad_rin     <= lad;
                lframe_nreg <= lframe_n;
        end if;
end process;
```

```
---------------------------------------------------------------------------
-- LPC state machine
-- LPC_State value is actually one clock cycle late.
---------------------------------------------------------------------------
P_LPC_StatMachine: process(lclk)

begin
  if (lclk'event and lclk='1') then

        -- Synchronous reset
        if (lreset_n = '0') then
                LPC_State <= IDLE;
                W_Data(7 downto 0) <= "00000000";     -- init. both displays to all on
                else
                        case LPC_State is

                          -- Looking for a START condition
                          when IDLE =>

                                if (lframe_nreg = '0') and (lad_rin = "0000") then
                                        LPC_State <= START;    -- START condition detected
                                        end if;

                                -- Skip extra cycles on START frame
                                -- (can be many clock cycles)
                                -- and then, check for I/O write transaction
                            when START =>
                                        if (lframe_nreg = '0') then -- frame still asserted
                                                if (lad_rin /= "0000") then
                                                LPC_State <= IDLE; -- unsupported start code
                                                end if;
                                        else
                                        if (lad_rin(3 downto 1) = "001") then
                                                LPC_State <= WADDN3;   -- I/O write detected
                                                else
                                                LPC_State <= IDLE;     -- unsupported command
                                                end if;
                                        end if;
```

```
-- -------------------------------
-- I/O write transaction processing
-- -------------------------------
when WADDN3 => -- Write Data Address Nibble 3

       -- Find next state
       if (lframe_nreg = '0') or (lad_rin /= "0000") then
       LPC_State <= IDLE; -   -- abort cycle, bad frame
                              -- or address mismatch
       else
              LPC_State <= WADDN2;
       end if;

when WADDN2 =>        -- Write Data Address Nibble 2

       -- Find next state
       if (lframe_nreg = '0') or (lad_rin /= "0000") then
              LPC_State <= IDLE; -- abort cycle, bad frame
                                  -- or address mismatch
       else
              LPC_State <= WADDN1;
       end if;

when WADDN1 =>        -- Write Data Address Nibble 1

       -- Find next state
       if (lframe_nreg = '0') or (lad_rin /= "1000") then
              LPC_State <= IDLE; -- abort cycle, bad frame
                                  -- or address mismatch
       else
              LPC_State <= WADDN0;
       end if;

when WADDN0 =>        -- Write Data Address Nibble 0

       -- Find next state
       if (lframe_nreg = '0') or (lad_rin /= "0000") then
              LPC_State <= IDLE; -- abort cycle, bad frame
                                  -- or address mismatch
       else
       -- Write address valid. Subsequent Data displays.
              LPC_State <= WDATN0;   -- Next state will get
                                     -- first data nibble
       end if;
```

```
when WDATN0 => -- Data LSN (Least Significant Nibble)is
               -- sent first
       W_Data(3 downto 0) <= lad_rin; -- latch data (LSN)
       if (lframe_nreg = '1') then
         LPC_State <= WDATN1; -- Next state gets
                                -- 2nd data nibble
       else
              LPC_State <= IDLE;
       end if;

when WDATN1 =>  -- Data MSN (Most Significant Nibble)
       W_Data(7 downto 4) <= lad_rin; -- latch data (MSN)
       if (lframe_nreg = '1') then
              LPC_State <= WHTAR0;
       else
              LPC_State <= IDLE;
       end if;

when WHTAR0 =>  -- Write Data Turn Around Cycle 0

       if (lframe_nreg = '1') and (lad_rin = "1111") then
              LPC_State <= WHTAR1;
       else
              LPC_State <= IDLE;
       end if;

when WHTAR1 =>   -- Write Data Turn Around Cycle 1

       if (lframe_nreg = '1') then
              LPC_State <= WSYNC;
       else
              LPC_State <= IDLE;
       end if;

when WSYNC =>  -- Write Data Sync Cycle
-- Note: No device to respond with a synch at I\O addr
-- 080h. Therefore bus should time out and abort.
-- State ==> to IDLE
       if (lframe_nreg = '1') then
              LPC_State <= WPTAR;
       else
              LPC_State <= IDLE;
       end if;
```

```
                                when WPTAR =>  -- Write Data Final Turn Around Cycle
                                               -- (not needed -- see WSYNC)
                                        LPC_State <= IDLE;     -- I/O write cycle end

                                when others =>
                                        LPC_State <= IDLE;     -- all other cases
                        end case;
                end if;
        end if;
end process;

P_sseg_decode: process(lclk)                         -- decode section for 7 seg displays
begin
        if (lclk'event and lclk='1') then

                case W_Data(7 downto 4) is                   -- Most sig digit for display
                        when    "0000" => seven_seg_H <= "00000011";  -- Hex 03 displays a 0
                        when    "0001" => seven_seg_H <= "10011111";  -- Hex 9f displays a 1
                        when    "0010" => seven_seg_H <= "00100101";  -- Hex 25 displays a 2
                        when    "0011" => seven_seg_H <= "00001101";  -- Hex 0d displays a 3
                        when    "0100" => seven_seg_H <= "10011001";  -- Hex 99 displays a 4
                        when    "0101" => seven_seg_H <= "01001001";  -- Hex 49 displays a 5
                        when    "0110" => seven_seg_H <= "01000001";  -- Hex 41 displays a 6
                        when    "0111" => seven_seg_H <= "00011111";  -- Hex 1f displays a 7
                        when    "1000" => seven_seg_H <= "00000001";  -- Hex 01 displays a 8
                        when    "1001" => seven_seg_H <= "00001001";  -- Hex 09 displays a 9
                        when    "1010" => seven_seg_H <= "00010001";  -- Hex 11 displays a A
                        when    "1011" => seven_seg_H <= "11000001";  -- Hex c1 displays a b
                        when    "1100" => seven_seg_H <= "01100011";  -- Hex 63 displays a C
                        when    "1101" => seven_seg_H <= "10000101";  -- Hex 85 displays a d
                        when    "1110" => seven_seg_H <= "01100001";  -- Hex 61 displays a E
                        when    "1111" => seven_seg_H <= "01110001";  -- Hex 71 displays a F
                        when    others => seven_seg_H <= "00000001";  -- Hex 01 displays a 8

                end case;
```

```
                    case W_Data(3 downto 0) is                    -- Least sig digit for display
                            when    "0000" => seven_seg_L <= "00000011";  -- Hex 03 displays a 0
                            when    "0001" => seven_seg_L <= "10011111";  -- Hex 9f displays a 1
                            when    "0010" => seven_seg_L <= "00100101";  -- Hex 25 displays a 2
                            when    "0011" => seven_seg_L <= "00001101";  -- Hex 0d displays a 3
                            when    "0100" => seven_seg_L <= "10011001";  -- Hex 99 displays a 4
                            when    "0101" => seven_seg_L <= "01001001";  -- Hex 49 displays a 5
                            when    "0110" => seven_seg_L <= "01000001";  -- Hex 41 displays a 6
                            when    "0111" => seven_seg_L <= "00011111";  -- Hex 1f displays a 7
                            when    "1000" => seven_seg_L <= "00000001";  -- Hex 01 displays a 8
                            when    "1001" => seven_seg_L <= "00001001";  -- Hex 09 displays a 9
                            when    "1010" => seven_seg_L <= "00010001";  -- Hex 11 displays a A
                            when    "1011" => seven_seg_L <= "11000001";  -- Hex c1 displays a b
                            when    "1100" => seven_seg_L <= "01100011";  -- Hex 63 displays a C
                            when    "1101" => seven_seg_L <= "10000101";  -- Hex 85 displays a d
                            when    "1110" => seven_seg_L <= "01100001";  -- Hex 61 displays a E
                            when    "1111" => seven_seg_L <= "01110001";  -- Hex 71 displays a F
                            when    others => seven_seg_L <= "00000001";  -- Hex 01 displays a 8

                    end case;
            end if;
    end process;

end RTL;
```

27 Appendix G – Applicable Documents and Standards

The following publications are used in conjunction with this manual. When any of the referenced specifications are superseded by an approved revision, that revision shall apply. All documents may be obtained from their respective organizations.

- Advanced Configuration and Power Interface Specification Revision 2.0c, August 25, 2003 Copyright © 1996-2003 Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Ltd., Toshiba Corporation. All rights reserved. http://www.acpi.info/

- ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001. http://www.ansi.org/

- ANSI INCITS 361-2002: AT Attachment with Packet Interface - 6 (ATA/ATAPI-6), November 1, 2002. http://www.ansi.org/

- ANSI INCITS 376-2003: American National Standard for Information Technology – Serial Attached SCSI (SAS), October 30, 2003. http://www.ansi.org/

- ATX12V Power Supply Design Guide, Version 2.2, March 2005, Copyright © 2002-2005 Intel Corporation. Available at www.formfactors.org

- ATX Specification, Version 2.2, Copyright © 2003-2004 Intel Corporation. Available at www.formfactors.org

- Audio Codec '97 Revision 2.3 Revision 1.0, April 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://www.intel.com/labs/media/audio/

- Display Data Channel Command Interface (DDC/CI) Standard (formerly DDC2Bi) Version 1, August 14, 1998 Copyright © 1998 Video Electronics Standards Association. All rights reserved. http://www.vesa.org/summary/sumddcci.htm

- Express Card Standard Release 1.0, December 2003 Copyright © 2003 PCMCIA. All rights reserved. http://www.expresscard.org/

- IEEE 802.3-2002, IEEE Standard for Information technology, Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications." http://www.ieee.org

- Intel Low Pin Count (LPC) Interface Specification Revision 1.1, August 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://developer.intel.com/design/chipsets/industry/lpc.htm

- IPC-2221 Generic Standard On Printed Circuit Board Design, Revision A, May 2003, IPC, www.ipc.org

- JIDA, Technical Specification Nr. X00391.DOC, Revision 2.7, file name jida.pdf, available from your Kontron FAE.

- JIDA32, Kontron JIDA32 Library API Technical Manual, Revision 1.5, file name jida32.pdf, available from your Kontron FAE.

- JIDA32 BIOS Specification, Technical Specification Nr. X01363.DOC, file name X01363_Jida_BIOS_Spec.pdf, available from your Kontron FAE.

- JILI, Revision 2.0, 07-April-2003 Copyright © 2003 Kontron Embedded Computers AG. http://www.jumptec.de/product/data/jili/Jilim120.pdf

- microATX Motherboard Interface Specification, Version 1.2, Copyright © 2003-2004 Intel Corporation. Available at www.formfactors.org

- Open LVDS Display Interface (Open LDI) Specification, v0.95, May 13, 1999, Copyright © National Semiconductor. http://www.national.com

- PC/104-*Plus* Specification, Version 2.0, November 2003, Copyright © 1992-2003, PC/104 Embedded Consortium. www.pc104.org

- PCI Express Base Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/

- PCI Express Card Electromechanical Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/

- PCI Local Bus Specification Revision 2.3, March 29, 2002 Copyright © 1992, 1993, 1995, 1998, 2002 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/

- PICMG COM.0 R1.0, "COM Express Module Base Specification", July 10, 2005, www.picmg.org Paper copies are available for purchase at the PICMG web site for $95 for non-PICMG members, $45 for PICMG members. PDF copies are available to PICMG members only and are more expensive ($250 to Executive Members and $500 to Affiliate Members).

- Serial ATA: High Speed Serialized AT Attachment Revision 1.0a January 7, 2003 Copyright © 2000-2003, APT Technologies, Inc., Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved. http://www.sata-io.org/

- Smart Battery Data Specification Revision 1.1, December 11, 1998. www.sbs-forum.org

- System Management Bus (SM Bus) Specification Version 2.0, August 3, 2000 Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, PowerSmart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc. All rights reserved. http://www.smbus.org/

- The I^2C Bus Specification, Version 2.1, January 2000, Philips Semiconductors, Document order number 9398 393 4001 1. http://www.semiconductors.philips.com

- Universal Serial Bus Specification Revision 2.0, April 27, 2000 Copyright © 2000 Compaq Computer Corporation, Hewlett-Packard Company, Intel Corporation, Lucent Technologies Inc, Microsoft Corporation, NEC Corporation, Koninklijke Philips Electronics N.V. All rights reserved. http://www.usb.org/

- VESA Enhanced EDID Standard, Video Electronics Standards Organization, www.vesa.org

- VESA Enhanced Extended Display Identification Guide, Version 1.0, June 4, 2001, Copyright © 2001 Video Electronics Standards Organization, www.vesa.org

28 Appendix H – Reference Materials

28.1 General PC Architecture

- *Building the Power-Efficient PC: A Developer's Guide to ACPI Power Management*, First Edition, Jerzy Kolinski, Ram Chary, Andrew Henroid, and Barry Press, Intel Press, 2002, ISBN 0-9702846-8-3
- *Hardware Bible*, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- *The Indispensable PC Hardware Book*, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- *The PC Handbook: For Engineers, Programmers, and Other Serious PC Users*, Sixth Edition, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1
- *PC Hardware in a Nutshell*, 3rd Edition, Robert Bruce Thompson and Barbara Fritchman Thompson, O'Reilly, 2003, ISBN 0-596-00513-X

28.2 PCI

- *PCI & PCI-X Hardware and Software Architecture & Design*, Fifth Edition, Edward Solari and George Willse, Annabooks, Intel Press, 2001, ISBN 0-929392-63-9.
- *PCI System Architecture*, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

28.3 PCIe

- *PCI Express Electrical Interconnect Design: Practical Solutions for Board-level Integration and Validation,* First Edition, Dave Coleman, Scott Gardiner, Mohamad Kolberhdari, and Stephen Peters, Intel Press, 2005, ISBN 0-9743649-9-1
- *Introduction to PCI Express: A Hardware and Software Developer's Guide*, First Edition, Adam Wilen, Justin Schade, and Ron Thornburg, Intel Press, 2003, ISBN 0-9702846-9-1

28.4 Serial ATA

- *Serial ATA Storage Architecture and Applications*, First Edition, Knut Grimsrud and Hubbert Smith, Intel Press, 2003, ISBN 0-9717861-8-6

28.5 USB

- *USB Design by Example*, *A Practical Guide to Building I/O Devices*, Second Edition, John Hyde, Intel Press, ISBN 0-9702846-5-9
- *Universal Serial Bus System Architecture,* Second Edition, Don Anderson and Dave Dzatko, Mindshare, Inc., ISBN 0-201-30975-0

28.6 RS-232 Serial

- *RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems*, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3

28.7 PCB Layout and Signal Integrity

- *Printed Circuits Handbook*, Fourth Edition, Clyde F. Coombs, Jr., McGraw-Hill, 1996, ISBN 0—07-012754-9

- *High Speed Signal Propagation*, First Edition, Howard Johnson and Martin Graham, Prentice Hall, 2003, ISBN 0-13-084408-X

- *High Speed Digital Design: A Handbook of Black Magic,* First Edition, Howard Johnson, Prentice Hall, ISBN: 0133957241

28.8 Programming

- *C Programmer's Guide to Serial Communications*, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0

- *The Programmer's PC Sourcebook*, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X

- *The Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas*, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

28.9 PLD / FPGA Programming

- *VHDL Modeling for Digital Design Synthesis,* Yu-Chin Hsu, Kevin F. Tsai, Jessie T. Liu and Eric S. Lin, Kluwer Academic Publishers, 1995, ISBN: 0-7923-9597-2

29 Appendix I – Informational Web Sites

Table 29-1: Informational Web Sites

Company / Org Name	Product / Information	Web Site URL
AMP / Tyco	All connector types, including ones suitable for COM Express Modules, ETXexpress Carrier Boards, PCIe slot cards, and IDE headers.	www.amp.com
Analog Devices	Reset monitors; thermal monitors	www.analog.com
Atmel	Serial EEPROMs	www.atmel.com
Bel Fuse	Ethernet magnetics	www.belfuse.com
Coilcraft	USB common mode chokes	www.coilcraft.com
Chrontel	SDVO to TMDS (DVI-D) transmitters SDVO to LVDS transmitters SDVO to NTSC transmitters	www.chrontel.com
Cirrus Logic	AC ’97 Codecs	www.cirrus.com
Cypress Semiconductor	Zero delay clock buffers	www.cypress.com
FCI	PCIe connectors Straddle-mount PCIe connectors High-speed mezzanine connectors	www.fciconnect.com
Form Factors	Information on PC form factors (ATX, microATX) and power supplies	www.formfactors.org
JEDEC	Industry standards organization Memory IC and socket standards IC packaging standards	www.jedec.org
ICS	Zero delay clock buffers	www.icst.com
Intel	CPUs, chipsets, and Gigabit Ethernet controllers	www.intel.com
IPC	Printed circuit board standards	www.ipc.org
Kontron	ETXexpress products, application notes, literature. This is the most important Web site on the list.	www.kontron.com
Lattice	Programmable logic devices	www.laticesemi.com
Maxim	Reset supervisory ICs; battery monitoring ICs	www.maxim-ic.com
Meritec	Right-angle PCIe and PCI connectors	www.meritec.com
Molex	Connectors: USB, SATA, PCIe slot connectors, ATX power headers	www.molex.com
National Semiconductor	LVDS receivers Audio amplifiers Super I/O devices Codecs Thermal monitors	www.national.com
Panasonic	Lithium coin cells	www.panasonic.com
PCI-SIG	PCI Special Interest Group Maintains PCI and PCI Express standards	www.pcisig.com
Pericom	PCIe multiplexers, switches, bridges	www.pericom.com
PICMG	COM Express COM.0 standard	www.picmg.org
PLX Technologies	PCIe switches and bridges PCI bridges and I/O interface chips	www.plxtech.com
Polar Instruments	PCB trace impedance calculators	www.polarinstruments.com
Pulse	Ethernet magnetics	www.pulseeng.com
Sigmatel	HD Audio Codecs	www.sigmatel.com
Silicon Image	SDVO to DVI-D transmitters; ADD2 cards	www.siimage.com
SST	Firmware hubs (Flash memory for code storage)	www.sst.com
ST Microelectronics	Firmware hubs (Flash memory for code storage)	www.st.com
Texas Instruments	USB Current Limit Switches LVDS receivers	www.ti.com
Thine	LVDS receivers	www.thine.co.jp
Vesa	Video Electronics Standards Association Video standards, flat-panel display standards	www.vesa.org
Winbond	Super I/O devices	www.winbond.com.tw
Xilinx	FPGAs and PLDs	www.xilinx.com

30 Appendix J – Document Revisions

Table 30-1: Document Revisions

Rev.	Date	By	Action
0.1	June 3, 2005	JP and JL / Kontron America	Released Preliminary Version 0.1 of Design Guide for ETXexpress Carrier Boards.
1.0	March 6, 2006	SM and JL Kontron America	Released V. 1.0 of Design Guide for ETXexpress Carrier Boards.
1.1	March 31, 2006	SM and JL Kontron America	Corrected an error in Figure 7.2 and an error in Figure 16.3.