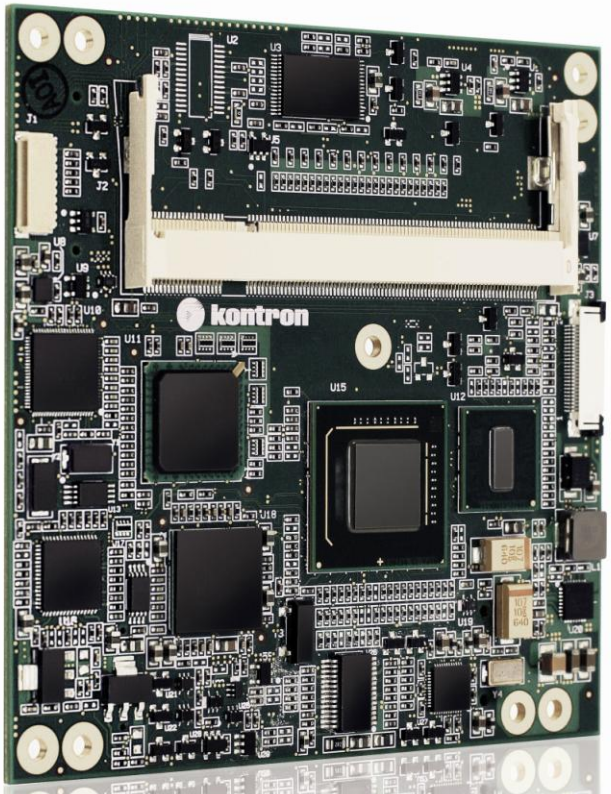
» Kontron User's Guide «



COMe-cSP2

Document Revision 120

If it's embedded, it's Kontron.

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1 User Information

1.1 About This Document

This document provides information about products from Kontron Embedded Modules GmbH and/or its subsidiaries. No warranty of suitability, purpose, or fitness is implied. While every attempt has been made to ensure that the information in this document is accurate, the information contained within is supplied "as-is" and is subject to change without notice.

For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

1.2 Copyright Notice

1.3 Trademarks

The following lists the trademarks of components used in this board.

- IBM, XT, AT, PS/2 and Personal System/2 are trademarks of International Business Machines Corp.
- Microsoft is a registered trademark of Microsoft Corp.
- Intel is a registered trademark of Intel Corp.
- All other products and trademarks mentioned in this manual are trademarks of their respective owners.

1.4 Standards

Kontron Embedded Modules GmbH is certified to ISO 9000 standards.

1.5 Warranty

This Kontron Embedded Modules GmbH product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Embedded Modules GmbH will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron Embedded Modules GmbH will not be responsible for any defects or damages to other products not supplied by Kontron Embedded Modules GmbH that are caused by a faulty Kontron Embedded Modules GmbH product.

1.6 Technical Support

Technicians and engineers from Kontron are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Please consult our Web site at http://www.kontron.com/support for the latest product documentation, utilities, drivers and support contacts. Consult our customer section for the latest BIOS downloads, Product Change Notifications and additional tools and software. This section is exclusively for registered Kontron customers and accessible from product web page on www.kontron.com.

In any case you can always contact your board supplier for technical support.

2 Introduction

2.1 COMe-cSP2

The Kontron COMe-cSP2 Computer-on-Module is designed to extend the COM Express® specification to include a small module format (95 x 95 mm) with the commonly used COM Express® Type 2 connector. This will enable the development of energy-saving, high-end graphics devices based on the Intel® Atom™ processor (up to 1.6GHz) and the Intel® System Controller Hub US15W without having to stray from the secure development path of utilizing an established and future-proof industry standard.

The Kontron COMe-cSP2 offers LVDS as well as more sophisticated graphics support with SDVO. SDVO delivers additional video signals for DVI monitor outputs, SDTV and HDTV television outputs and TV tuner inputs that greatly simplify system graphics design. This special feature makes this 95 x 95 mm Computer-on-Module ideal for small mobile and extremely energy-efficient multimedia devices as well as for mobile test and measurement applications. Other standard features of the COMe-cSP2 include: Gigabit Ethernet, Serial ATA, single-channel LVDS and USB 2.0.

All Kontron microCOM Express® family modules are compatible with the COM Express® standard (Pin-out Type 2) allowing for easy interchangeability and ensuring design scaleability and future migration paths.

The COMe-cSP2 is a complete PC with standard interfaces including USB and additional options such as sound capabilities, flat panel interface, Ethernet, etc.

2.2 Understanding COMe-cSP2 functionality

All Kontron COM Express® basic and compact modules contain two connectors; each of it has two rows. The primary connector has two rows called Row A and Row B. The secondary connector has two rows called Row C and Row D. The primary connector (Row A and Row B) feature the following legacy-free functionality:

- Ethernet
- Serial ATA (SATA)
- USB 2.0
- LVDS/VGA and dual display video
- Intel High Definition Audio (Azalia)
- LPC (low pin count) Bus
- PCIexpress

The secondary connector (Row C and Row D) provides support for the following buses and I/O:

- PCI Express
- PCI
- IDE

2.3 COM Express® Documentation

This product manual serves as one of three principal references for a COM Express® design. It documents the specifications and features of COMe-cSP2. The other two references, which are available from your Kontron Support or from PICMG®, include:

- The COM Express Specification defines the form factor, pinout, and signals. This document is available from the PIGMG website by filling out the order form.
- The COM Express® Carrier Board Design Guide by PICMG serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of COM Express® modules.

Note:	Some of the information contained within this product manual applies only to certain product revisions (CE: xxx). If certain information applies to specific product revisions (CE: xxx) it will be stated. Please check the product revision of your module to see if this information is applicable.

2.4 COM Express® Benefits

COM Express® Computer-on-Modules in compact form factor are very compact (95 x 95 mm), highly integrated computers. All COM Express® compact modules feature a standardized form factor and a standardized connector layout that carry a specified set of signals.

Modules include common personal computer (PC) peripheral functions such as:

- Graphics
- USB ports
- Ethernet
- Sound
- IDE and SATA

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

A peripheral PCI bus can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard using the computer as one plug-in component simplifies packaging, eliminates cabling, and significantly reduces system-level cost.

A single baseboard design can use a range of COM Express® basic, compact and mini form factor modules. This flexibility can differentiate products at various price/performance points, or to design future proof systems that have a built-in upgrade path. The modularity of a COM Express® solution also ensures against obsolescence as computer technology evolves. A properly designed COM Express® baseboard can work with several successive generations of COM Express® modules.

A COM Express® baseboard design offers many of the advantages of a custom, computer board design, but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

3 Specification

3.1 Functional Specification

Processor: Intel® Atom™ Zxx

- » CPU: 45nm Silverthorne Z510 (1.1 GHz) or Z530 (1.6 GHz)
- » Cores: 1
- » Bus Speed: 400 / 533 MHz
- » Bus/Core Ratio: 11 / 12
- » Cache: 32 kByte Instruction Cache + 24 kByte L1 Cache 512 kByte L2 Cache
- » Features: Hyper-Threading Technology (Z530 only)
  Intel® Virtualization Technology
  Execute Disable Bit
  Enhanced Intel® Speedstep Technology
  C-States: C0, C1/C1E, C2/C2E, C3, C4/C4E, Intel Deep Power Down State C6
- » Instruction Set: 32-bit
- » Package: 13mm x 14mm PBGA441
- » Max TDP: 2W
- » Thermal Spec: 90°C

Chipset: Intel® System Controller Hub US15W (Poulsbo)

- » Speed: 400 / 533 MHz FSB
- » RAM: One DDR2 400/533MHz SO-DIMM Socket up to 2048MByte (8 chip configuration only)
- » USB: 6 x USB 1.1/2.0 (1x USB Client) + 2 x USB 2.0 only
- » Audio: Intel® High Definition Audio (24 bit / 96 kHz)
- » PCI Express: 1 x PCIexpress x1 to COM Express® Lane #1
  1 x PCIexpress x1 used onboard for PCIexpress Hub
- » Max TDP: 2.3W

Integrated graphics Intel® GMA500

- » Graphics Memory: up to 352 MByte with IEGD, up to 256MB with GMA
- » Features: HDTV/HD capable, Decoder for MPEG2(HD) / H.264, DirectX®9.0c, OpenGL 2.0

Display Interfaces

- » CRT: VGA is not supported my the US15W System Controller Hub
- » Flat Panel: Single Channel LVDS 18/24 Bit, resolution up to 1366 x 768 (WXGA), no dithering.
- » Digital Display: Only SDVO supported on SDVO/PEG Interface on connector CD with resolution up to FullHD 1920x1080.

Storage

- » IDE: Primary IDE (Master/Slave) from the US15W SCH with UDMA 100/66/33 support
- » SATA: 2x Serial ATA supporting up to 3.0 GBit/s transfer rate (SIL 3132 PCIe2SATA Bridge)
- » SATA Features: Boot, RAID0, RAID1, NCQ, Staggered Spinup, Port Multiplier

Onboard devices:

- » Ethernet: Intel® 82574L (Hartwell), 10/100/1000 Mbit Ethernet (Max TDP 0.727W)
  Features: WakeOnLAN, PXE Lanboot, Time Sync Protocol Indicator, Jumbo Frames
- » TPM: Infineon SLB9635TT1 Trusted Platform Module 1.2 onboard
- » Watchdog: integrated in onboard CPLD, possible delay: 1s, 5s, 10s, 30s, 1min, 5min, 10min, 15min
- » PCI: PCIe-to-PCI Bridge PLX Technology PEX8112 (0.4W typical, 32bit/33MHz PCI 3.0)
- » PCIe Switch: 8 Port PCIe Switch PLX Technology PEX8509 (1.2W typical, PCIe Gen1 with 2.5Gb/s, Link Power Management L0-L3, Device Power Management D0-D3hot)
- » Optional: 4 Port PCIe Switch PEX8505 (without support for PCIe Lane #2-4 on COMe connector)

Additional Interfaces:

- » LPC: Yes
- » SMBus: Yes
- » I2C: Fast I2C (from US15W SCH)
- » GPIO: 8 GPIO, 4 GPI and 4 GPO
- » SDIO: 1x onboard miniSD Card Socket (US15W SDIO port #0)
  1x SDIO port shared with GPIO signals (US15W SDIO port #1)
  SD Card Specification 1.1
  SDIO boot supported

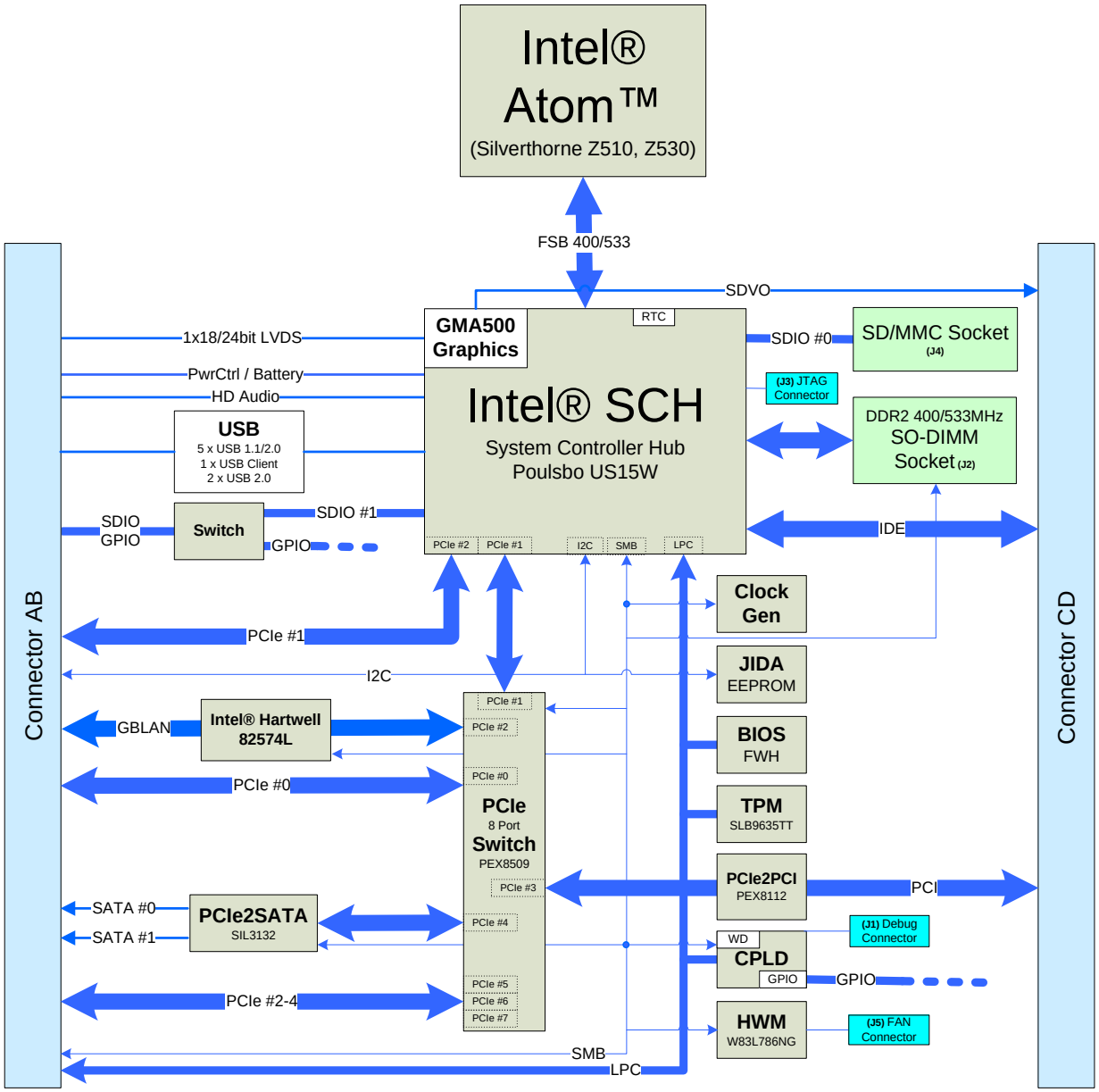
Power Management & Misc

- » JIDA: Yes
- » K-Station: Yes
- » Bootlogo: Yes
- » MARS: Yes, Charger & Manager Support
- » HWM: Temperature Monitoring for CPU and Board Temperature (onboard W83L786 HWM)
  HWM for external Winbond 83627
- » Passive Cooling: Passive and Critical Trip Point
- » ACPI: ACPI 1.0 / 2.0 / 3.0
- » S-States: S0, S3, S4, S5
- » Input Voltage: Single supply support with wide range input 8,5 V - 18 V

3.1.1 Available Modules

Part No	CPU	Features
36003-0000-11-1	Intel® Atom™ Z510 1.1GHz	US15W SCH
36003-0000-16-1	Intel® Atom™ Z530 1.6GHz	US15W SCH
36003-0000-11-4	Intel® Atom™ Z510 1.1GHz	US15W SCH (US version)
36003-0000-16-4	Intel® Atom™ Z530 1.6GHz	US15W SCH (US version)

3.2 Block Diagram



3.3 Mechanical Specification

Module Dimensions

» 95 mm x 95 mm ±0.2 mm

Height on Top

» Maximum approx. 5 mm (without printed circuit board)

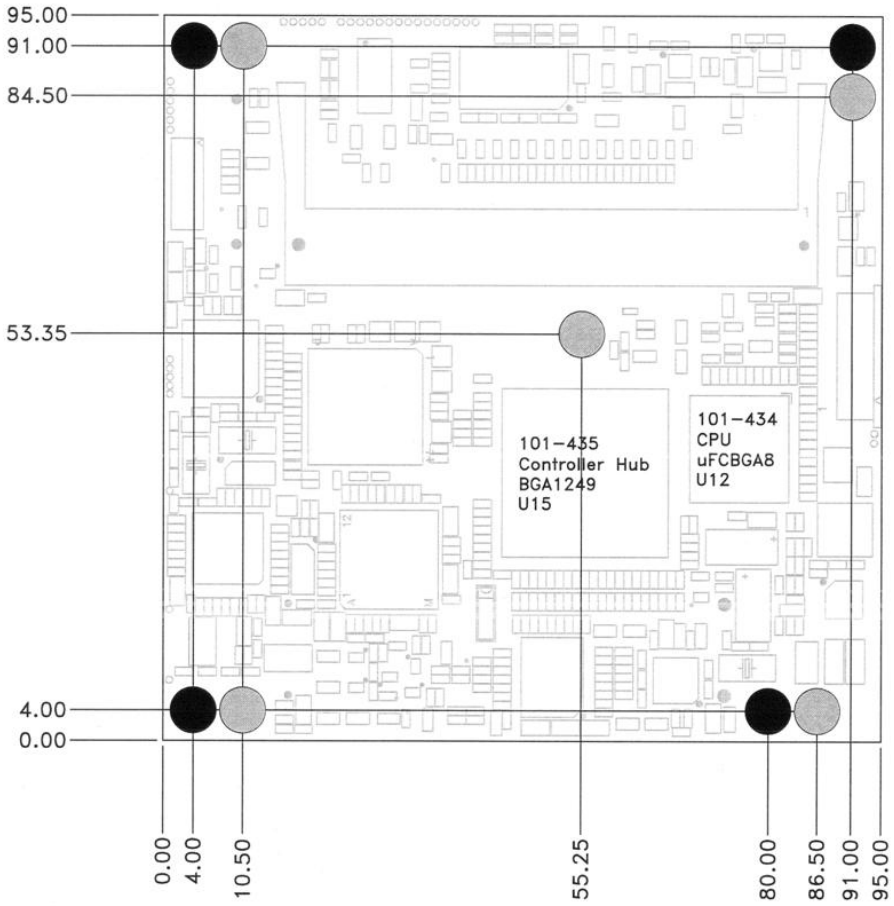
» Highest component: memory socket

» Height is depending upon optionally CPU cooler/heatpreader

Height on Bottom

» Maximum approx. 4.06 mm (without printed circuit board)

Mechanical Drawing



All dimensions are shown in millimetres. Tolerances should be ± 0.25mm [±0.010"], unless otherwise noted. The tolerances on the module connector locating peg holes (dimensions [16.50, 6.00]) should be ± 0.10mm [±0.004"]. The 220 pin connector shall be mounted on the backside of the PCB and is seen "through" the board in this view. The 4 mounting holes shown in the drawing should use 6mm diameter pads and should have 2.7mm plated holes, for use with 2.5mm hardware. The pads should be tied to the PCB ground plane. Gray circles represent the mechanical mounting holes. Black circles represent the mounting holes required by the PICMG COM Express® standard.

Note: A complete SolidWorks eDrawing package is available at EMD Customer Section
http://emdcustomersection.kontron.com

3.4 Electrical Specification

3.4.1 Supply Voltage

» 8.5 V to 18 V DC in single supply mode

» VCC + 5VSB ±5% in ATX mode (VCC > 5VSB)

Note: If a module is E1 rated and should be used in E1 temperature range the supply voltage must be 12V +- 5%!

Power Supply Risetime

» The input voltages shall increase from ≤10% of nominal to within the regulation ranges within 0.1ms to 20ms.

» There must be a smooth and continuous ramp of each DC input voltage from 10% to 90% of its final set-point following the ATX specification

Supply Voltage Ripple

» Maximum 100 mV peak to peak 0-20MHz

3.4.2 Environmental Specification

Temperature

Operating: (with Kontron Embedded Modules GmbH heat-spreader plate assembly):

- » Ambient temperature: 0 to +60 °C
- » Maximum heatspreader-plate temperature: 0 to +60 °C (*)
- » Non-operating: -30 to +85 °C

Note: *The maximum operating temperature with the heatspreader plate is the maximum measurable temperature on any spot on the heatspreader's surface. You must maintain the temperature according to the above specification.

Operating (without Kontron Embedded Modules GmbH heat-spreader plate assembly):

- » Maximum operating temperature: 0 to +60 °C (**)
- » Non operating: -30 to +85 °C

Note: **The maximum operating temperature is the maximum measurable temperature on any spot on a module's surface. You must maintain the temperature according to the above specification.

Humidity

- » Operating: 10% to 90% (non condensing)
- » Non operating: 5% to 95% (non condensing)

3.5 MTBF

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturers' test data, where available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50% stress level in a 40°C ambient environment and the system is assumed to have not been burned in. The component manufacturers' data has been used wherever possible. The manufacturer's data, when used, is specified at 50°C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40°C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

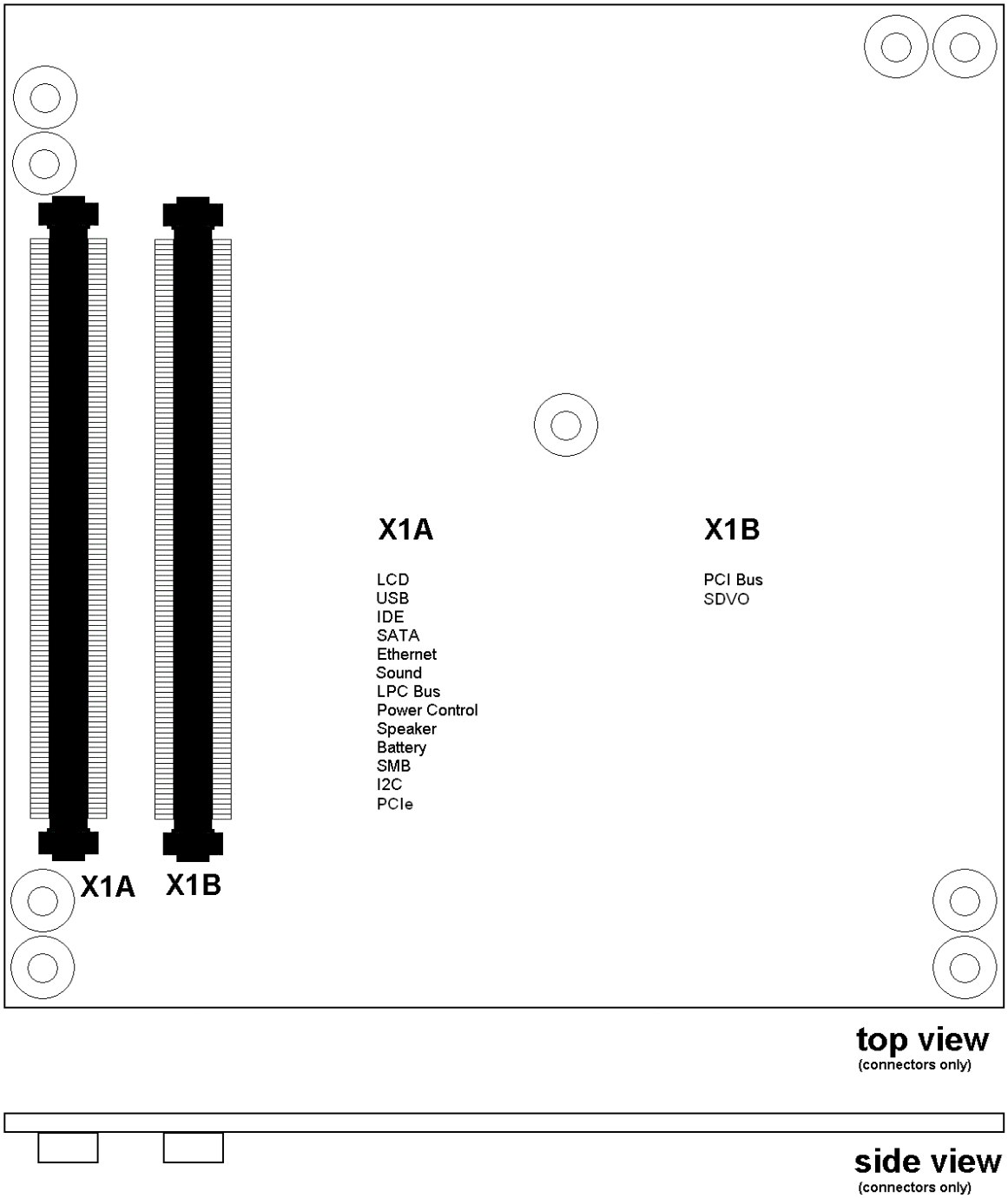
» System MTBF (hours) : **191717 hours @ 40°C**

Note: Fans provided by Kontron have 50,000-hour typical operating life. The above estimates assume a passive heat sinking arrangement (no fan). Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and needs to be considered separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power, the only battery drain is from leakage paths.

4 COMe-cSP2 Connector

See the COM Express® Specification and COM Express® Design Guide for detailed, design-level information.

4.1 Connector Locations



4.2 Pinout List

4.2.1 General Signal Description

Type	Description
I/O-3,3	Bi-directional 3,3 V IO-Signal
I/O-5T	Bi-dir. 3,3V I/O (5V Tolerance)
I/O-5	Bi-directional 5V I/O-Signal
I-3,3	3,3V Input
I/OD	Bi-directional Input/Output Open Drain
I-5T	3,3V Input (5V Tolerance)
OA	Output Analog
OD	Output Open Drain
O-1,8	1,8V Output
O-3,3	3,3V Output
O-5	5V Output
DP-I/O	Differential Pair Input/Output
DP-I	Differential Pair Input
DP-O	Differential Pair Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection
nc	Not Connected, Signal not available

Notes: To protect external power lines of peripheral devices, make sure that: the wires have the right diameter to withstand the maximum available current the enclosure of the peripheral device fulfills the fire-protection requirements of IEC/EN60950

4.2.2 Connector X1A - Row A

Pin	Signal	Description	Type	Termination	Comment
A1	GND_1	Power Ground	PWR	-	-
A2	GBE0_MDI3-	Ethernet Receive Data-	DP-I	-	-
A3	GBE0_MDI3+	Ethernet Receive Data+	DP-I	-	-
A4	GBE0_LINK100#	Ethernet Speed LED 100Mbps	O-3.3	-	-
A5	GBE0_LINK1000#	Ethernet Speed LED 1000Mbps	O-3.3	-	-
A6	GBE0_MDI2-	Ethernet Receive Data-	DP-I	-	-
A7	GBE0_MDI2+	Ethernet Receive Data+	DP-I	-	-
A8	GBE0_LINK#	LAN Link LED	OD	-	-
A9	GBE0_MDI1-	Ethernet Receive Data-	DP-I	-	-
A10	GBE0_MDI1+	Ethernet Receive Data+	DP-I	-	-
A11	GND_2	Power Ground	PWR	-	-
A12	GBE0_MDI0-	Ethernet Transmit Data-	DP-O	-	-
A13	GBE0_MDI0+	Ethernet Transmit Data+	DP-O	-	-
A14	GBE0_CTREF	LAN Reference Voltage	O-1.8	is on a power rail controlled	-
A15	SUS_S3#	Indicates Suspend to RAM state	O-3.3	-	CPLD I/O
A16	SATA0_TX+	SATA 0 Transmit Data+	DP-O	-	-
A17	SATA0_TX-	SATA 0 Transmit Data-	DP-O	-	-
A18	SUS_S4#	Indicates Suspend to Disk state	O-3.3	-	CPLD I/O
A19	SATA0_RX+	SATA 0 Receive Data+	DP-I	-	-
A20	SATA0_RX-	SATA 0 Receive Data-	DP-I	-	-
A21	GND_3	Power Ground	PWR	-	-
A22	SATA2_TX+	Not Connected	nc	-	not supported
A23	SATA2_TX-	Not Connected	nc	-	not supported
A24	SUS_S5#	Indicates Soft Off state	O-3.3	-	CPLD I/O
A25	SATA2_RX+	Not Connected	nc	-	
A26	SATA2_RX-	Not Connected	nc	-	
A27	BATLOW#	Indicates low external battery	I-3.3	-	CPLD I/O
A28	ATA_ACT#	SATA, IDE, SD Activity Indicator	O-3.3	CMOS	-
A29	AC_SYNC	HD Audio Sync	O-3.3	PD 22k in US15W	-
A30	AC_RST#	HD Audio Reset	O-3.3	PD 22k in US15W	-
A31	GND_4	Power Ground	PWR	-	-
A32	AC_BITCLK	HD Audio Clock	O-3.3	PD 22k in US15W	24MHz
A33	AC_SDOUT	HD Audio Data	O-3.3	PD 22k in US15W	-
A34	BIOS_DISABLE#	Disable Module BIOS. Enables boot from a BIOS on Baseboard	I-3.3	PU 10k 3.3V	fir external LPC FWH
A35	THRMTRIP#	CPU thermal shutdown indicator	O-3.3	PU 2k 3.3V	-
A36	USB3-	USB Data- Port #3	DP-I/O	PD 15k in US15W	-
A37	USB3+	USB Data+ Port #3	DP-I/O	PD 15k in US15W	-
A38	USB_2_7_OC#	USB Overcurrent Pair 2 / 3	I-3.3	PU 10k 3.3V	-
A39	USB6-	USB Data- Port #6	DP-I/O	PD 15k in US15W	-
A40	USB6+	USB Data+ Port #6	DP-I/O	PD 15k in US15W	-
A41	GND_5	Power Ground	PWR	-	-
A42	USB4-	USB Data- Port #4	DP-I/O	PD 15k in US15W	-
A43	USB4+	USB Data+ Port #4	DP-I/O	PD 15k in US15W	-
A44	USB_4_5_OC#	USB Overcurrent Pair 4 / 5	I-3.3	PU 10k 3.3V	-

A45	USB0-	USB Data- Port #0	DP-I/O	PD 15k in US15W	-
A46	USB0+	USB Data+ Port #0	DP-I/O	PD 15k in US15W	-
A47	VCC_RTC	RTC Power Supply +3V	PWR	-	-
A48	EXCD0_PERST#	PCIe Express Card 0 Reset	O-3.3	-	-
A49	EXCD0_CPPE#	PCIe Express Card 0 Request	I-3.3	PU 8k2 3.3V	-
A50	LPC_SERIRQ	LPC Serial Interrupt Request	IO-3.3	PU 8k2 3.3V	-
A51	GND_6	Power Ground	PWR	-	-
A52	PCIE_TX5+	PCIe lane #5 Transmit+	nc	-	not supported
A53	PCIE_TX5-	PCIe lane #5 Transmit-	nc	-	not supported
A54	SDIO_D0 GPI0	SDIO#0 Data0 General Purpose Input 0	I/O-3.3 I-3.3	PU 75k in US15W PU 10k 3.3V	Bus Switch PI5C3390
A55	PCIE_TX4+	PCIe lane #4 Transmit+	DP-O	-	PCIe Bridge
A56	PCIE_TX4-	PCIe lane #4 Transmit-	DP-O	-	PCIe Bridge
A57	GND_7	Power Ground	PWR	-	-
A58	PCIE_TX3+	PCIe lane #3 Transmit+	DP-O	-	PCIe Bridge
A59	PCIE_TX3-	PCIe lane #3 Transmit-	DP-O	-	PCIe Bridge
A60	GND_8	Power Ground	PWR	-	-
A61	PCIE_TX2+	PCIe lane #2 Transmit+	DP-O	-	PCIe Bridge
A62	PCIE_TX2-	PCIe lane #2 Transmit-	DP-O	-	PCIe Bridge
A63	SDIO_D1 GPI1	SDIO#0 Data1 General Purpose Input 1	I/O-3.3 I-3.3	PU 75k in US15W PU 10k 3.3V	Bus Switch PI5C3390
A64	PCIE_TX1+	PCIe lane #1 Transmit+	DP-O	-	PCIe Bridge
A65	PCIE_TX1-	PCIe lane #1 Transmit-	DP-O	-	PCIe Bridge
A66	GND_9	Power Ground	PWR	-	-
A67	SDIO_D2 GPI2	SDIO#0 Data2 General Purpose Input 2	I/O-3.3 I-3.3	PU 75k in US15W PU 10k 3.3V	Bus Switch PI5C3390
A68	PCIE_TX0+	PCIe lane #0 Transmit+	DP-O	PU 50R inUS15W	-
A69	PCIE_TX0-	PCIe lane #0 Transmit-	DP-O	PU 50R inUS15W	-
A70	GND_10	Power Ground	PWR	-	-
A71	LVDS_A0+	LVDS Channel A (positive)	DP-O	PU 50R inUS15W	-
A72	LVDS_A0-	LVDS Channel A (negative)	DP-O	PU 50R inUS15W	-
A73	LVDS_A1+	LVDS Channel A (positive)	DP-O	PU 50R inUS15W	-
A74	LVDS_A1-	LVDS Channel A (negative)	DP-O	PU 50R inUS15W	-
A75	LVDS_A2+	LVDS Channel A (positive)	DP-O	PU 50R inUS15W	-
A76	LVDS_A2-	LVDS Channel A (negative)	DP-O	PU 50R inUS15W	-
A77	LVDS_VDD_EN	LVDS Panel Power Control	O-3.3	PD 100k	
A78	LVDS_A3+	LVDS Channel A (positive)	DP-O	PU 50R inUS15W	-
A79	LVDS_A3-	LVDS Channel A (negative)	DP-O	PU 50R inUS15W	-
A80	GND_11	Power Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS Channel A Clock+	DP-O	PU 50R inUS15W	-
A82	LVDS_A_CK-	LVDS Channel A Clock-	DP-O	PU 50R inUS15W	-
A83	LVDS_I2C_CK	LVDS I2C Clock (DDC)	IO-3.3	PU 10k 3.3V	-
A84	LVDS_I2C_DAT	LVDS I2C Data (DDC)	IO-3.3	PU 10k 3.3V	
A85	SDIO_D3 GPI3	SDIO# Data3 General Purpose Input 3	I/O-3.3 I-3.3	PU 75k in US15W PU 10k 3.3V	Bus Switch PI5C3390
A86	KBD_RST#	Keyboard Reset	I-3.3	PU 10k 3.3V	-
A87	KBD_A20GATE	A20 gate	I-3.3	PU 10k 3.3V	-
A88	PCIE0_CK_REF+	PCIe Clock (positive)	DP-O	-	100MHz
A89	PCIE0_CK_REF-	PCIe Clock (negative)	DP-O	-	100MHz
A90	GND_12	Power Ground	PWR	-	-

A91	RSVD1	Reserved	nc	-	-
A92	RSVD2	Reserved	nc	-	-
A93	SDIO_Clk GPO0	SDIO#0 Clock General Purpose Output 0	O-3.3 O-3.3	PU 75k in US15W PD 1k	Bus Switch PI5C3390
A94	RSVD3	Reserved	nc	-	-
A95	RSVD4	Reserved	nc	-	-
A96	GND_13	Power Ground	PWR	-	-
A97	VCC_12V_1	12V VCC	PWR	-	-
A98	VCC_12V_2	12V VCC	PWR	-	-
A99	VCC_12V_3	12V VCC	PWR	-	-
A100	GND_14	Power Ground	PWR	-	-
A101	VCC_12V_4	12V VCC	PWR	-	-
A102	VCC_12V_5	12V VCC	PWR	-	-
A103	VCC_12V_6	12V VCC	PWR	-	-
A104	VCC_12V_7	12V VCC	PWR	-	-
A105	VCC_12V_8	12V VCC	PWR	-	-
A106	VCC_12V_9	12V VCC	PWR	-	-
A107	VCC_12V_10	12V VCC	PWR	-	-
A108	VCC_12V_11	12V VCC	PWR	-	-
A109	VCC_12V_12	12V VCC	PWR	-	-
A110	GND_15	Power Ground	PWR	-	-

4.2.3 Connector X1A - Row B

Pin	Signal	Description	Type	Termination	Comment
B1	GND_16	Power Ground	PWR	-	-
B2	GBE0_ACT#	Ethernet Activity LED	OD	-	-
B3	LPC_FRAME#	LPC Frame Indicator	O-3.3	-	-
B4	LPC_AD0	LPC Address / Data Bus	IO-3.3	PU 20k in US15W	-
B5	LPC_AD1	LPC Address / Data Bus	IO-3.3	PU 20k in US15W	-
B6	LPC_AD2	LPC Address / Data Bus	IO-3.3	PU 20k in US15W	-
B7	LPC_AD3	LPC Address / Data Bus	IO-3.3	PU 20k in US15W	-
B8	LPC_DRQ0#	Not Connected	nc	-	-
B9	LPC_DRQ1#	Not Connected	nc	-	-
B10	LPC_CLK	LPC Clock	O-3.3	-	up to 33MHz
B11	GND_17	Power Ground	PWR	-	-
B12	PWRBTN#	Power Button Input	I-3.3	PU 100k 3.3V	Diode, serial 470
B13	SMB_CLK	SMBus Clock	O-3.3	PU 4k7 3.3V	-
B14	SMB_DAT	SMBus Data	IO-3.3	PU 4k7 3.3V	-
B15	SMB_ALERT#	SMBus Interrupt	IO-3.3	PU 10k 3.3V	Diode serial
B16	SATA1_TX+	SATA 1 Transmit Data+	DP-O	-	-
B17	SATA1_TX-	SATA 1 Transmit Data-	DP-O	-	-
B18	SUS_STAT#	Indicates imminent suspend operation; used to notify LPC devices.	O-3.3	-	CPLD I/O
B19	SATA1_RX+	SATA 1 Receive Data+	DP-I	-	-
B20	SATA1_RX-	SATA 1 Receive Data-	DP-I	-	-
B21	GND_18	Power Ground	PWR	-	-
B22	SATA3_TX+	Not Connected	nc	-	not supported
B23	SATA3_TX-	Not Connected	nc	-	not supported
B24	PWR_OK	Power OK from power supply	I-3.3	PU 100k up after diode	CPLD I/O
B25	SATA3_RX+	Not Connected	nc	-	not supported
B26	SATA3_RX-	Not Connected	nc	-	not supported
B27	WDT	Indicator for Watchdog Timeout	O-3.3	-	CPLD I/O
B28	AC_SDIN2	Not Connected	nc	-	not supported
B29	AC_SDIN1	Audio Codec Serial Data in 1	I-3.3	PD 22k in US15W	-
B30	AC_SDIN0	Audio Codec Serial Data in 0	I-3.3	PD 22k in US15W	-
B31	GND_19	Power Ground	PWR	-	-
B32	SPKR	Speaker Interface	O-3.3	-	-
B33	I2C_CK	General Purpose I2C Clock	IO-3.3	PU 2k2 3.3V	US15W
B34	I2C_DAT	General Purpose I2C Data	IO-3.3	PU 2k2 3.3V	US15W
B35	THRM#	Over Temperature Indicator	I-3.3	PU 10k	TC7SET08FU input
B36	USB2-	USB Data- Port #2 (USB Mode)	DP-I/O	PD 15k in US15W	-
B37	USB2+	USB Data+ Port #2 (USB Mode)	DP-I/O	PD 15k in US15W	-
B38	USB_6_7_OC#	USB Overcurrent Pair 6 / 7	I-3.3	PU 10k 3.3V	-
B39	USB7-	USB Data- Port #7 USB Data- Client (Client Mode)	DP-I/O DP-I/O	PD 15k in US15W PU 1k5 in US15W	- -
B40	USB7+	USB Data+ Port #7 USB Data+ Client (Client Mode)	DP-I/O DP-I/O	PD 15k in US15W PU 1k5 in US15W	- -
B41	GND_20	Power Ground	PWR	-	-
B42	USB5-	USB Data- Port #5	DP-I/O	PD 15k in US15W	-

B43	USB5+	USB Data+ Port #5	DP-I/O	PD 15k in US15W	-
B44	USB_0_1_OC#	USB Overcurrent Pair 0 /1	I-3.3	PU 10k 3.3V	-
B45	USB1-	USB Data- Port #1	DP-I/O	PD 15k in US15W	-
B46	USB1+	USB Data+ Port #1	DP-I/O	PD 15k in US15W	-
B47	EXCD1_PERST#	PCIe Express Card 1 Reset	O-3.3	-	-
B48	EXCD1_CPPE#	PCIe Express Card 1 Request	I-3.3	PU 8k2 3.3V	-
B49	SYS_RESET#	Reset button input	I-3.3	PU 100k 3.3V after diode and 470R Serial	CPLD I/O
B50	CB_RESET#	Carrier Board Reset	O-3.3	-	CPLD I/O
B51	GND_21	Power Ground	PWR	-	-
B52	PCIE_RX5+	Not Connected	-	-	-
B53	PCIE_RX5-	Not Connected	-	-	-
B54	SDIO_CMD GPO1	SDIO#0 Command General Purpose Output 1	I/O-3.3 O-3.3	PU 75k in US15W PD 1k	Bus Switch PI5C3390
B55	PCIE_RX4+	PCIe lane #4 Receive+	DP-I	-	PCIe Bridge
B56	PCIE_RX4-	PCIe lane #4 Receive-	DP-I	-	PCIe Bridge
B57	SDIO_WP GPO2	SDIO#0 WriteProtection General Purpose Output 2	I-3.3 O-3.3	PU 75k in US15W PD 1k	Bus Switch PI5C3390
B58	PCIE_RX3+	PCIe lane #3 Receive+	DP-I	-	PCIe Bridge
B59	PCIE_RX3-	PCIe lane #3 Receive-	DP-I	-	PCIe Bridge
B60	GND_22	Power Ground	PWR	-	-
B61	PCIE_RX2+	PCIe lane #2 Receive+	DP-I	-	PCIe Bridge
B62	PCIE_RX2-	PCIe lane #2 Receive-	DP-I	-	PCIe Bridge
B63	SDIO_CD# GPO3	SDIO#0 CardDetect General Purpose Output 3	I-3.3 O-3.3	PU 75k in US15W PD 1k	Bus Switch PI5C3390
B64	PCIE_RX1+	PCIe lane #1 Receive+	DP-I	PD 50R inUS15W	-
B65	PCIE_RX1-	PCIe lane #1 Receive-	DP-I	PD 50R inUS15W	-
B66	WAKE0#	PCI Express Wake Event	I-3.3	PU 10k 3.3V	CPLD I/O
B67	WAKE1#	General Purpose Wake Event	I-3.3	PU 10k 3.3V	CPLD I/O
B68	PCIE_RX0+	PCIe lane #0 Receive+	DP-I	PD 50R inUS15W	-
B69	PCIE_RX0-	PCIe lane #0 Receive-	DP-I	PD 50R inUS15W	-
B70	GND_23	Power Ground	PWR	-	-
B71	LVDS_B0+	Not Connected	nc	-	not supported
B72	LVDS_B0-	Not Connected	nc	-	not supported
B73	LVDS_B1+	Not Connected	nc	-	not supported
B74	LVDS_B1-	Not Connected	nc	-	not supported
B75	LVDS_B2+	Not Connected	nc	-	not supported
B76	LVDS_B2-	Not Connected	nc	-	not supported
B77	LVDS_B3+	Not Connected	nc	-	not supported
B78	LVDS_B3-	Not Connected	nc	-	not supported
B79	LVDS_BKLT_EN	Backlight Enable	O-3.3	PD 100k	-
B80	GND_24	Power Ground	PWR	-	-
B81	LVDS_B_CK+	Not Connected	nc	-	not supported
B82	LVDS_B_CK-	Not Connected	nc	-	not supported
B83	LVDS_BKLT_CTRL	Backlight Brightness Control	O-3.3	-	-
B84	VCC_5V_SBY	+5V Standby	PWR	-	-
B85	VCC_5V_SBY	+5V Standby	PWR	-	-
B86	VCC_5V_SBY	+5V Standby	PWR	-	-
B87	VCC_5V_SBY	+5V Standby	PWR	-	-

B88	RSVD5	Reserved	-	-	-
B89	VGA_RED	Not Connected	nc	-	not supported
B90	GND_25	Power Ground	PWR	-	-
B91	VGA_GRN	Not Connected	nc	-	not supported
B92	VGA_BLU	Not Connected	nc	-	not supported
B93	VGA_HSYNC	Not Connected	nc	-	not supported
B94	VGA_VSYNC	Not Connected	nc	-	not supported
B95	VGA_I2C_CK	Not Connected	nc	-	not supported
B96	VGA_I2C_DAT	Not Connected	nc	-	not supported
B97	TV_DAC_A	Not Connected	nc	-	not supported
B98	TV_DAC_B	Not Connected	nc	-	not supported
B99	TV_DAC_C	Not Connected	nc	-	not supported
B100	GND_26	Power Ground	PWR	-	-
B101	VCC_12V_13	12V VCC	PWR	-	-
B102	VCC_12V_14	12V VCC	PWR	-	-
B103	VCC_12V_15	12V VCC	PWR	-	-
B104	VCC_12V_16	12V VCC	PWR	-	-
B105	VCC_12V_17	12V VCC	PWR	-	-
B106	VCC_12V_18	12V VCC	PWR	-	-
B107	VCC_12V_19	12V VCC	PWR	-	-
B108	VCC_12V_20	12V VCC	PWR	-	-
B109	VCC_12V_21	12V VCC	PWR	-	-
B110	GND_27	Power Ground	PWR		

Note: The termination resistors in this table are already mounted on the COM Express® board. Refer to the design guide for information about additional termination resistors.

4.2.4 Connector X1B - Row C

Pin	Signal	Description	Type	Termination	Comment
C1	GND	Power Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	I/O-5T	-	-
C3	IDE_D6	IDE Data Bus	I/O-5T	-	-
C4	IDE_D3	IDE Data Bus	I/O-5T	-	-
C5	IDE_D15	IDE Data Bus	I/O-5T	-	-
C6	IDE_D8	IDE Data Bus	I/O-5T	-	-
C7	IDE_D9	IDE Data Bus	I/O-5T	-	-
C8	IDE_D2	IDE Data Bus	I/O-5T	-	-
C9	IDE_D13	IDE Data Bus	I/O-5T	-	-
C10	IDE_D1	IDE Data Bus	I/O-5T	-	-
C11	GND	Power Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	I/O-5T	-	-
C13	IDE_IORDY	IDE I/O Ready	I/O-5T	PU 10k 3,3V (S0)	-
C14	IDE_IOR#	IDE I/O Read	I/O-3,3	-	-
C15	PCI_PME#	PCI Power Management Event	I/O-3,3	PU 10k 3,3V (A)	Serial diode,CPLD
C16	PCI_GNT2#	PCI Bus Grant 2	O-3,3		PCI Bridge
C17	PCI_REQ2#	PCI Bus Request 2	I-5T	PU 8k2 5V (S0)	PCI Bridge
C18	PCI_GNT1#	PCI Bus Grant 1	O-3,3		PCI Bridge
C19	PCI_REQ1#	PCI Bus Request 1	I-5T	PU 8k2 5V (S0)	PCI Bridge
C20	PCI_GNT0#	PCI Bus Grant 0	O-3,3		PCI Bridge
C21	GND	Power Ground	PWR	-	-
C22	PCI_REQ0#	PCI Bus Reqest 0	I-5T	PU 8k2 5V (S0)	PCI Bridge
C23	PCI_RST#	PCI Bus Reset	O-3,3	-	PCI Bridge
C24	PCI_AD0	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C25	PCI_AD2	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C26	PCI_AD4	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C27	PCI_AD6	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C28	PCI_AD8	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C29	PCI_AD10	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C30	PCI_AD12	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C31	GND	Power Ground	PWR	-	-
C32	PCI_AD14	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C33	PCI_C/BE1#	PCI Bus Command and Byte enables 1	I/O-5T	-	PCI Bridge
C34	PCI_PERR#	PCI Bus Grant Error	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
C35	PCI_LOCK#	PCI Bus Lock	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
C36	PCI_DEVSEL#	PCI Bus Device Select	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
C37	PCI_IRDY#	PCI Bus Bus Initiator Ready	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
C38	PCI_C/BE2#	PCI Bus Command and Byte enables 2	I/O-5T	-	PCI Bridge
C39	PCI_AD17	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C40	PCI_AD19	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C41	GND	Power Ground	PWR	-	-
C42	PCI_AD21	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C43	PCI_AD23	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C44	PCI_C/BE3#	PCI Bus Command and Byte enables 3	I/O-5T	-	PCI Bridge
C45	PCI_AD25	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C46	PCI_AD27	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge

C47	PCI_AD29	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C48	PCI_AD31	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-5T	PU 8k2 5V (S0)	PCI Bridge
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-5T	PU 8k2 5V (S0)	PCI Bridge
C51	GND	Power Ground	PWR	-	-
C52	PEG_RX0+	SDVO_TV_CLKIN_P	DP-I	-	-
C53	PEG_RX0-	SDVO_TV_CLKIN_N	DP-I	-	-
C54	TYPE0#	n.c. for type 2 module	nc	-	-
C55	PEG_RX1+	SDVO_INT_P	DP-I	-	-
C56	PEG_RX1-	SDVO_INT_N	DP-I	-	-
C57	TYPE1#	n.c. for type 2 module	nc	-	-
C58	PEG_RX2+	SDVO_FLDSTALL_P	DP-I	-	-
C59	PEG_RX2-	SDVO_FLDSTALL_N	DP-I	-	-
C60	GND	Power Ground	PWR	-	-
C61	PEG_RX3+	n.c.	Nc	-	-
C62	PEG_RX3-	n.c.	Nc	-	-
C63	RSVD	n.c.	nc	-	-
C64	RSVD	n.c.	nc	-	-
C65	PEG_RX4+	n.c.	Nc	-	-
C66	PEG_RX4-	n.c.	Nc	-	-
C67	RSVD	n.c.	nc	-	-
C68	PEG_RX5+	n.c.	Nc	-	-
C69	PEG_RX5-	n.c.	Nc	-	-
C70	GND	Power Ground	PWR	-	-
C71	PEG_RX6+	n.c.	Nc	-	-
C72	PEG_RX6-	n.c.	Nc	-	-
C73	SDVO_DATA	SDVO_CTRLDATA	I/O-3,3	-	-
C74	PEG_RX7+	n.c.	Nc	-	-
C75	PEG_RX7-	n.c.	Nc	-	-
C76	GND	Power Ground	PWR	-	-
C77	RSVD	n.c.	nc	-	-
C78	PEG_RX8+	n.c.	Nc	-	-
C79	PEG_RX8-	n.c.	Nc	-	-
C80	GND	Power Ground	PWR	-	-
C81	PEG_RX9+	n.c.	Nc	-	-
C82	PEG_RX9-	n.c.	Nc	-	-
C83	RSVD	n.c.	nc	-	-
C84	GND	Power Ground	PWR	-	-
C85	PEG_RX10+	n.c.	Nc	-	-
C86	PEG_RX10-	n.c.	Nc	-	-
C87	GND	Power Ground	PWR	-	-
C88	PEG_RX11+	n.c.	Nc	-	-
C89	PEG_RX11-	n.c.	Nc	-	-
C90	GND	Power Ground	PWR	-	-
C91	PEG_RX12+	n.c.	Nc	-	-
C92	PEG_RX12-	n.c.	Nc	-	-
C93	GND	Power Ground	PWR	-	-
C94	PEG_RX13+	n.c.	Nc	-	-
C95	PEG_RX13-	n.c.	Nc	-	-
C96	GND	Power Ground	PWR	-	-

C97	RSVD	n.c.	nc	-	-
C98	PEG_RX14+	n.c.	Nc	-	-
C99	PEG_RX14-	n.c.	Nc	-	-
C100	GND	Power Ground	PWR	-	-
C101	PEG_RX15+	n.c.	Nc	-	-
C102	PEG_RX15-	n.c.	Nc	-	-
C103	GND	Power Ground	PWR	-	-
C104	VCC_12V	12V VCC	PWR	-	-
C105	VCC_12V	12V VCC	PWR	-	-
C106	VCC_12V	12V VCC	PWR	-	-
C107	VCC_12V	12V VCC	PWR	-	-
C108	VCC_12V	12V VCC	PWR 8	-	-
C109	VCC_12V	12V VCC	PWR	-	-
C110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the COM Express® module. Refer to the COM Express® design guide for information about additional termination resistors.

4.2.5 Connector X1B - Row D

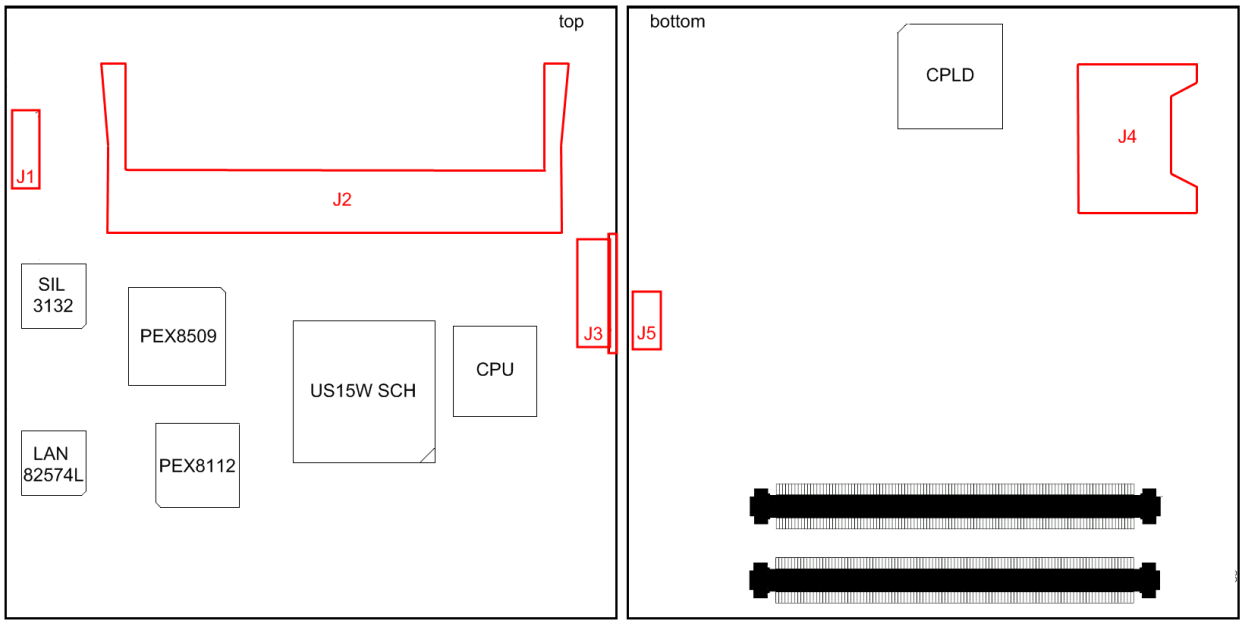
Pin	Signal	Description	Type	Termination	Comment
D1	GND	Power Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	I/O-5T	-	-
D3	IDE_D10	IDE Data Bus	I/O-5T	-	-
D4	IDE_D11	IDE Data Bus	I/O-5T	-	-
D5	IDE_D12	IDE Data Bus	I/O-5T	-	-
D6	IDE_D4	IDE Data Bus	I/O-5T	-	-
D7	IDE_D0	IDE Data Bus	I/O-5T	-	-
D8	IDE_REQ	IDE Data Bus	I/O-5T	-	-
D9	IDE_IOW#	IDE IO Write	O-3,3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O-3,3	-	-
D11	GND	Power Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-5T	PD 10k 3V3	-
D13	IDE_A0	IDE Adress Bus	O-3,3	-	-
D14	IDE_A1	IDE Adress Bus	O-3,3	-	-
D15	IDE_A2	IDE Adress Bus	O-3,3	-	-
D16	IDE_CS1#	IDE Chip Select Channel 0	O-3,3	-	-
D17	IDE_CS3#	IDE Chip Select Channel 1	O-3,3	-	-
D18	IDE_RESET#	IDE Hard Drive Reset	O-3,3	-	CPLD
D19	PCI_GNT3#	PCI Bus Grant 3	O-3,3		PCI Bridge
D20	PCI_REQ3#	PCI Bus Reqest 0	I-5T	PU 8k2 5V (S0)	PCI Bridge
D21	GND	Power Ground	PWR	-	-
D22	PCI_AD1	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D23	PCI_AD3	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D24	PCI_AD5	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D25	PCI_AD7	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	I/O-5T	-	PCI Bridge
D27	PCI_AD9	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D28	PCI_AD11	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D29	PCI_AD13	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D30	PCI_AD15	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D31	GND	Power Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	I/O-5T	-	PCI Bridge
D33	PCI_SERR#	PCI Bus System Error	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
D34	PCI_STOP#	PCI Bus Stop	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
D35	PCI_TRDY#	PCI Bus Target Ready	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
D36	PCI_FRAME#	PCI Bus Cycle Frame	I/O-5T	PU 8k2 5V (S0)	PCI Bridge
D37	PCI_AD16	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D38	PCI_AD18	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D39	PCI_AD20	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D40	PCI_AD22	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D41	GND	Power Ground	PWR	-	-
D42	PCI_AD24	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D43	PCI_AD26	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D44	PCI_AD28	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D45	PCI_AD30	PCI Adress & Data Bus line	I/O-5T	-	PCI Bridge
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-5T	PU 8k2 5V (S0)	PCI Bridge

D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-5T	PU 8k2 5V (S0)	PCI Bridge
D48	PCI_CLKRUN#	PCI Clock Run	O-3,3	PU 8k2 3,3V (S0)	
D49	PCI_M66EN	PCI_M66EN	I-5T	PU 8k2 5V (S0)	PCI Bridge
D50	PCI_CLK	CLK_PCI_33M_EXT | PCI Clock 33MHz	O-3,3	-	PCI Bridge
D51	GND	Power Ground	PWR	-	-
D52	PEG_TX0+	SDVOB_RED_P	DP-O	-	-
D53	PEG_TX0-	SDVOB_RED_N	DP-O	-	-
D54	PEG_LANE_RV#	n.c.	Nc	-	-
D55	PEG_TX1+	SDVOB_GREEN_P	DP-O	-	-
D56	PEG_TX1-	SDVOC_GREEN_N	DP-O	-	-
D57	TYPE2#	n.c. for type 2 module	nc	-	-
D58	PEG_TX2+	SDVOB_BLUE_P	DP-O	-	-
D59	PEG_TX2-	SDVOB_BLUE_N	DP-O	-	-
D60	GND	Power Ground	PWR	-	-
D61	PEG_TX3+	SDVOB_CLK_P	DP-O	-	-
D62	PEG_TX3-	SDVOB_CLK_N	DP-O	-	-
D63	RSVD	-	nc	-	
D64	RSVD	-	nc	-	
D65	PEG_TX4+	n.c.	Nc	-	-
D66	PEG_TX4-	n.c.	Nc	-	-
D67	GND	Power Ground	PWR	-	-
D68	PEG_TX5+	n.c.	Nc	-	-
D69	PEG_TX5-	n.c.	Nc	-	-
D70	GND	Power Ground	PWR	-	-
D71	PEG_TX6+	n.c.	Nc	-	-
D72	PEG_TX6-	n.c.	Nc	-	-
D73	SDVO_CLK	SDVO_CTRLCLK	IO-3,3	-	-
D74	PEG_TX7+	n.c.	Nc	-	-
D75	PEG_TX7-	n.c.	Nc	-	-
D76	GND	Power Ground	PWR	-	-
D77	IDE_CBLID	IDE_CBLID# | IDE cable type detect	I/O-3,3	PU 10k 3V3	-
D78	PEG_TX8+	n.c.	Nc	-	-
D79	PEG_TX8-	n.c.	Nc	-	-
D80	GND	Power Ground	PWR	-	-
D81	PEG_TX9+	n.c.	Nc	-	-
D82	PEG_TX9-	n.c.	Nc	-	-
D83	RSVD	n.c.	nc	-	-
D84	GND	Power Ground	PWR	-	-
D85	PEG_TX10+	n.c.	Nc	-	-
D86	PEG_TX10-	n.c.	Nc	-	-
D87	GND	Power Ground	PWR	-	-
D88	PEG_TX11+	n.c.	Nc	-	-
D89	PEG_TX11-	n.c.	Nc	-	-
D90	GND	Power Ground	PWR	-	-
D91	PEG_TX12+	n.c.	Nc	-	-
D92	PEG_TX12-	n.c.	Nc	-	-
D93	GND	Power Ground	PWR	-	-
D94	PEG_TX13+	n.c.	Nc	-	-
D95	PEG_TX13-	n.c.	Nc	-	-
D96	GND	Power Ground	PWR	-	-

D97	PEG_ENABLE#	n.c.	Nc	-	-
D98	PEG_TX14+	n.c.	Nc	-	-
D99	PEG_TX14-	n.c.	Nc	-	-
D100	GND	Power Ground	PWR	-	-
D101	PEG_TX15+	n.c.	Nc	-	-
D102	PEG_TX15-	n.c.	Nc	-	-
D103	GND	Power Ground	PWR	-	-
D104	VCC_12V	12V VCC	PWR	-	-
D105	VCC_12V	12V VCC	PWR	-	-
D106	VCC_12V	12V VCC	PWR	-	-
D107	VCC_12V	12V VCC	PWR	-	-
D108	VCC_12V	12V VCC	PWR	-	-
D109	VCC_12V	12V VCC	PWR	-	-
D110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the COM Express® module. Refer to the COM Express® design guide for information about additional termination resistors.

4.2.6 Onboard Connectors



Connector J1 - CPLD Debug

The onboard 12pin connector J1 allows accessing the CPLD.

Warning:The debug port is for internal use only. Do not connect any devices.

Connector J2 - SO-DIMM DDR2 Socket

Standard 200pin DDR2 SO-DIMM socket for 400MHz / 533MHz memory modules up to 2GB.

Connector J3 - US15W JTAG Connector

This is the US15W SCH debug connector

Warning:The debug port is for internal use only. Do not connect any devices.

Connector J4 - SDIO/MMC Socket

The onboard SDIO Socket J4 provides the SDIO port #0 from US15W SCH. See SD Card description for more details.

Connector J5 - FAN

3-pin FAN connector for a 5V fan. This can be configured in setup. See fan connector description for more details.

4.3 Signal Description

4.3.1 PCIexpress

The PCI express x1 lane is a fast connection interface for many different system devices, such as network controllers, I/O controllers or express card devices. The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the official PICMG documentation for additional information.

The COMe-cSP2 supports up to 5 PCIexpress x1 Lanes. See the table below for detailed configuration:

Source 1	Optional	Standard	Target
Intel US15W PCIe #2	-	-	COMe PCIe Lane #1
-	PEX8505 Port #0	PEX8509 Port #0	COMe PCIe Lane #0
Intel US15W PCIe #1	PEX8505 Uplink Port #1	PEX8509 Uplink Port #1	-
-	PEX8505 Port #2	PEX8509 Port #2	Intel 82574L GBLan
-	PEX8505 Port #3	PEX8509 Port #3	PEX8112 PCIe2PCI Bridge
-	PEX8505 Port #4	PEX8509 Port #4	SIL3132 PCIe2SATA Bridge
-	-	PEX8509 Port #5	COMe PCIe Lane #2
-	-	PEX8509 Port #6	COMe PCIe Lane #3
-	-	PEX8509 Port #7	COMe PCIe Lane #4

Note1: The PCIexpress lanes can only be used in x1 configuration. No x4 lane is possible.

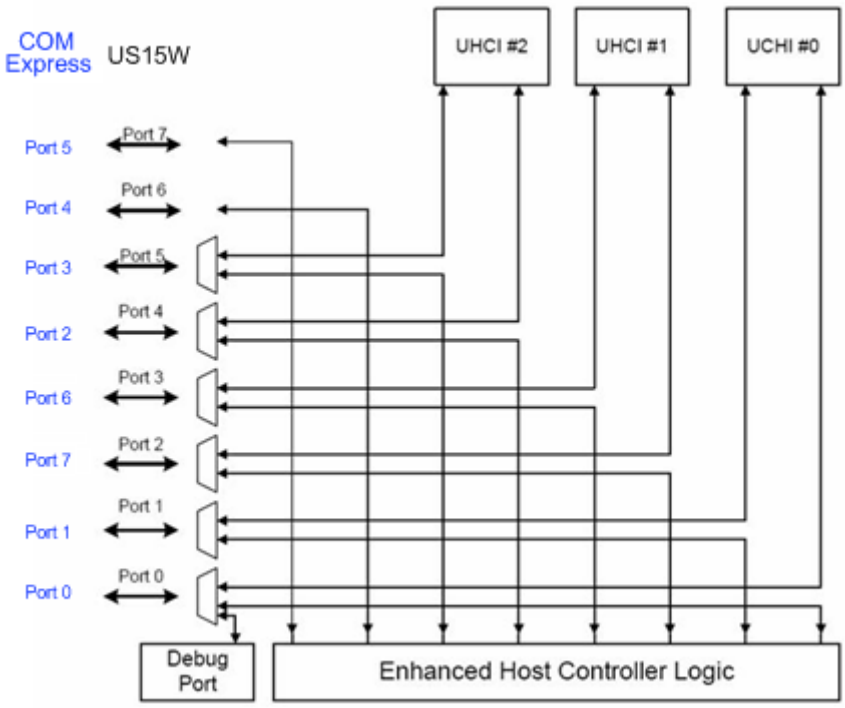
Note2: PCIexpress HotPlug functionality is not supported by the US15W SCH.

4.3.2 USB

The USB interface comes with three USB controllers (6 USB ports). The USB configuration of the COMe-cSP2 module is described in the following table:

COM Express Port	US15W SCH Port	Description
USB0	USB0	USB 2.0 compliant ports
USB1	USB1	
USB2	USB4	
USB3	USB5	
USB4	USB6	Not USB 2.0 compliant, no UHCI controller (no USB 1.1 / USB 2.0 only)
USB5	USB7	
USB6	USB3	USB 2.0 compliant port
USB7	USB2	USB Client or USB 2.0 compliant port (configurable in BIOS Setup)

The following diagram shows the internal USB mapping from US15W SCH:



The amount of available USB connections can be expanded by adding external USB-hubs.

USB Client Port

The USB interface also supports one USB client port (USB port 7) that can be activated in setup. If the client function is disabled in the BIOS this port acts as a standard USB port. Please be aware that USB power lines may not be connected on the USB client port.

Note:	A Special USB client and host driver software is needed for USB client function. When this driver and software is installed the client port appears as a mass storage device and NDIS Network device or as NDIS Network device only in the device manager of the operating system. Please refer to the Kontron download page for COMe-cSP2 for the driver

Configuration

The USB controllers are PCI bus devices. The BIOS allocates required system resources during configuration of the PCI bus.

4.3.3 SATA

The Intel® US15W System Controller Hub does not support a SATA interface. Therefore an external controller from Silicon Image (SIL3132) for PCIexpress is used on COMe-cSP2. The controller provides 2 SATA Ports (COMe SATA#0 and SATA#1) up to 3Gb/s connection with support for RAID Level 0 and 1, Native Command Queing, Port Multiplier and Staggered Spinup. The pins for the SATA connection are listed in the pinout table for the module connector.

Note:	Using a SATA harddisk for operating systems requires a driver during installation. Please visit the Kontron download page for COMe-cSP2. Windows XP driver installation via USB floppy when installing from SATA to SATA does not work with this module. The driver must then be integrated into the installation CD before installation.

Configuration

The SATA controller is a PCIexpress bus device. The BIOS allocates required system resources during configuration of the PCIexpress device.

4.3.4 Audio

The US15W Intel® System Controller Hub supports Intel® High Definition Audio (HDA). The Intel® High Definition Audio supports up to four audio streams (up to 16 channels each), 32-bit sample depth, and sample rates to 192 KHz.

This allows implementation of a hardware codec on your baseboard for 7.1/5.1 audio systems and SDIF ouput. The pins for the Intel® High Definition Audio are described in the module connector description.

Warning: Only baseboards with HD Audio codec are supported. AC97 codecs are not compatible to US15W SCH.

Configuration

The audio controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI device.

4.3.5 Serial IRQ

The serial IRQ pin offers a standardized interface to link interrupt request lines to a single wire.

Configuration

The serial IRQ machine is in “Continuous Mode”.

4.3.6 Graphics Interface

The COMe-cSP2 uses the graphics accelerator GMA500 with 200MHz GPU clock integrated in the Intel® US15W System Controller Hub, which delivers shader-based technologies and high-performance 2D, 3D and video capabilities. The GMA500 graphics engine supports a variety of LCD panels with single clock, color depths of 18/24 bit and resolutions up to WXGA (1366x768). The maximum supported pixelclock of the US15W SCH is 112 MHz.

Hardware video decode acceleration relieves the decode burden from the processor and reduces the power consumption of the system. Full hardware acceleration of H.264, MPEG2, VC1 and WMV9 eliminates the need of a software codec and offloads the CPU.

The graphic adapter uses the onboard RAM as graphic memory. The preallocated memory is defined through BIOS settings.

Possible settings include:

- 1MB
- 4MB
- 8MB

The total amount of graphics memory in the operating system depends on the size of system memory and the used driver settings. The graphics media accelerator driver GMA uses DVMT to manage allocating of system memory according to the needs of running applications. The Intel® Embedded Graphics Driver IEGD allocates the maximum of graphics memory depending on system memory and driver settings.

Physical Memory of COMe-cSP2	Preallocated Memory in BIOS Setup	Maximum Graphics Memory with GMA Driver	Maximum Graphics Memory with IEGD
512MB	1MB	127MB	352MB
512MB	4MB	126MB	352MB
512MB	8MB	125MB	352MB
1024MB	1MB	255MB	352MB
1024MB	4MB	254MB	352MB
1024MB	8MB	253MB	352MB

Note : When using 1MB pre-allocated memory, a Operating Systems without active GMA or IEGD may have problems displaying a screen (e.g. during WinXP installation).

VGA

The COMe-cSP2 graphics subsystem integrated in the Intel® US15W System Controller Hub does not natively support VGA output.

Note: Systems that require VGA support need to include a component on the carrier board. It is recommended to implement a SDVO-to-VGA conversion (e.g. from Chrontel)

LVDS Flat Panel Interface (JILI)

The user interface for flat panels is the JUMPtec Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the documentation for additional information.

SDVO

The COMe-cSP2 Serial Digital Video Output port is integrated in the Intel® US15W System Controller Hub. It has the following features:

- Shares pins with the PEG interface
- Serial Digital Video Out Port (one port)
- The SDVO port can drive a variety of SDVO devices (TV-Out Encoders, TMDS and LVDS transmitters, etc.)

The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the official PICMG documentation for additional information.

4.3.7 Ethernet

The Ethernet interface of the COMe-cSP2 uses the latest Intel® 82574L Gigabit Ethernet controller that is connected to the PCIexpress Switch Port #1. The network controller supports a 10/100/1000 Base-T interface. The device auto-negotiates the use of 10 Mbit/sec, 100 Mbit/sec or 1Gbit/sec connections.

The ethernet interface operates at lowest power (<1W) when Gbit-Ethernet is fully active and supports functions as WOL (Wake On LAN) and PXE (Preboot eXecution Environment) boot.

For cable lenghts and ternminations on your baseboard please refer to the COM Express® Design Guide.

Configuration

The Ethernet controller is a PCIexpress bus device. The BIOS allocates required system resources during configuration of the PCIexpress device.

4.3.8 LPC Bus

The Low Pin Count (LPC) Interface signals are connected to the LPC Bus bridge, which is located in the Intel® US15W system controller hub. The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller, which typically combines legacy-device support into a single IC. The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide maintained by PICMG. Please refer to the official PICMG documentation for additional information.

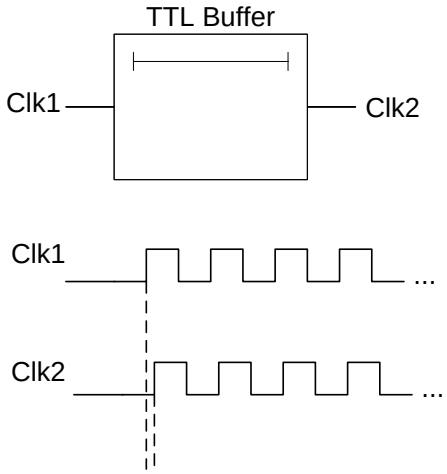
The LPC bus does not support DMA (Direct Memory Access). This leads to limitations for ISA bus and SIO (standard I/O´s like Floppy or LPT interfaces) implementations. When more than one device is connected to the LPC bus a clock buffer is required!

Warning: Due to the power management feature of the LPC Bus, clock buffers that require synchronization should be used with great care and may prevent the board from booting up.

Active LPC Clock frequency

- with Z530 CPU: 33MHz
- with Z510 CPU: 25MHz

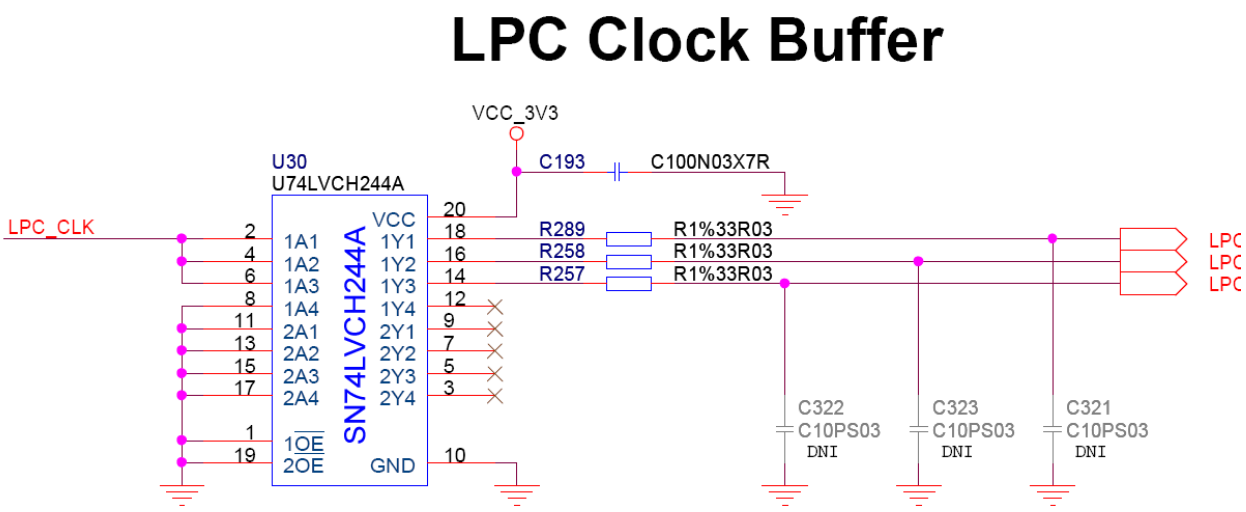
Standard Clock Buffer



When using a standard clock buffer on the baseboard please be aware that the generated delay has to be considered for the length matching of the layout.

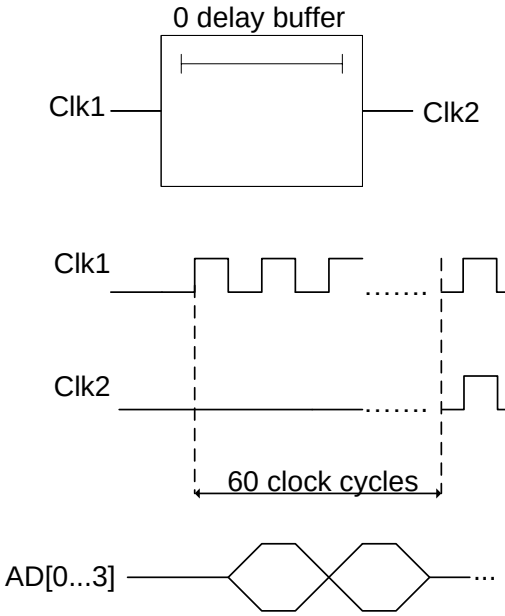
Clock Buffer Reference Schematic

The implementation of a clock buffer can be achieved as shown in the evaluation schematic below:



Zero Delay Clock Buffer

The use of a zero delay clock buffer leads to problems because it needs approximatley 60 clock cycles before the clock is present on the output. The Intel® USB15W System Controller Hub typically detects if a device is connected to the LPC clock, but it will not wait the 60 clock cycles to stay active.



Warning: Do not use the reference schematic in the COM Express® Design Guide. Either use another Clock Buffer solution without a long start up process or use series resistors to double the LPC clock line. Follow the design recommendations in the COM Express Design Guide maintained by PICMG.

Overview of LPC Adresses

Address (HEX)	Device
0000 - 00FF	IBM PC compatible devices (IRQ-Controller, Keyboard, RTC etc.)
002E-002F	Optional: Super I/O W83627
004e - 004f	TPM
01F0 - 01F7	Fixed Disk
03C0 - 03CF	VGA/EGA compatible registers
03F6	Fixed Disk
0400 - 043F	SMBus
0480 - 04BF	GPIO SCH
04D0 - 04D1	IRQ Configuration
08F0 - 08FF	Optional
0900 - 091F	Power Management
0A80 - 0A83	reserved
0CF8 - 0CFF	PCI Configuration
D880 - D887	PCI LAN Controller *
E080 - E09F	PCI USB Controller *
E480 - E49F	PCI USB Controller *
E880 - E887	PCI VGA Controller *
EF00 - EF1F	PCI USB Controller*
FFA0 – FFAF	PCI IDE Controller *

Note *: Not fixed. Configured by BIOS automatically. May be different in other system configurations.

Address (HEX)	Device
00000000 - 0009FFFF	DOS- (Real mode-) memory
000A0000 - 000BFFFF	Display memory
000C0000 - 000CBFFF	VGA BIOS
000CC000 - 000DFFFF	Other Option ROM
000E0000 - 000EFFFF	System BIOS extended space
000F0000 - 000FFFFF	System BIOS base segment
00100000 - 7FFFFFFF	System Memory
80000000 - FFF00000	PCI memory, other extensions
CFDDC000 - CFFFFFFF	PCI LAN Controller
D0000000 - DFFFFFFF	PCI VGA Controller / Audio Controller / USB Controller
FEC00000 - FEC00040	APIC Configuration
FED00000 - FED003FF	Event Timer
FED10000 - dynamic	Audio Controller
FED40000 - FED4BFFF	LPC Configuration
F0000000 - F0003FFF	RCRB (Root Complex)
FFC00000 - FFF00000	Reserved
FFF00000 - FFFFFFFF	Firmware Hub
FFF80000 - FFFFFFFF	Mapping space for BIOS ROM

For further details, please refer to Intels “System Controller Hub External Design Specification (EDS)”, chapter “I/O Address Space”.

4.3.9 Power Control

Power Good (PWR_OK)

The COMe-cSP2 provides an external input for a power-good signal (Pin B24). The implementation of this subsystem complies with the COM Express® Specification. PWR_OK is internally pulled up to 3.3V and must be high level to power on the module.

Power Button (PWRBTN#)

The power button (Pin B12) is available through the module connector described in the pinout list. To start the module via Power Button the PWRBTN# signal must be at least 50ms (50ms ≤ t < 4s) at low level (Power Button Event).

Pressing the power button for at least 4seconds will turn off power to the module (Power Button Override).

Reset Button (SYS_RESET#)

The reset button (Pin B49) is available through the module connector described in the pinout list. The module will stay in reset as long as SYS_RESET# is grounded.

Power Supply

The COMe-cSP2 has a wide range power input from 8.5 to 18V DC. The supply voltage is applied through 42pins (VCC) of the module connector. In ATX mode with 5V standby voltage the VCC input must be higher than the standby voltage.

In general, single supply mode means the module starts as soon as power is applied to the module, ATX mode is for power button controlled operation. A powerloss function cannot be implemented in the BIOS setup, because there is no Southbridge available on the module. That is where this function is usually managed.

ATX Mode / Single Supply Mode

ATX Mode:

By connecting an ATX power supply, PWR_OK is set to low level and VCC is off. Press the power button to enable the ATX PSU setting PWR_OK to high level and powering on VCC. The ATX PSU is controlled by the PS_ON# signal which is generated by SUS_S3# via inversion.

	ATX Mode				
State	**PWRBTN#**	**PWR_OK**	**V5_StdBy**	**PS_ON#**	**VCC**
G3	x	x	0V	x	0V
S5	high	low	5V	high	0V
S5 -> S0	PWRBTN Event	low -> high	5V	high -> low	0 V-> VCC
S0	high	high	5V	low	VCC

Single Supply Mode:

In single supply mode the module will start automatically when VCC power is connected and Power Good input is open or at high level (internal PU to 3.3V). PS_ON# is not used in singly supply mode.

To power on the module from S5 state press the power button or reconnect VCC

Single supply mode				
State	**PWRBTN#**	**PWR_OK**	**V5_StdBy**	**VCC**
G3	x	x	x	0
G3 -> S0	high	open / high	x	connecting VCC
S5	high	open / high	x	VCC
S5 -> S0	PWRBTN Event	open / high	x	reconnecting VCC

- All columbs marked with an “x” are not important for the specific power state.

- All ground pins have to be tied to the ground plane of the carrier board.

4.3.10 Miscellaneous Circuits

Speaker

The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the official PICMG documentation for additional information.

Battery

The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the official documentation maintained by PICMG for additional information.

In compliance with EN60950, there are at least two current-limiting devices (resistor and diode) between the battery and the consuming component.

I2C Bus

For additional information, refer to the COM Express® Design Guide, I2C application notes and JIDA specifications which are available at the Kontron Web site. See BIOS chapter for supported features and speed of I2C.

SM Bus

System Management (SM) bus signals are connected to the SM bus controller, which is located in the Intel® US15W system controller hub. The SMBus is a two wire bidirectional bus (clock and serial data) used for system management such as reading parameters from a memory card, and reading temperatures and voltages of system components.

The SM Bus uses the same signaling scheme as an I2C bus.

PCI Bus

The Intel® US15W SCH does not support PCI. Therefore a PLX Technology PCIexpress to PCI bridge PEX8112 is used. The bridge is connected to Port #3 of the PCIe switch and provides a standard PCI 3.0 32bit/33MHz interface. The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the official PICMG documentation for additional information.

IDE Port

The IDE host adapter in the Intel® US15W SCH is capable of UDMA-33/66/100 operation. The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the documentation maintained by PICMG for additional information.

5 Special Features

5.1 S5 Eco

Kontron's new high-efficient power-off state S5 Eco enables lowest power-consumption in soft-off state – less than 1 mA compared to the regular S5 state this means a reduction by at least factor 200!

In the "normal" S5 mode the board is supplied by 5V_Stb and needs usually up to 300mA just to stay off. This mode allows to be switched on by power button, RTC event and WakeOnLan, even when it is not necessary. The new S5 Eco mode reduces the current tremendously.

The S5 Eco Mode can be enabled in BIOS Setup

Following prerequesites and consequences occur when S5 Eco Mode is enabled

- The power button must be pressed at least for 200ms to switch on.
- Wake via Powerbutton only.
- "Power On After Power Fail": only "stay off" is possible
- In 12V only mode the S5 Eco Mode must be switched off to enable the board to start immediatelly

5.2 Hyper Threading

Hyper Threading (officially termed Hyper Threading Technology or HTT) is an Intel®-proprietary technology used to improve parallelization of computations performed on PC´s. Hyper-Threading works by duplicating certain sections of the processor—those that store the architectural state but not duplicating the main execution resources. This allows a Hyper-Threading equipped processor to pretend to be two "logical" processors to the host operating system, allowing the operating system to schedule two threads or processes simultaneously. HTT support always relies on the Operating System.

Note:	HTT is only supported on the Z530 (1.6 GHz) version of the COMe-cSP2. Operating system images from the 1.1GHz (Z510) and 1.6GHz (Z530) module may not be fully compatible. It's recommended to use separate images on hyperthreading and non-hyperthreading variant.

5.3 Speedstep Technology

The Intel® Atom Processor offers the Intel® Enhanced SpeedStep™ technology that automatically switches between maximum performance mode and battery-optimized mode, depending on the needs of the application being run. It let you customize high performance computing on your applications. When powered by a battery or running in idle mode, the processor drops to lower frequencies (by changing the CPU ratios) and voltage, conserving battery life while maintaining a high level of performance. The frequency is set back automatically to the high frequency, allowing you to customize performance.

In order to use the Intel® Enhanced SpeedStep™ technology the operating system must support SpeedStep™ technology.

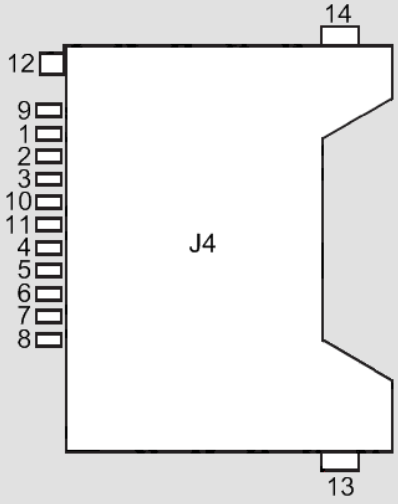
By disabling the SpeedStep feature in the BIOS, manual control/modification of CPU performance is possible. Setup the CPU Performance State in the BIOS Setup or use 3rd party software to control CPU Performance States.

5.4 SD-card Interface (SDIO)

The SD card standard is a standard for removable memory storages designed and licensed by the SD Card Association (http://sdcard.org). The card form factor, electrical interface, and protocol are all part of the SD Card specification. The Intel® US15W System Controller Hub supports up to 3 SDIO interfaces. On COMe-cSP2 the first interface SDIO#0 is used for the onboard miniSD Card socket. The second Port SDIO#1 provides the SD card interface shared with the module GPIO signals to the baseboard. SDIO#3 is not used and deactivated. The integrated SDIO 1.1 / MMC 4.1 controller in US15W SCH only supports byte-address mode for SDIO storage cards up to 2GB. Sector-addressing and SDHC is not supported.

- » MMC 4.1 transfer rates can be up to 48MHz and bus widths of 1, 4 or 8 bits
- » SDIO 1.1 supports transfer rates up to 24MHz and bus widths of 1 or 4 bits

Onboard miniSD/MMC Socket J4



PIN	Description
1	DAT3/CD - Data Line 3/Card Detection
2	CMD - Command/Response
3	VSS 1 - Supply Voltage - GND
4	VDD - Supply Voltage - 3.3V
5	CLK - Clock
6	VSS2 - Supply Voltage - GND
7	DAT0 - Data Line 0
8	DAT1 - Data Line 1
9	DAT2 - Data Line 2
10	n.c.
11	n.c.
12	Detect
13	Ground 0
14	Ground 1
15	Ground 2

SDIO/GPIO on COM Express® Connector

General purpose Input/Output	SD card interface signals
GPI0	SLOT0_DATA0
GPI1	SLOT0_DATA1
GPI2	SLOT0_DATA2
GPI3	SLOT0_DATA3
GPO0	SLOT0_CLK
GPO1	SLOT0_CMD
GPO2	SLOT0_WP
GPO3	SLOT0_CD#

SD card compatibility

Due to the mechanical variability with different SD card manufacturers, Kontron recommends that miniSD cards from the following vendor for use with the COMe-cSP2:

- Transcend
- Apacer
- Elecom
- Hidata

The use of miniSD cards from other manufacturers may cause difficulty when ejecting the cards from the on-module mini SD card socket.

This note applies to modules of the following part numbers:

- 36003-0000-11-4
- 36003-0000-16-4.

SD recommendations

- The SD_CMD line needs a pull-up resistor that can vary depending on the length of the electrical paths (typical from 10kOhm to 100kOhm).
- The maximum length for SDIO signals on the baseboard should be 80mm
- SDIO boot is supported on baseboards following the maximum length specification for SDIO (80mm).

5.5 Watchdog

This feature is implemented in the CPLD and offers a single staged watchdog. You can configure the Watchdog Timer (WDT) by JIDA32 Library API (Refer to Appendix: JIDA Standard) or BIOS Setup and directly via register settings. The application software should strobe the WDT to prevent its timeout. Upon timeout, the WDT resets and restarts the system. This provides a way to recover from program crashes or lockups.

The Watchdog can be enabled via:

- BIOS Setup (with BIOS NOW1R113 or newer)
- JIDA32 or K-Station
- Direct programming over register settings

The Watchdog can be triggered via

- JIDA32 or K-Station
- Direct programming (just write data into one register of the CPLD)

For Programming the feature please refer to the JIDA32 driver paket in the download section and for direct programming please contact your local sales or support for an application note.

5.6 GPIO - General Purpose Input and Output

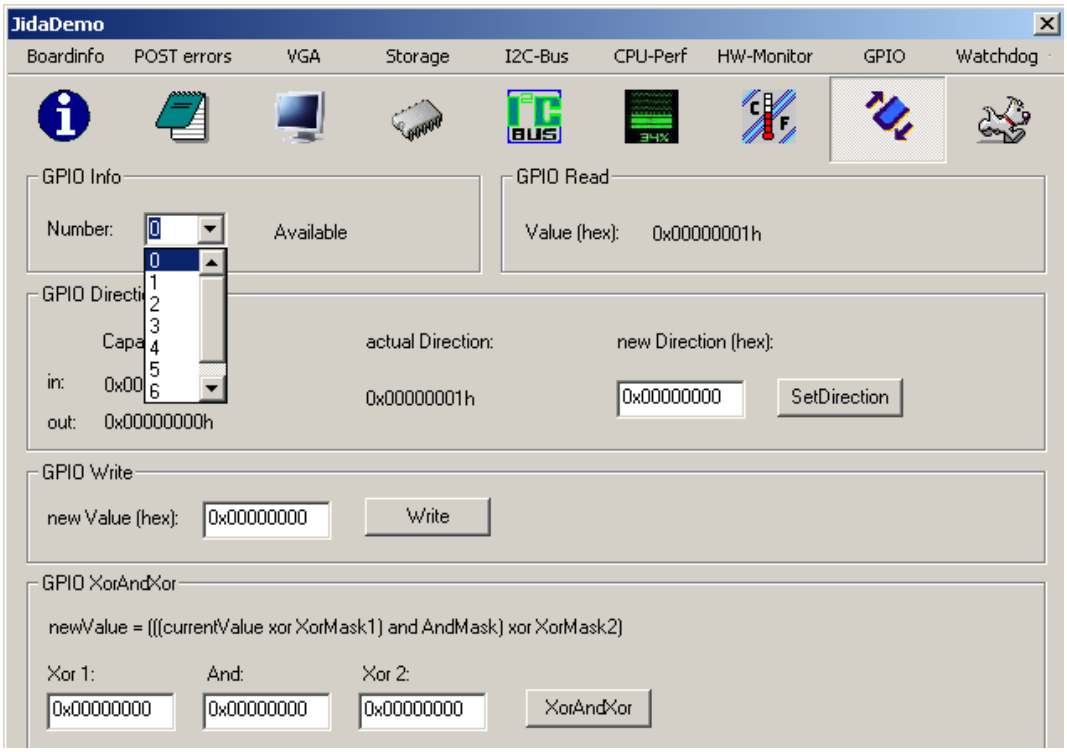
The COMe-cSP2 provides 8 GPIOs that can be accessed through the module connector described in the pinout list. The GPIO interface is shared with SDIO signals and can be enabled in BIOS setup.

Note:	The General Purpose Inputs and Outputs are not applicable to drive applications faster than 2ms. It's recommended to use data transfer rates only up to 1kHz.

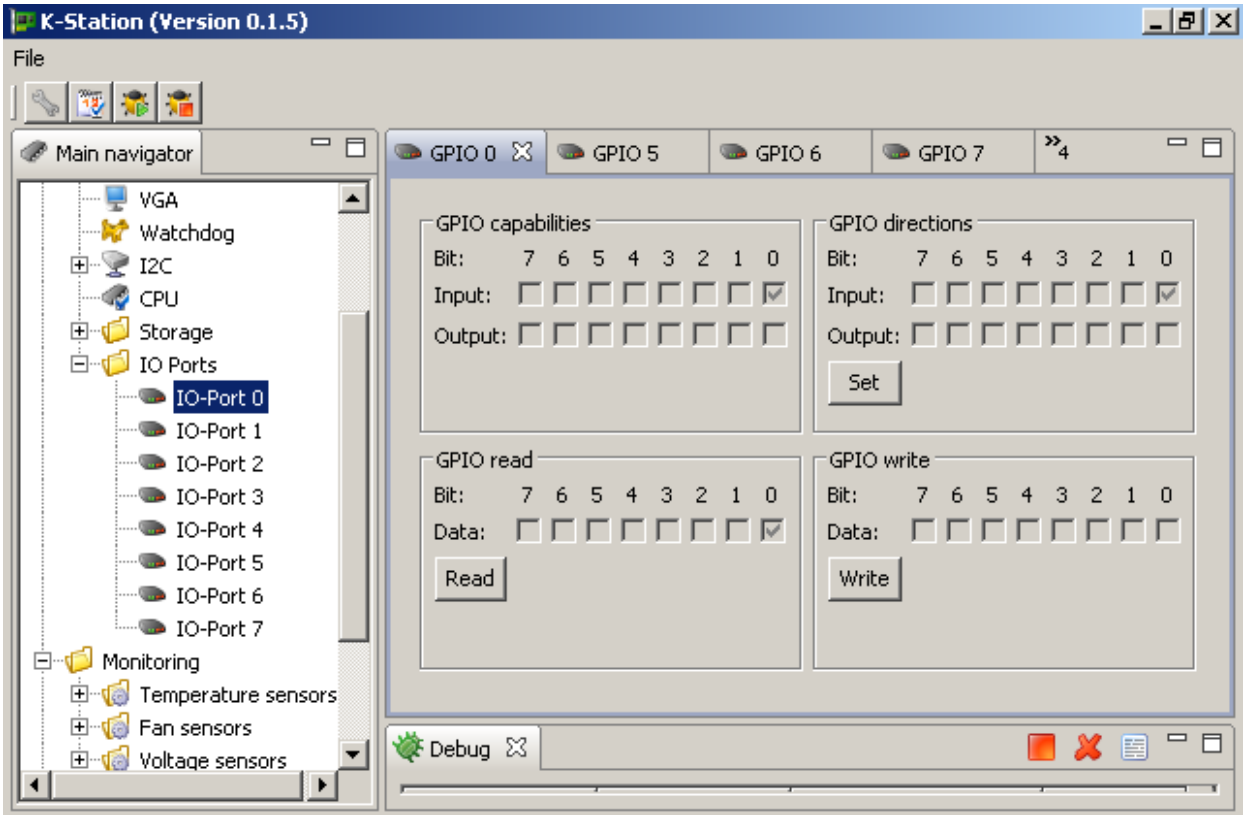
There is one IO Port controlled via onboard CPLD (1 Byte, Port 0) available and the 4 Inputs and 4 Outputs are fixed in direction. To access the GPIOs use the JIDA32 interface. You can write to a General Purpose Output with the upper half byte. To read a General purpose Input use the lower half byte.

Bit of GPIO Port0	Function	COM Express Pin
0	GPI0	A54
1	GPI1	A63
2	GPI2	A67
3	GPI3	A85
4	GPO0	A93
5	GPO1	B54
6	GPO2	B57
7	GPO3	B63

JIDA32 for Windows:

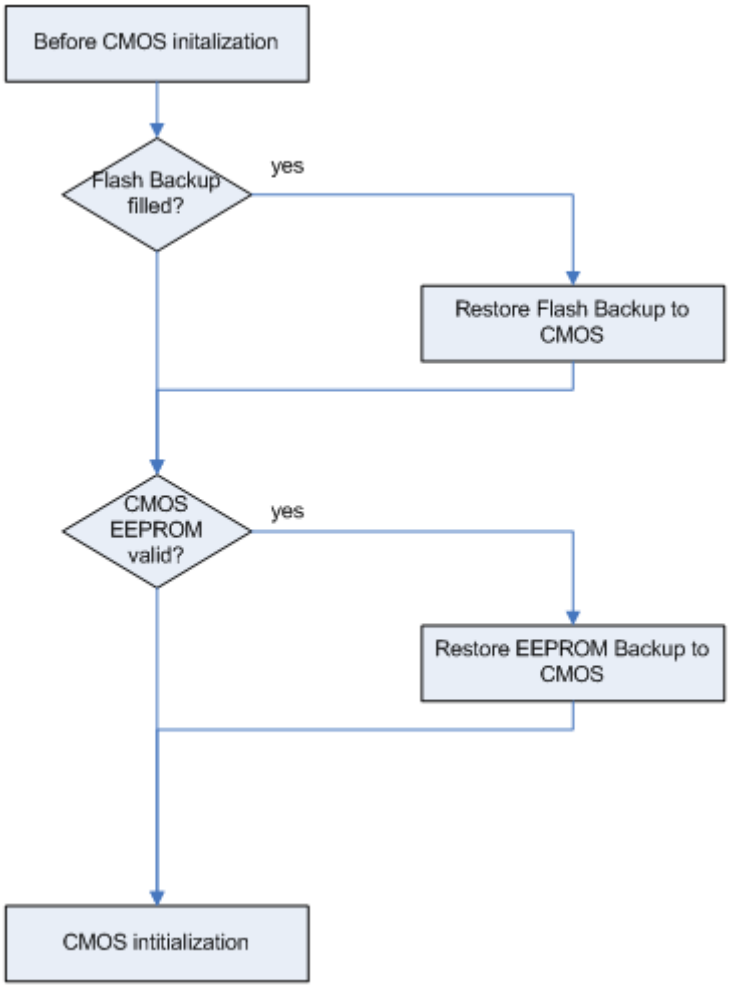


K-Station for Windows:



5.7 Flash Backup Feature

The COMe-cSP2 supports a new functionality called “Flash Backup”. This new feature allows saving custom defaults directly into the Flash. With invalid EEPROM data or without a CMOS EEPROM, the module will start up with these custom defaults. It’s possible to save this BIOS with changed defaults to an image and flash it on other modules.



To create a BIOS with custom defaults:

» Change your BIOS settings

» Save as custom defaults to RTC/Flash and Exit (module will now always start with these settings)

» Extract the BIOS including custom defaults with afudos or kflash utility for windows

AFUDOS: c:\>afudos.exe biosname.rom /O

KFLASH: c:\>kflash.exe backup biosname.rom

Flash your BIOS with custom defaults:

To flash a BIOS with customized defaults extracted like described above, use following options

» Update the BIOS with kflash utility in windows

c:\>kflash.exe flash biosname.rom /bncr

» Update the BIOS with standard afudos utility in DOS and invalidate the EEPROM

c:\>afudos.exe biosname.rom /p /b /n /c

c:\>jidacmos.exe eep /clean

Note1: kflash.exe is a shell tool included in Kontron K-Station System Utility Package.

Note2: Contact your local sales or support for jidacmos utility. It is also included in the BIOS download package on Kontron's customer section.

5.8 Fast I2C

The COMe-cSP2 integrates two configurable I2C buses. The external I2C provided via US15W GPIOs on COM Express® Connector Pin B33/B34 and the JILI (LVDS) I2C from US15W SCH is available on COM Express® connector pin A83/A84. See the BIOS resource list for reserved addresses. The I2C interface offers full MultiMaster and Clock Stretching support. Fast I2C clock speed depends on the CPU performance and differs between ATOM™ Z510 and ATOM™ Z530 modules. See the tables below for measured values on COMe-cSP2.

JIDA/external I2C speed

Setup	ATOM™ Z510	ATOM™ Z530
Extra high	not supported	not supported
Very high	150 kHz	210 kHz
High	80 kHz	110 kHz
Medium	40 kHz	60 kHz
Slow	11 kHz	16 kHz
Very slow	1.5 kHz	2 kHz
Ultra slow	0.8 kHz	1 kHz

JILI I2C speed

Setup	ATOM™ Z510	ATOM™ Z530
Extra high	not supported	not supported
Very high	90 kHz	125 kHz
High	36 kHz	50 kHz
Medium	18 kHz	25 kHz
Slow	2.8 kHz	4 kHz
Very slow	1.0 kHz	1.3 kHz
Ultra slow	not supported	not supported

5.9 ACPI Suspend Modes and Resume Events

The COMe-cSP2 only supports the S3 state (=Save to Ram). S4 (=Save to Disk) is not supported by the BIOS (S4_BIOS) but S4_OS is supported by the following operating systems:

- Windows XP
- Windows Vista
- Windows 7

The following events resume the system from S3:

- USB Keyboard (1)
- USB Mouse (1)
- Power Button
- WakeOnLan (2)

The following events resume the system from S4/S5:

- Power Button
- WakeOnLan

Note: (1) OS must support wake up via USB devices and baseboard must power the USB Port with StBy-Voltage
(2) WakeOnLan must be enabled in the driver options.

6 Design Consideration

6.1 Thermal Management

A heat-spreader plate assembly is available from Kontron Embedded Modules for the COMe-cSP2. The heatspreader plate on top of this assembly is NOT a heat sink. It works as a COM Express™-standard thermal interface to use with a heat sink or other cooling device.

External cooling must be provided to maintain the heat-spreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heat-spreader plate temperature of 60° C or less.

The aluminum slugs and thermal pads on the underside of the heat-spreader assembly implement thermal interfaces between the heat spreader plate and the major heat-generating components on the COMe-cSP2. About 80 percent of the power dissipated within the module is conducted to the heat-spreader plate and can be removed by the cooling solution.

You can use many thermal-management solutions with the heat-spreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the COM Express® application and environmental conditions. Please see the COM Express® Design Guide for further information on thermal management.

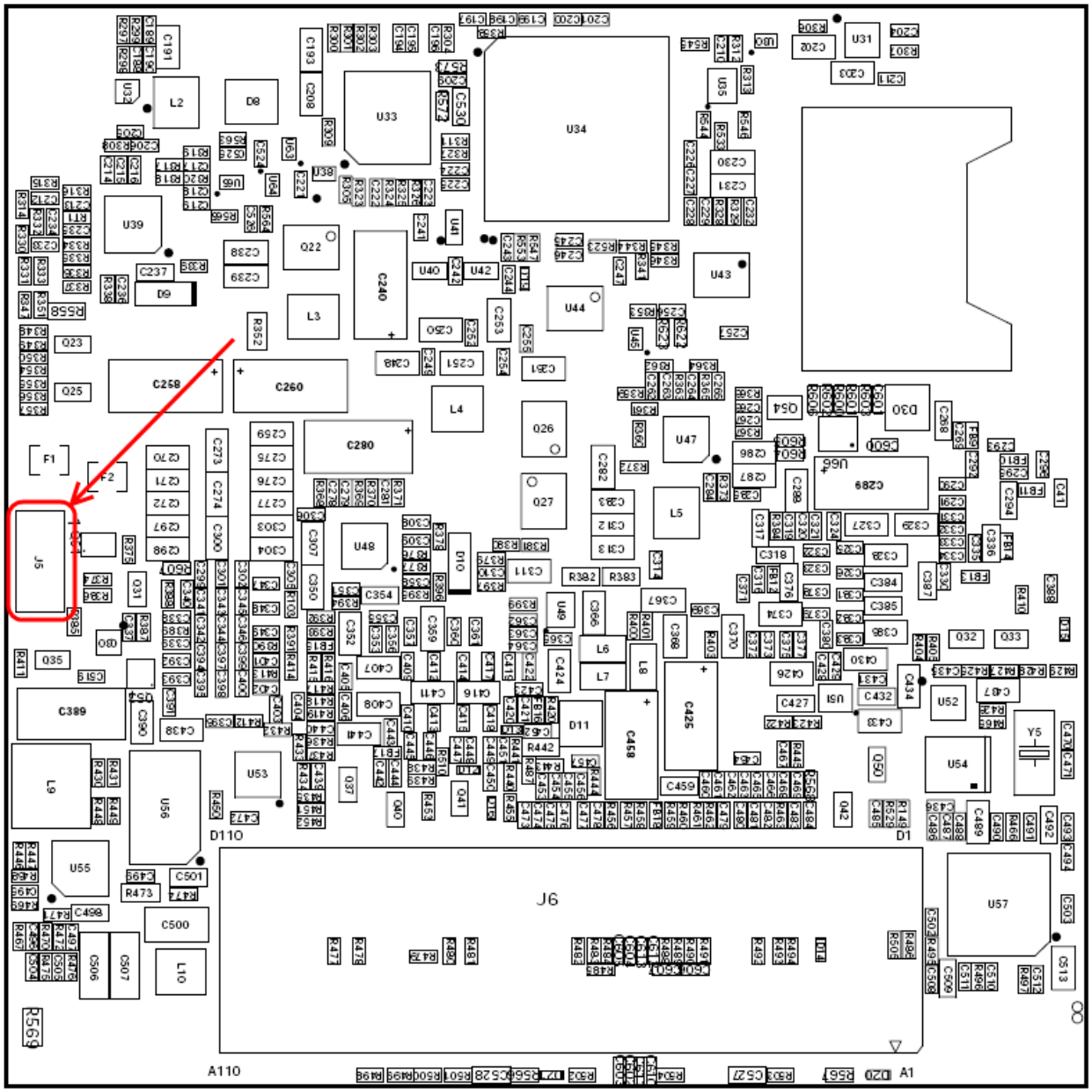
6.2 Heatspreader Dimensions

Documentation of COMe-cSP2 heatspreader is available in Kontron's customer section.

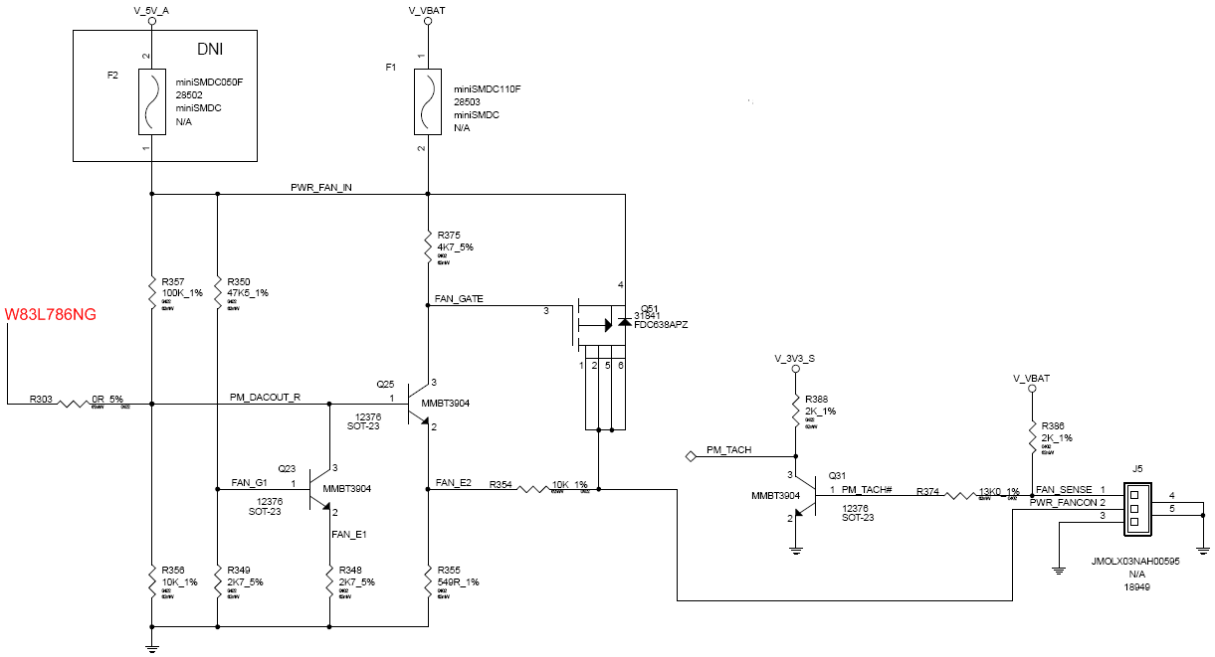
6.3 COMe-cSP2 onboard fan connector

This section describes how to connect an optinal fan to the connector located directly on the COMe-cSP2. With certain BIOS settings, it is possible to control fan operation depending on the Active Trip Point temperature. The fan switches on/off depending on the adjusted Active Trip Point temperature. In order for this feature to function properly an ACPI compliant OS is necessary.

6.3.1 Location and Pin-out of fan connector



The onboard fan connector (J5) can be found on the left side, on the bottom surface of COMe-cSP2 PCB and it is connected onboard according to the following schematic:

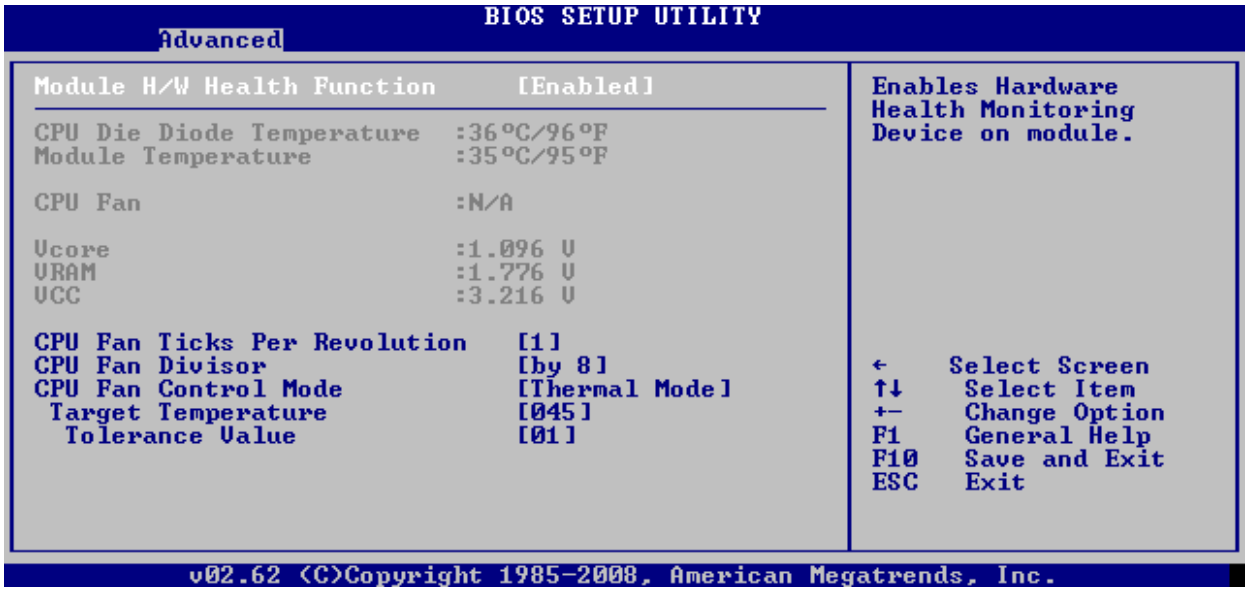


Connector J5 has following specification:

- Part number (Molex) J8: 53261-0390
- Mates with: 51021-0300
- Crimp terminals: 50079-8100

6.3.2 BIOS Settings for fan control

Please refer to the Module Hardware Monitor Setup for fan control.



6.3.3 Electrical Characteristics

» VCC in FANCON: VCC of board, limited to 12V max

» Imax: 0.40 A

Note:	The VCC_in_FANCON output is not short-circuit proof. If necessary, the user has to ensure that the circuit is protected externally (i.e. protection via a fuse installed on the application-specific carrier board)

7 System Ressources

7.1 Interrupt Request (IRQ) Lines

7.1.1 In 8259 PIC mode

IRQ #	Used For	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Cascade	No	
3	External SIO - COM2	Yes (No)	Note (1)
4	External SIO - COM1	Yes (No)	Note (1)
5	PCI	for PCI	Dynamic (BIOS default)
6	External SIO	Yes (No)	Note (1)
7	External SIO - LPT1	Yes (No)	Note (1)
8	RTC	No	
9	ACPI	No	Note (2)
10	PCI	for PCI	Dynamic (BIOS default)
11	PCI	for PCI	Dynamic (BIOS default)
12	PS/2 Mouse	Yes (No)	Note (1)
13	FPU	No	
14	Primary IDE	No	Note (1)
15	PCI	for PCI	Dynamic (BIOS default)

Note: (1) If the “Used For” device is disabled in setup, the corresponding interrupt is available for other devices.
(2) Not available if ACPI is used

7.1.2 In APIC mode

IRQ #	Used For	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Cascade	No	
3	External SIO - COM2	Yes (No)	Note (1)
4	External SIO - COM1	Yes (No)	Note (1)
5	PCI	for PCI	Dynamic (BIOS default)
6	External SIO	Yes (No)	Note (1)
7	External SIO - LPT1	Yes (No)	Note (1)
8	RTC	No	
9	ACPI	No	Note (2)
10	PCI	for PCI	Dynamic (BIOS default)
11	PCI	for PCI	Dynamic (BIOS default)
12	PS/2 Mouse	Yes (No)	Note (1)
13	FPU	No	
14	Primary IDE	No	Note (1)
15	PCI	for PCI	Dynamic (BIOS default)
16	PIRQ [A]	No	PCI IRQ line 1 + US15W graphics + SDcard + PCIe- Switch + HDAudio + SATA Bridge + USB client (if enabled) (3)
17	PIRQ [B]	No	PCI IRQ line 2 + SDcard + PCIe- Switch, Note (3)
18	PIRQ [C]	No	PCI IRQ line 3 + LAN Controller + PCIe- Switch, Note (3)
19	PIRQ [D]	No	PCI IRQ line 4 + PCIe- Switch + PCIe2PCI-Bridge, Note (3)
20	PIRQ [E]	No	USB UHCI Controller #1, Note (3)
21	PIRQ [F]	No	USB UHCI Controller #2, Note (3)
22	PIRQ [G]	No	USB UHCI Controller #3, Note (3)
23	PIRQ [H]	No	USB UHCI Controller #4, Note (3)

Note: (1) If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.
(2) Not available if ACPI is used
(3) ACPI OS decides on particular IRQ usage

7.2 Memory Area

The first 640 kB of DRAM are used as main memory. Using DOS, you can address 1 MB of memory directly. Memory area above 1 MB (high memory, extended memory) is accessed under DOS via special drivers such as HIMEM.SYS and EMM386.EXE, which are part of the operating system. Please refer to the operating system documentation or special textbooks for infor- mation about HIMEM.SYS and EMM386.EXE.

Other operating systems (Linux or Windows versions) allow you to address the full memory area directly.

Upper Memory	Used for	Available	Comment
A0000h – BFFFFh	VGA Memory	No	Mainly used by graphic controller
C0000h – CFFFFh	VGA BIOS	No	Used by onboard VGA ROM
D0000h – DFFFFh		Yes	Free for shadow RAM in standard configurations.
E0000h – FFFFFh	System BIOS	No	Fixed

7.3 I/O Address Map

The I/O-port addresses of the COMe-cSP2 are functionally identical to a standard PC/AT. All addresses not mentioned in this table should be available. We recommend that you do not use I/O addresses below 0100h with additional hardware for compatibility reasons, even if available.

I/O Address	Used for	Available	Comment
0000 - 001F	System Ressources	No	Fixed
0020 - 003F	Interrupt Controller 1	No	Fixed
002E - 002F	WB 83627	No	Fixed if WB83627HG is in system
0040 - 005F	Timer, Counter	No	Fixed
004E - 004F	TPM	No	Fixed if TPM is in system
0060 - 006F	Keyboard controller	No	Fixed
0070 - 007F	RTC and CMOS Registers	No	Fixed
0080	BIOS Postcode	No	Fixed
0081 - 008F	DMA Page Register	No	Fixed
00A0 - 00BF	Interrupt Controller 2	No	Fixed
00C0 - 00DF	DMA Controller 2	No	Fixed
00E0 - 00EF	System Control	No	Fixed
00F0 - 00FF	Math Coprocessor	No	Fixed
0170 – 0177 0376	Fixed Disk	No	Available if IDE port 1 is disabled
01F0 - 01F7 03F6	Fixed Disk	No	Available if IDE port 1 is disabled
0290-0295	WB83627 HWM	No	Fixed if WB83627HG is in system
03B0 - 03DF	VGA	No	Fixed
0400 - 043F	SMBus	No	Fixed
0480 - 04BF	GPIO	No	Fixed
04D0 - 04D1	PIC Extension	No	Fixed
0900 - 091F	Power Management	No	Fixed
09C0 - 09FF	GPE	No	Fixed
0A05 – 0A06	WB83627HG Hardware Monitor	No	Fixed if WB83627HG is in system
0A80 – 0A81	CPLD	No	in Future versions
C000 - CFFF	PCIe-to-PCI bridge	No	Dynamic (BIOS default address)
0CF8 - 0CFF	PCI Configuration	No	Fixed
D000 - DFFF	PCIe-to-PCI bridge	No	Dynamic (BIOS default address)
D880 - D88F	Sil SATA Controller	No	Dynamic (BIOS default address)
E080 - E09F	PCI USB Controller	No	Dynamic (BIOS default address)
E480 - E49F	PCI USB Controller	No	Dynamic (BIOS default address)
E880 - E887	VGA	No	Dynamic (BIOS default address)
EF00 - EF1F	PCI USB Controller	No	Dynamic (BIOS default address)
FFA0 - FFAF	PCI IDE Controller	No	Dynamic (BIOS default address)

7.4 Peripheral Component Interconnect (PCI) Devices

All devices follow the Peripheral Component Interconnect 2.3 (PCI 2.3) respectivily the PCI Express Base 1.0a specification. The BIOS and OS control memory and I/O resources. Please see the PCI 2.3 specification for details.

PCI Device	PCI IRQ	Interface	Comment
Host Bridge / Memory Controller	None		Integrated in chipset
Graphics / Video Controller	INTA		Integrated in chipset
USB Client Controller	INTA		Integrated in chipset
HD Audio Controller	INTA		Integrated in chipset
PCIexpress Port (Bridge)	INTA		Integrated in chipset
PCIexpress Port (Bridge)	INTB		Integrated in chipset
UHCI USB Controller 1	INTE		Integrated in chipset
UHCI USB Controller 2	INTF		Integrated in chipset
UHCI USB Controller 3	INTG		Integrated in chipset
EHCI USB Controller	INTH		Integrated in chipset
SDIO/MMC Controller 1	INTA		Integrated in chipset
SDIO/MMC Controller 2	INTB		Integrated in chipset
ISA Bridge / LPC Controller	None		Integrated in chipset
IDE Controller	None		Integrated in chipset
Network Controller	INTC	PCI Express	External i82574
SATA	INTA	PCI Express	External SIL3132

Note: POST Codes (Power On Self Test) are not routed via PCI interface and are only available via LPC.

7.5 External I2C Bus #1

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	JIDA-EEPROM	No	EEPROM for CMOS Data	0
A2h	JIDA-EEPROM	No	EEPROM for CMOS Data	0

7.6 External I2C Bus #2

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
B0h	Watchdog	NO	external WD PIC	2

7.7 JILI I2C Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	JILI-EEPROM	No	EEPROM for JILI Data	4

7.8 SDVO I2C Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
				3

7.9 System Management (SM) Bus

Address	Device	Comment	JIDA Bus Nr.
12h	SMART_CHARGER	Not to be used with any SM bus deivce except a charger	1
14h	SMART_SELECTOR	Not to be used with any SM bus deivce except a selector	1
16h	SMART_BATTERY	Not to be used with any SM bus deivce except a battery	1
5Ch	Winbond W83L786NG HWM	Do not use under an circumstances	1
A0h	SPD EEPROM on DDR2 memory	Do not use under an circumstances	1
D2h / DCh	Clock Gen CK610/ICS9DB403	Do not use under an circumstances	1
E6h	PCA9538 Digital I/O (GPIO)	Do not use under an circumstances	1
7Eh	PEX8509 PCIe switch	Do not use under an circumstances	1

7.10 K-Station / JIDA32 resources

I2C

BUS	Function
I2C 0	Internal / JIDA I2C #1
I2C 1	SM-Bus
I2C 2	Internal / JIDA I2C #2 (for slow devices)
I2C 3	SDVO I2C
I2C 4	JILI I2C

Storage

Device	Function
EEPROM 0	JIDA EEPROM Area1 with 32 Bytes (free to use)
EEPROM 1	JIDA EEPROM Area 2 with 33 Bytes (reserved)

GPIO

Port	Function
IO-Port 0	GPIO Port, Bit 0-3: Input, Bit 4-7: Output

Hardware Monitor

Sensor	Function
Temp 0	CPU ACPI Temperature (measured with Winbond W839786 HWM)
Temp 1	Module Temperature (internal IC temperature of onboard Winbond W839786 HWM)
FAN 0	Module CPU fan sensor (measured with Winbond W839786 HWM)
Voltage 0	Winbond 839786 Voltage Sensor 0: CoreA
Voltage 1	Winbond 839786 Voltage Sensor 1: VRAM
Voltage 2	Winbond 839786 Voltage Sensor 2: +3.3V

8 BIOS Operation

The module is equipped with AMI® BIOS, which is located in an onboard SPI serial flash memory. You can update the BIOS using a Flash utility.

8.1 Determining the BIOS Version

To determine the AMI® BIOS version, immediately press the Pause key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

- AMIBIOS © 2006 American Megatrends, Inc.
- BIOS Date: 06/16/08 10:52:49 Ver: 08.00.14
- Kontron® BIOS Version <EEP1RXXX>
- © Copyright 2002-2008 Kontron Embedded Modules GmbH

8.2 Setup Guide

The AMIBIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

Note:	Selecting incorrect values may cause system boot failure. Load setup default values to recover by pressing <F9>.

8.2.1 Start AMI® BIOS Setup Utility

To start the AMI® BIOS setup utility, press <DEL> when the following string appears during bootup.

Press <DEL> to enter Setup

The Info Menu then appears.

The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Right side Bottom	Lists setup navigation keys.
Item Specific Help Window	Right side Top	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (▸) marks all submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

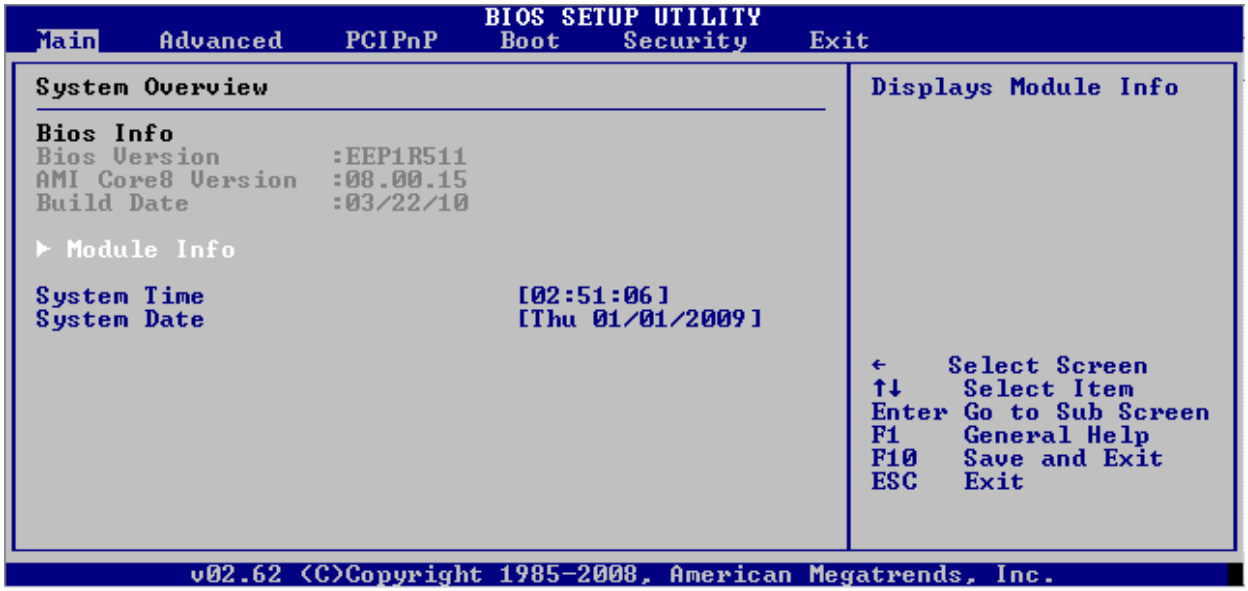
General Help Window

Pressing <F1> or <Alt-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

8.3 BIOS Setup

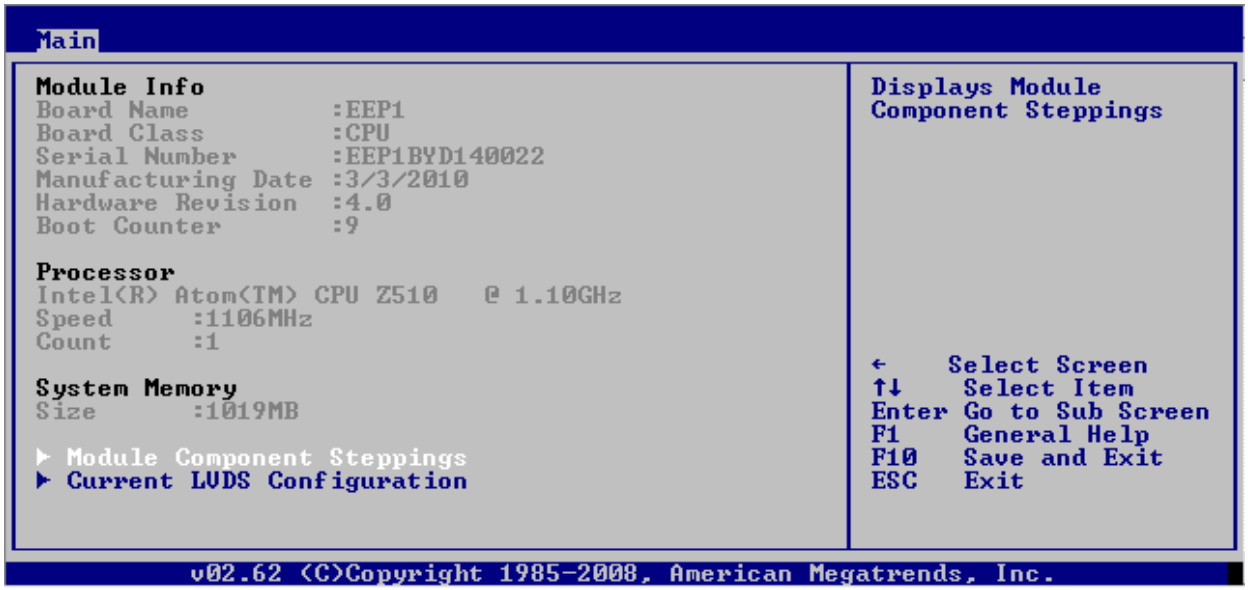
Note:	Default settings are marked bold

8.3.1 Main Menu

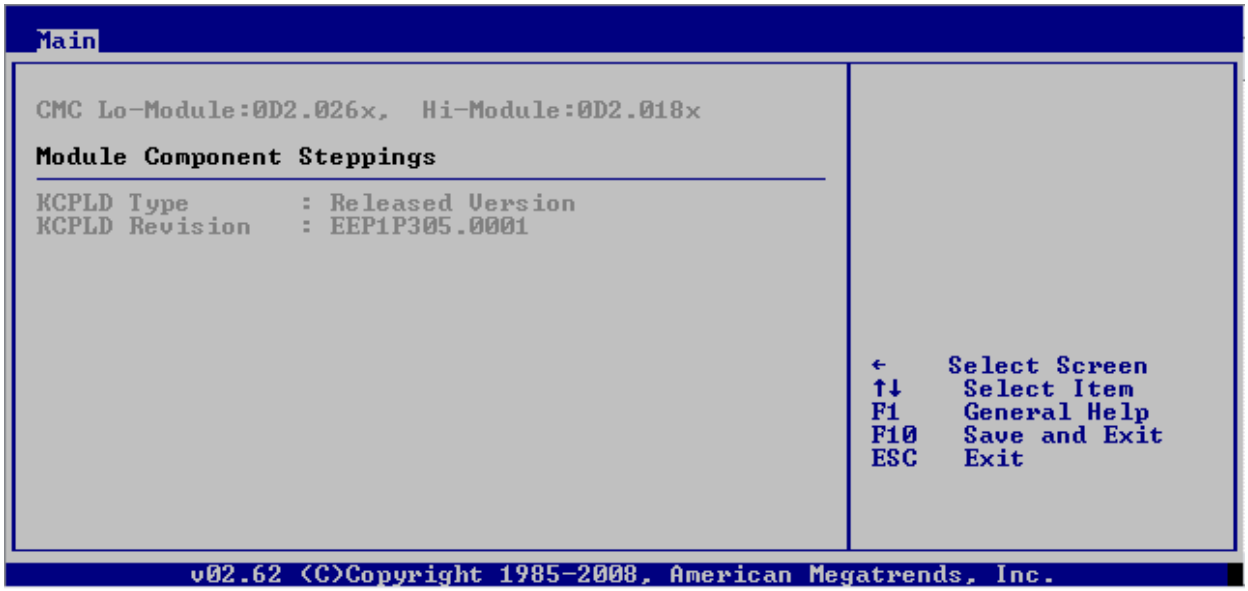


Feature	Option	Description
System Time	[hh:mm:ss]	<Tab>, <Shift-Tab>, or <Enter> selects field
System Date	[mm-dd-yyyy]	<Tab>, <Shift-Tab>, or <Enter> selects field

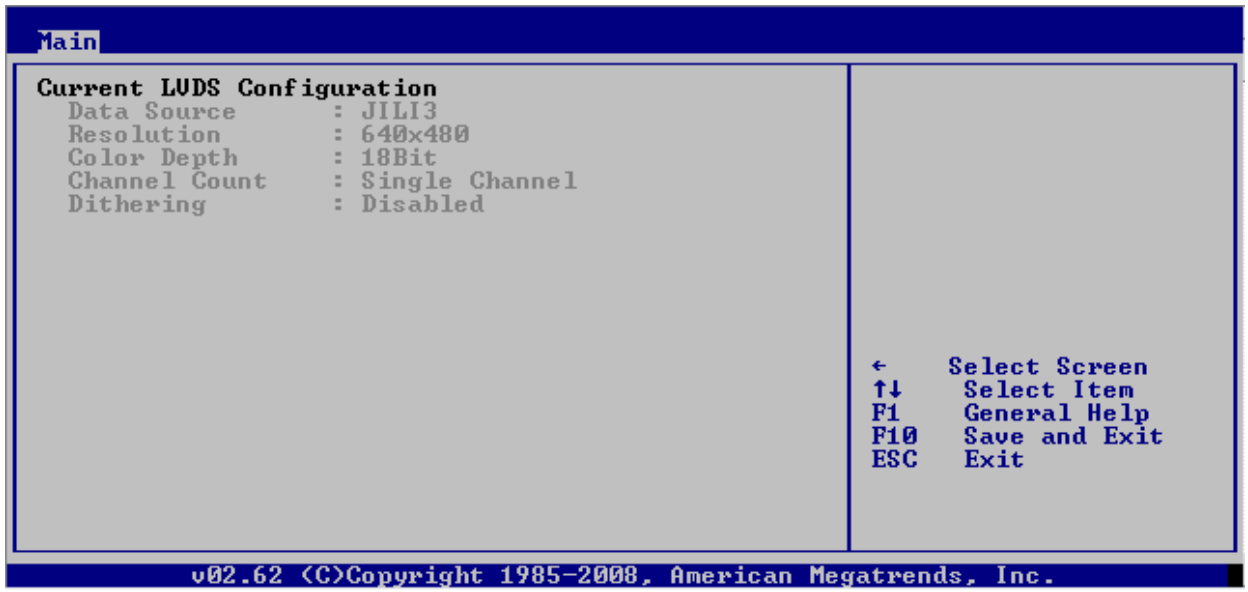
8.3.2 Module Info



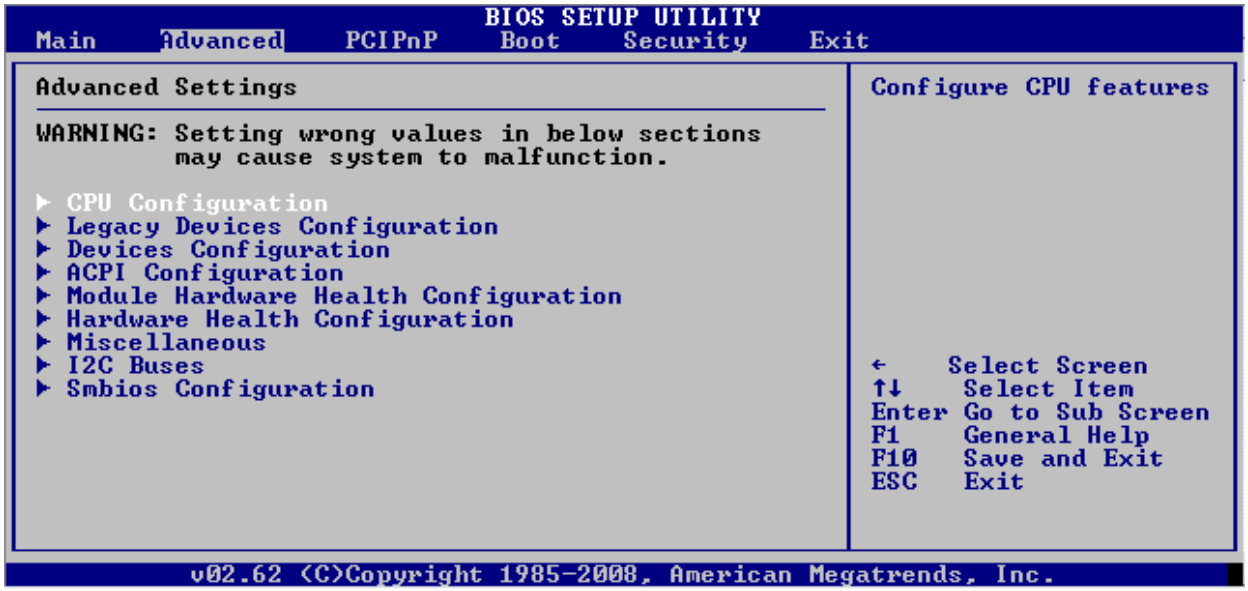
Module Component Steppings



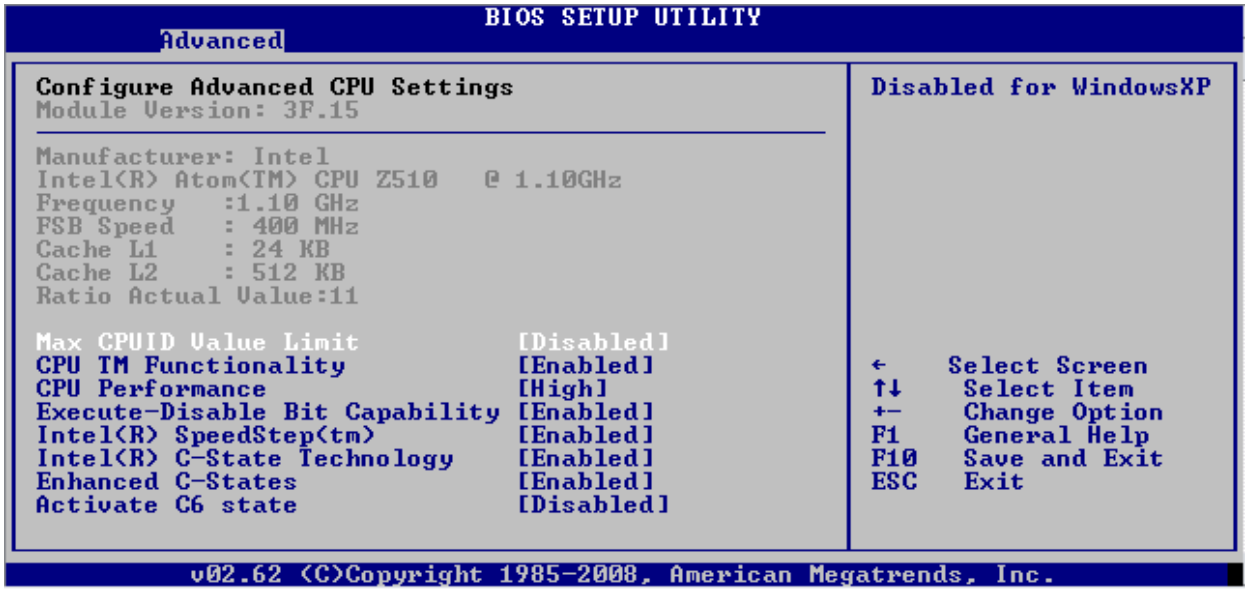
Current LVDS Configuration



8.3.3 Advanced Menu

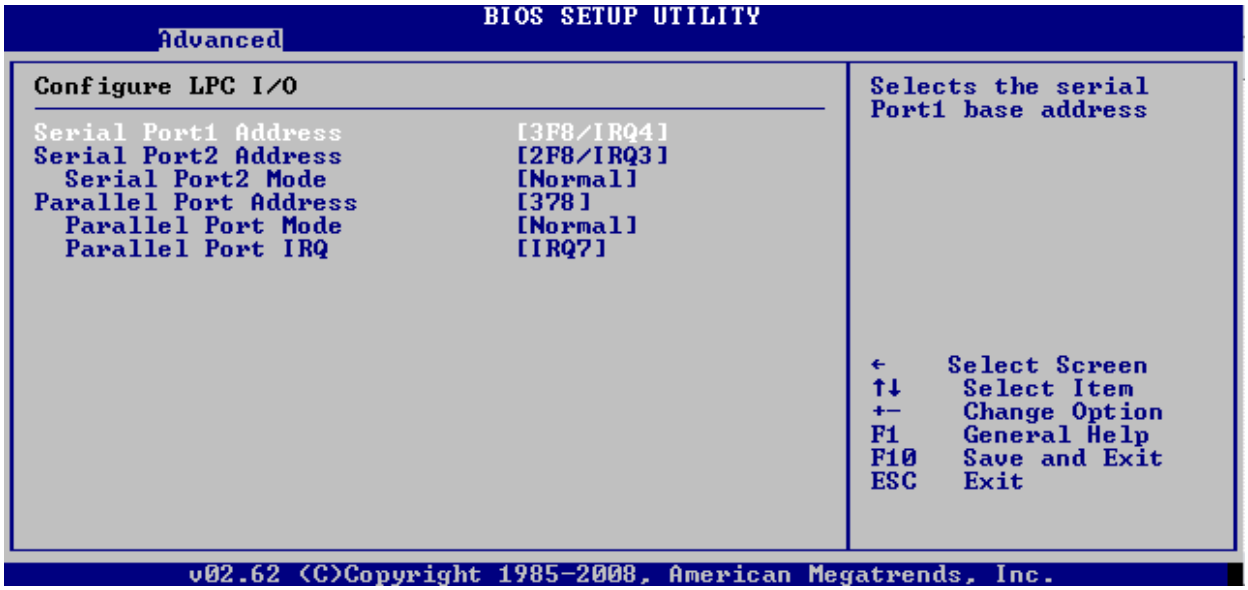


CPU Configuration



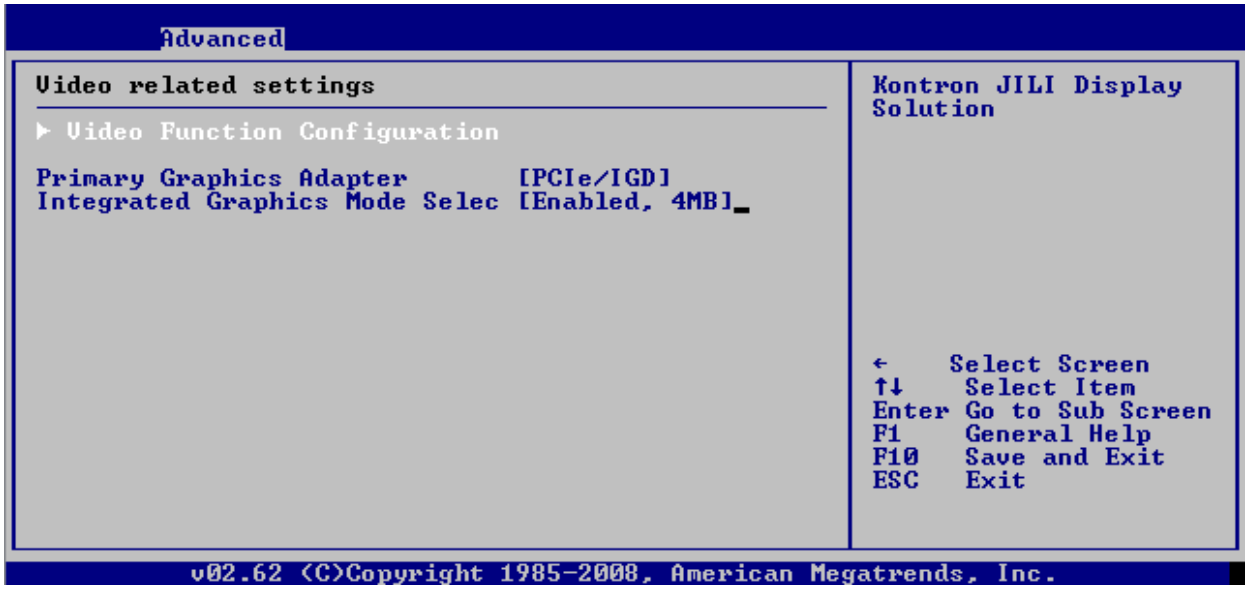
Feature	Option	Description
Max CPUID Value Limit	**Disabled** Enabled	Disabled for WindowsXP
CPU TM Functionality	Disabled **Enabled**	Enables or disables both TM1 and TM2 simultaneously.
CPU Performance	Low Middle **High**	Sets the CPU ratio for Z510 / Z530 CPU Low: 600MHz / 800MHz Middle: 800MHz / 1200MHz High: 1100MHz / 1600MHz Note: Speedstep is disabled if CPU P-State is fixed to low or middle
Execute-Disable Bit Capability	**Enabled** Disabled	When disabled, force the XD feature flag to always return 0
Hyper Threading Technology	**Enabled** Disabled	Enables or Disables Intel® Hyper Threading Technology
Intel® SpeedStep™	**Enabled** Disabled	Enables and Disables the SpeedStep power management feature
Intel® C-State tech	**Enabled** Disabled	Enables and Disables the C - States. If enabled, the CPU is set to C2 - C6 state in idle mode
Enhanced C-STATE	**Enabled** Disabled	CPU idle is set to enhanced C-states
Activate C6 state	**Disabled** Enabled	Enables and disables the usage of the C6 state.

Legacy Devices Configuration



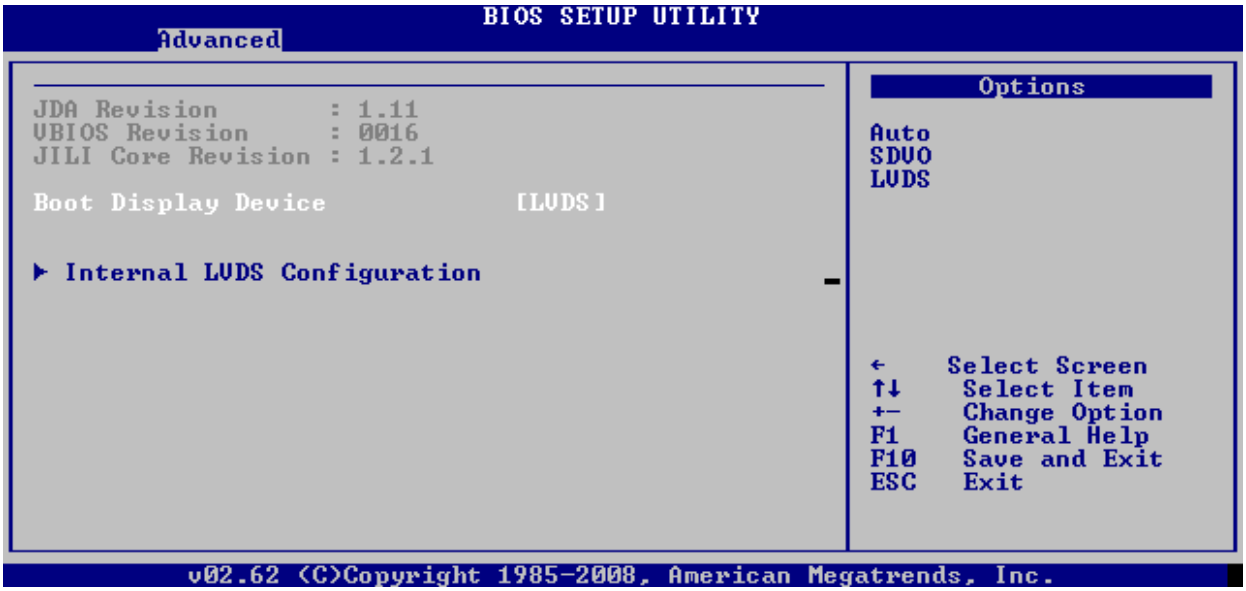
Feature	Option	Description
Serial Port1 Address	Disabled **3F8/IRQ4** 3E8/IRQ4 2E8/IRQ3	Selects the serial Port 1 base address
Serial Port2 Address	Disabled **2F8/IRQ3** 3E8/IRQ4 2E8/IRQ3	Selects the serial Port 2 base address
Serial Port2 Mode	**Normal** IrDA ASK IR	Selects the mode for serial Port2
Parallel Port Address	Disabled **378** 278 3BC	Selects the parallel Port base addrdess
Parallel Port Mode	**Normal** Bi-Directional ECP EPP ECP & EPP	Selects the parallel Port mode
Parallel Port IRQ	IRQ5 **IRQ7**	Selects the parallel Port IRQ

Devices - Configuration - Video Configuration



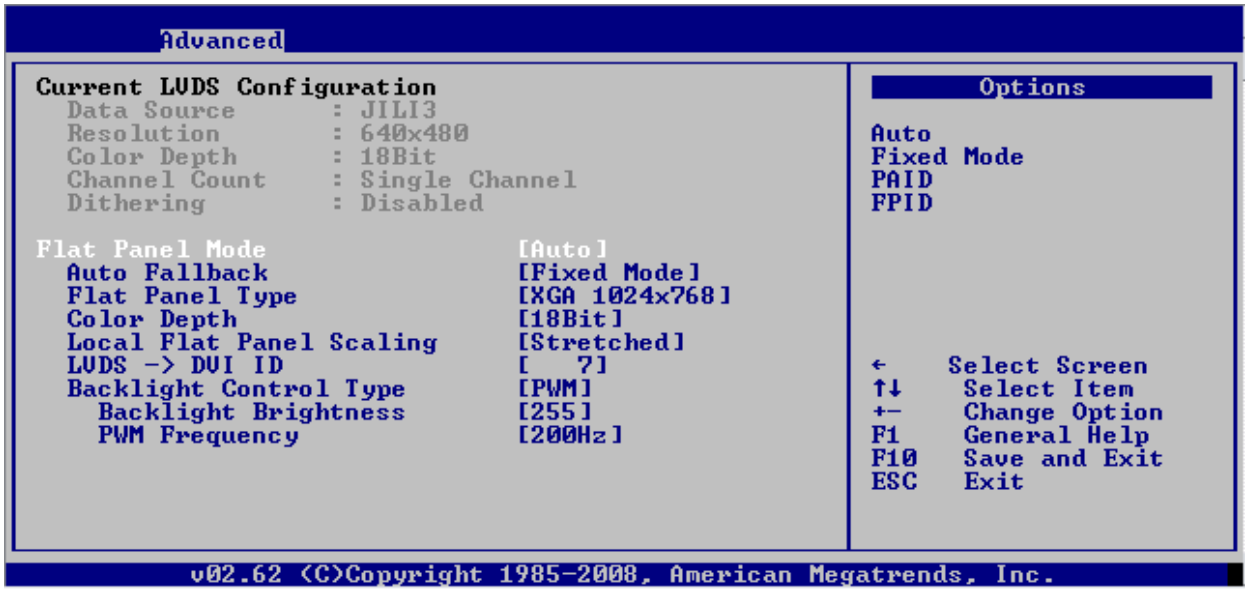
Feature	Option	Description
Video Function Configuration	Submenu	Kontron JILI Display Solution
Primary Graphics Adapter	Onboard **PCIe/Onboard**	Selects which graphics controller is used as primary boot device (boot sequence)
Onboard Graphics Mode	Enabled, 1 MB **Enabled, 4 MB** Enabled, 8 MB	Selects the amount of pre-allocated system memory used by the onboard graphics controller

Devices - Conficuration - Video Configuration - Video Function Configuration



Feature	Option	Description
Boot Display Device	**Auto** SDVO LVDS	Select the Boot Display Device.
▸ Internal LVDS Configuration	Submenu	

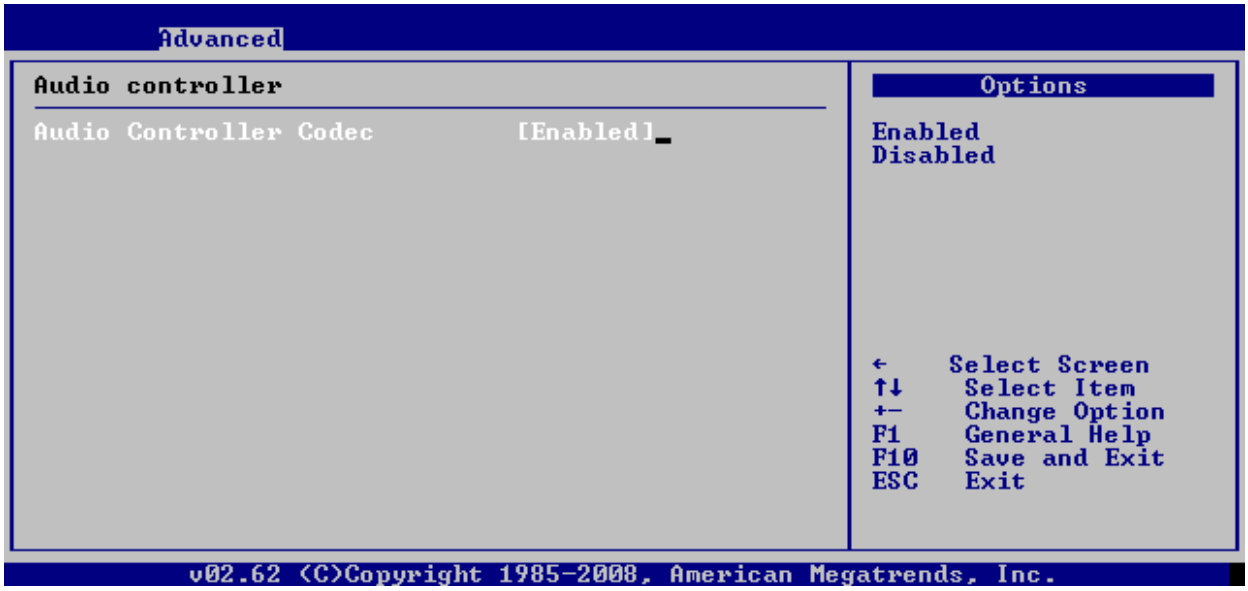
Devices - Conficuration - Video Configuration - Video Function Configuration - Internal LVDS Configuration



Feature	Option	Description
Flat Panel Mode	**Auto** Fixed Mode PAID FPID	Select the Flat Panel Mode Auto: Load settings from Configuration EEPROM and if not present use settings from 'Auto Fallback' Fixed mode: Use manual settings PAID/FPID: Use Panel Adapter / Flat Panel ID
Auto Fallback	**Fixed Mode** Disabled	Use fixed settings for LVDS out or disable LVDS if no Configuration EEPROM is detected
Flat Panel Type	VGA 640x480 SVGA 800x600 **XGA 1024x786** WXGA 1280x786 WVGA 800x480 WXGA 1266x768 WXGA 1280x800	Select Resolution of used Flat Panel
PAID/FPID	[...]	Enter the Panel Adapter or Flat Panel ID (only available when PAID/FPID is selected in Flat Panel Mode)
Color Depth	**18Bit** 24Bit	Select Display Color Depth
Local Flat Panel Scaling	Centered **Stretched** Disabled	Select the Scaling for the flat panel
LVDS -> DVI ID	5 **7**	Select the type of used LVDStoDVI converter 5 = 1x18bit Adapter, 7 = 1x24bit Adapter
Backlight Control Type	None/External I2C **PWM**	Select how the panel backlight is controlled
Backlight Brightness	**[128]**	Set LCD backlight brightness (0-255)

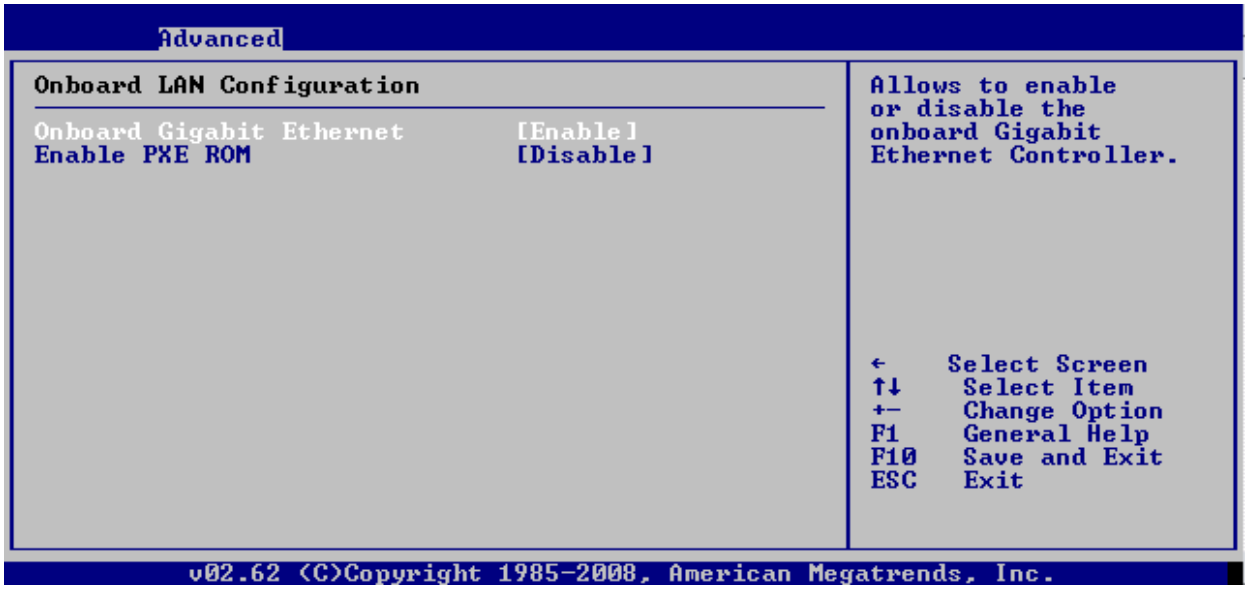
PWM Frequency	**200 HZ** 400 Hz 1 kHz 2 kHz 4 kHz 8 kHz 20 kHz 32 kHz	Selects the value of the regarding PWM base frequency.

Devices Conficuration - Audio Configuration



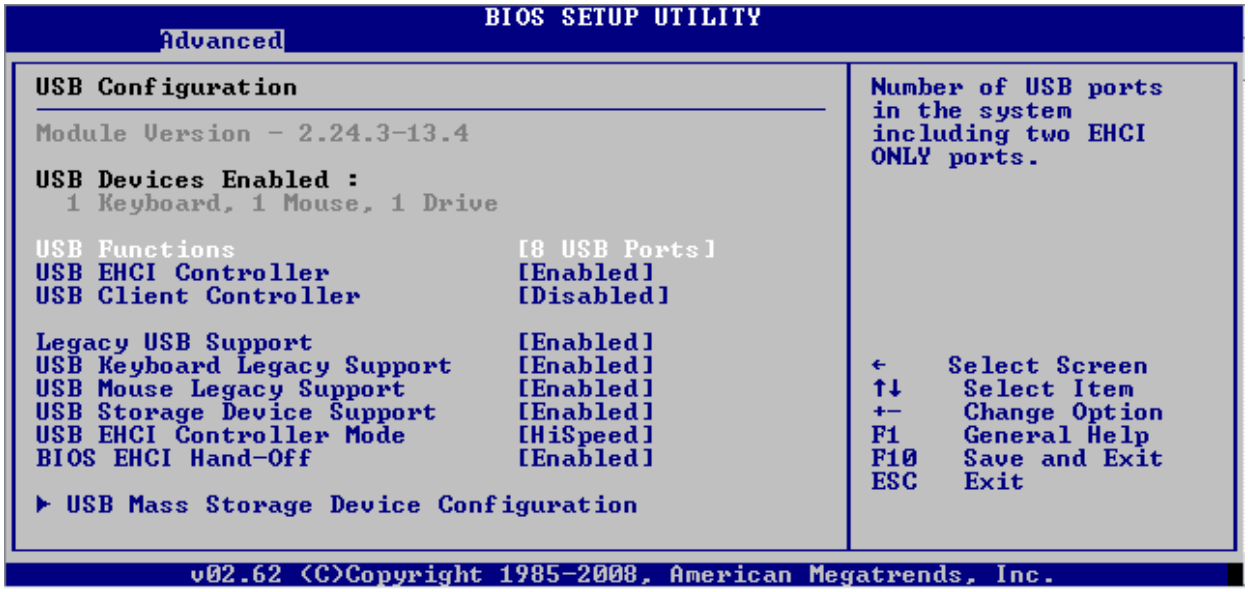
Feature	Option	Description
Audio Controller Codec	**Enabled** Disabled	Enable or Disable HDAudio to external Codec

Devices Conficuration - Onboard LAN



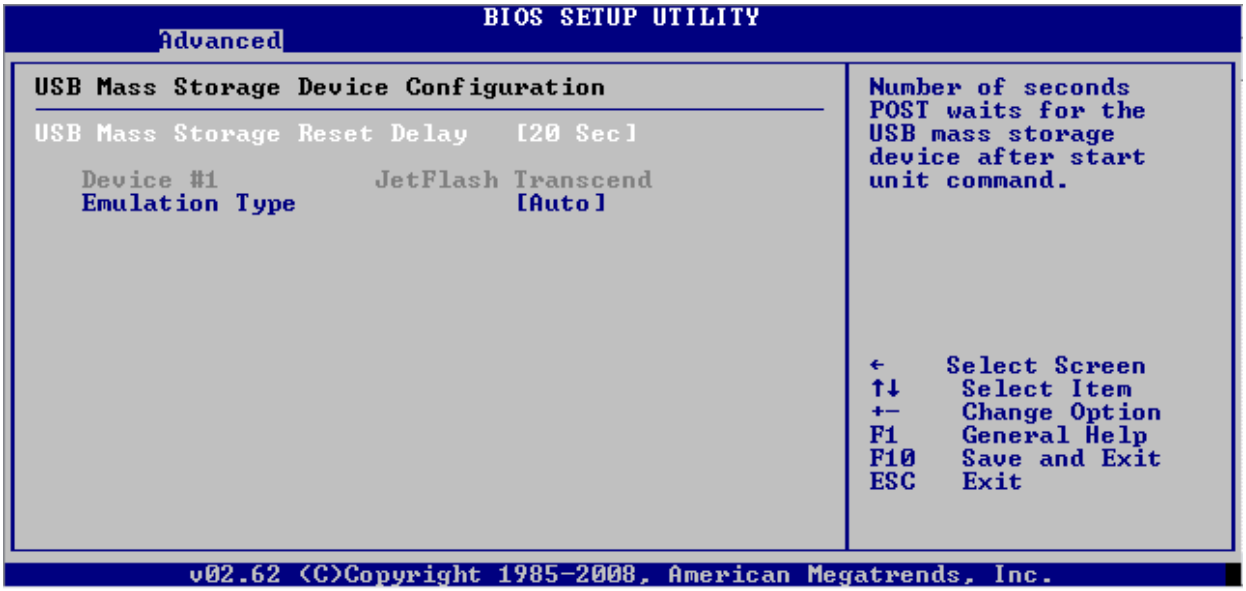
Feature	Option	Description
Onboard Gigabit Ethernet	**Enable** Disable	Allows to enable or disable the onboard Gigabit Ethernet Controller
Enable PXE ROM	Enable **Disable**	Allows to enable or disable PXE ROM which is needed to boot from LAN

Devices Conficuration - USB Configuration



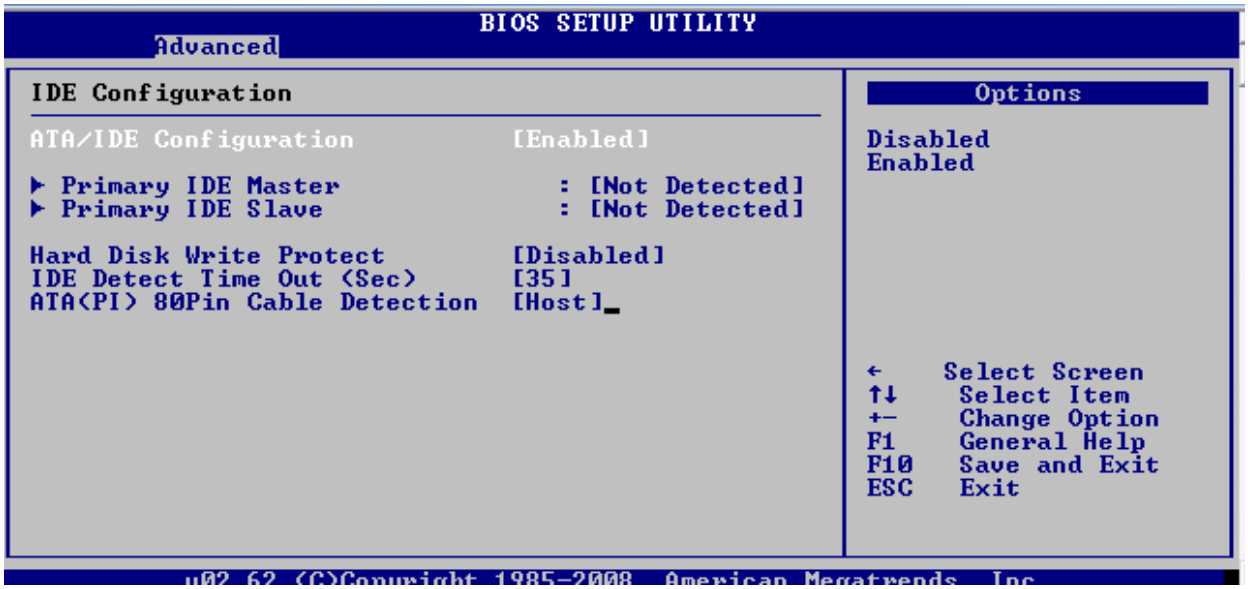
Feature	Option	Description
USB Functions	Disabled 2 Ports 4 Ports 6 Ports **8 Ports**	Number of USB ports in the system including the two EHCI ONLY ports.
USB EHCI Controller	**Enabled** Disabled	Controls EHCI (USB 2.0) functionality for all the UHCI ports set to active state
USB Client Controller	Enabled **Disabled**	This enables the USB client functionality on COM Express USB Port #7
Legacy USB Support	Disabled **Enabled** Auto	Enables support for legacy USB. AUTO option disables legacy support if no USB devices are connected
USB Keyboard Legacy Support	**Enabled** Disabled	Enables legacy support for USB keyboard
USB Mouse Legacy Support	**Enabled** Disabled	Enables legacy support for USB mouse
USB Storage Device Support	**Enabled** Disabled	Enables support for USB mass storage devices
USB 2.0 Controller Mode	FullSpeed **HiSpeed**	Configures the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps)
BIOS EHCI Hand-Off	Disabled **Enabled**	This is a workaround for an OS without EHCI hand-off support. The EHCI ownership change should claim by the EHCI driver

USB Mass Storage Device Configuration



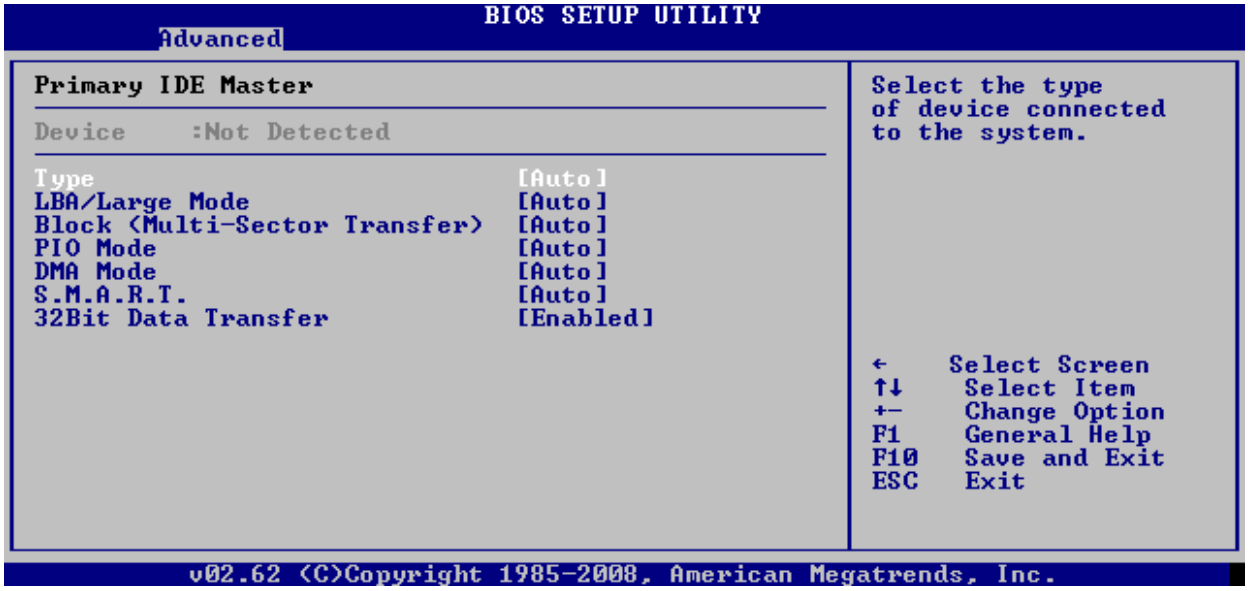
Feature	Option	Description
USB Mass Storage Reset Delay	10 Sec **20 Sec** 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	Controls EHCI (USB 2.0) functionality for all the UHCI ports set to active state

Devices Conficuration - IDE Configuration



Feature	Option	Description
ATA/IDE Configuration	Disabled **Enabled**	Enables or disables the IDE interface of US15W SCH.
▸ Primary IDE Master	Submenu	While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of autodetection of IDE Devices
▸ Primary IDE Slave	Submenu	While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of autodetection of IDE Devices
Hard Disk Write Protect	**Disabled** Enabled	Allows the write protection of Hard Disk devices. Only valid if the device is accessed through the BIOS
IDE Detect Time Out (Sec.)	0, 5, 10, 15 20, 25, 30, 35	Selects the time out value for the detection of ATA/ ATAPI devices
ATA(PI) 80Pin Cable Detection	Host & Device **Host** Device	Selects the 80 Pin Cable Detection Methode

Devices Conficuration - IDE Configuration - IDE Master/Slave Submenu

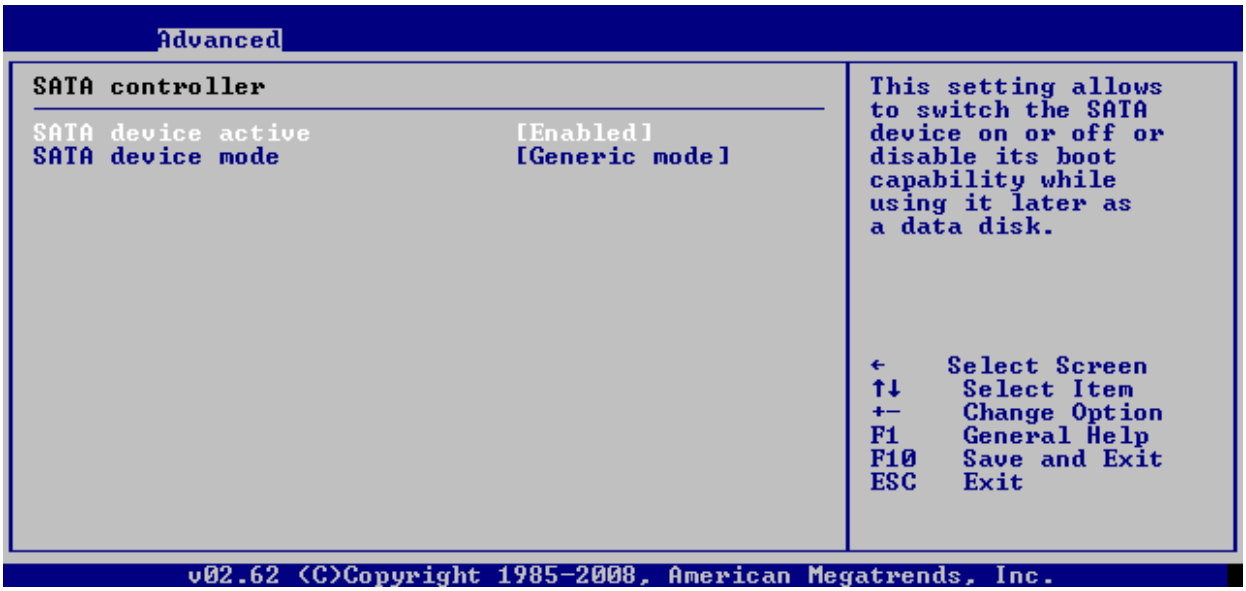


Feature	Option	Description
Type	Not Installed **Auto** CD/DVD ARMD	Selects the type of the IDE Devices connected to the system
LBA/Large Mode	Disabled **Auto**	Disables the LBA mode or enables it, when a device supports it
Block (Multi-Sector Transfer)	Disabled **Auto**	Disabled: The data transfer from and to the device occurs one sector ata atime Auto: The data transfer from and to the device occurs multiple sectors at a time if the device supports ist
PIO Mode	**Auto** 0 1 2 3 4	(Auto) Configures the PIO Mode
DMA Mode	**Auto** SWDMAn MWDMAn UDMAn	SWDMA: Single Word DMA MWDMA: Multi Word DMA UDMA: Ultra DMA
S.M.A.R.T.	**Auto** Enabled Disabled	Disables, Enables or automatically enables the S.M.A.R.T feature (Self-Monitoring, Analysis and Reporting Technology)
32Bit Data Transfer	**Enabled** Disabled	Disables and Enables the 32Bit Data Transfer Mode

Devices Conficuration - On-Module SDIO Configuration

Feature	Option	Description
Enable SDIO Host Controller	Disable HC0 **HC0+1**	Disable/Enable SDIO host controllers. Numbers refer to the three possible HC's (named 0, 1 and 2)
SDIO Controller	**GPIO** SDIO	SDIO Slot 1 lines may be routed as secondary SDIO channel or as generic I/O. If using GPIO control with this module it is necessary to set this switch to GPIO
Data Access Mode	**Auto** DMA PIO	Auto Option: Access SD device in DMA mode if controller supports it, otherwise in PIO mode. DMA Option: Access SD device in DMA mode. PIO Option: Access SD devie in PIO mode.

Devices Conficuration - SATA Configuration

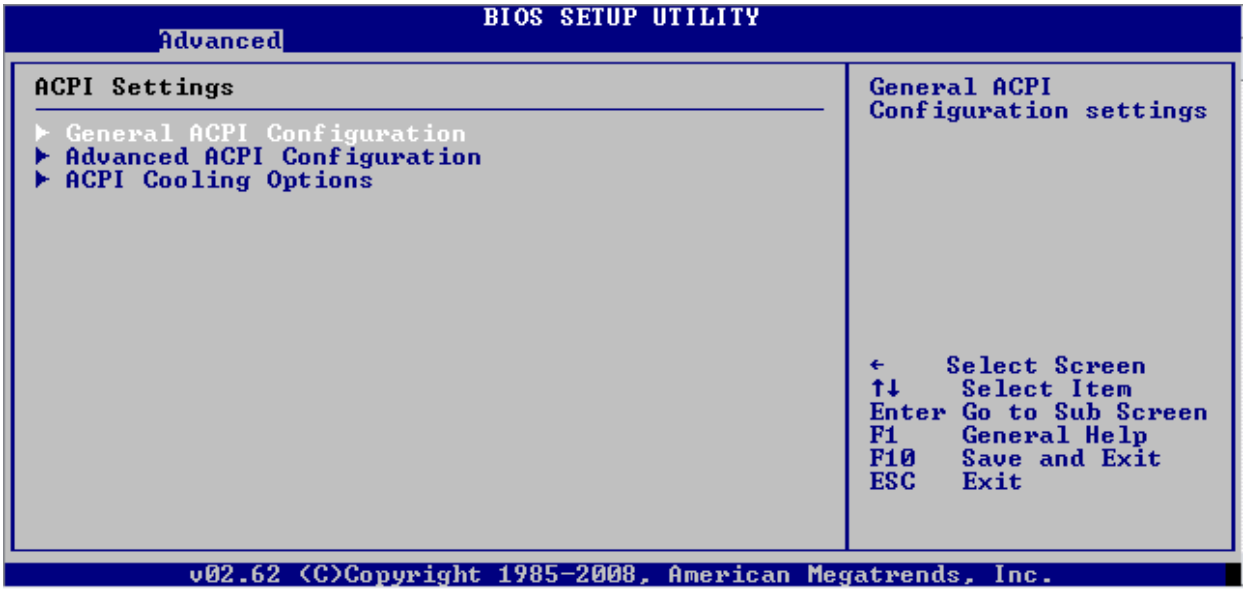


Feature	Option	Description
SATA device active	**Enabled** Disabled	This setting allows to switch the SATA device on or off or disable its boot capability while using it later as a data disk
SATA device mode	**Generic mode** RAID mode	This setting allows to choose between a generic usage of the SATA interface or a SATA RAID mode. Previously installed OS images might not be running anymore if this option was changed

Devices Conficuration - PCI Express Configuration

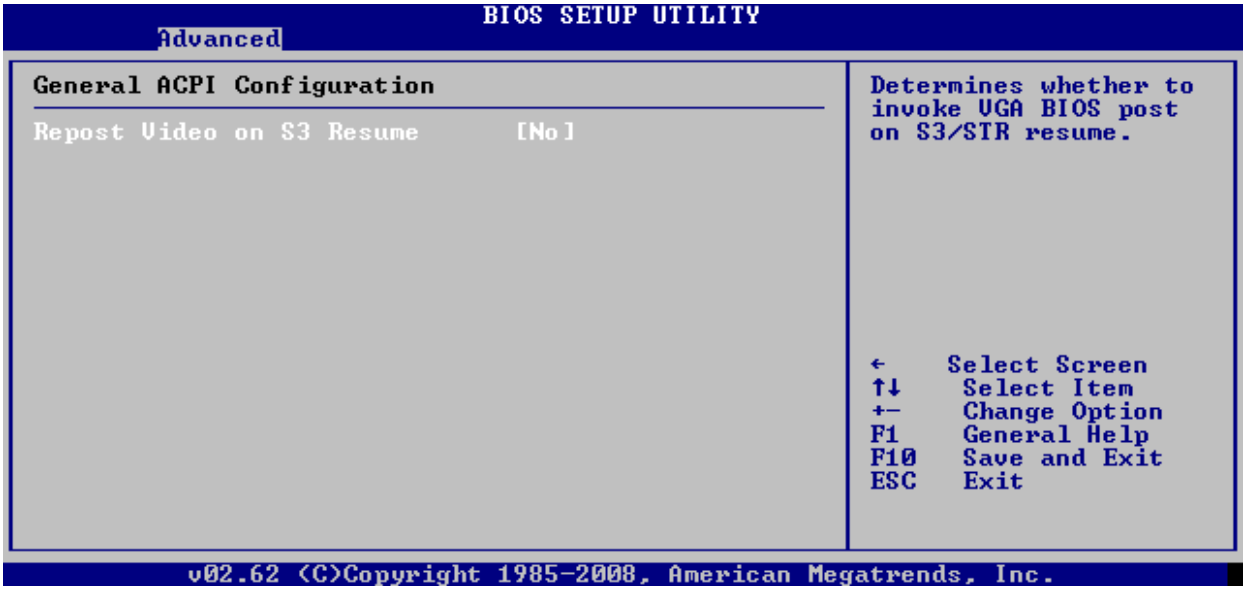
Feature	Option	Description
PCIe Port 0	**Auto** Enabled Disabled	Enables or disables PCIe Port 0 Note: This Port is used for onboard PCIe Switch
PCIe Port 1	**Auto** Enabled Disabled	Enables or disables PCIe Port 1
PCIE Base Spec Compliance	**Enabled** Disabled	Allows to choose between strict PCIE base specification compliance and power saving mode
SDVO PCIE Base Spec Compliance	Enabled **Disabled**	Allows to choose between strict PCIE base specification compliance and power saving mode
Active State Power-Management	Enabled **Disabled**	Enable/Disable PCI Express L0s and L1 link power states

ACPI Configuration



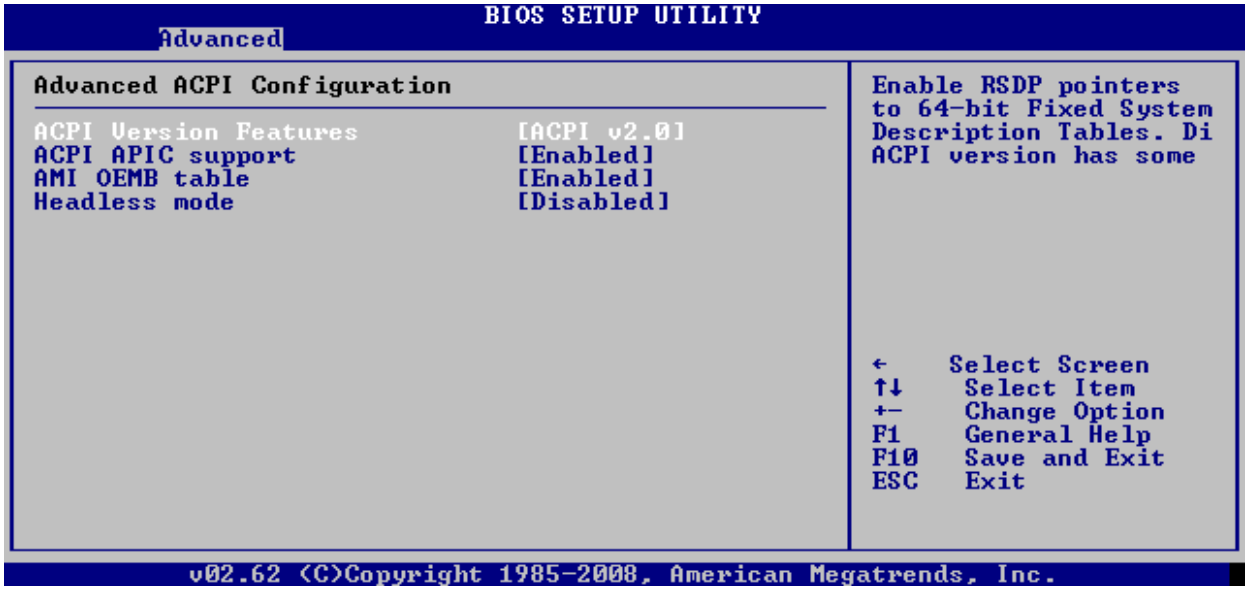
Feature	Option	Description
▸ General ACPI Configuration	Submenu	
▸ Advanced ACPI Configuration	Submenu	
▸ ACPI Cooling Options	Submenu	

ACPI Configuration - General ACPI Configuration



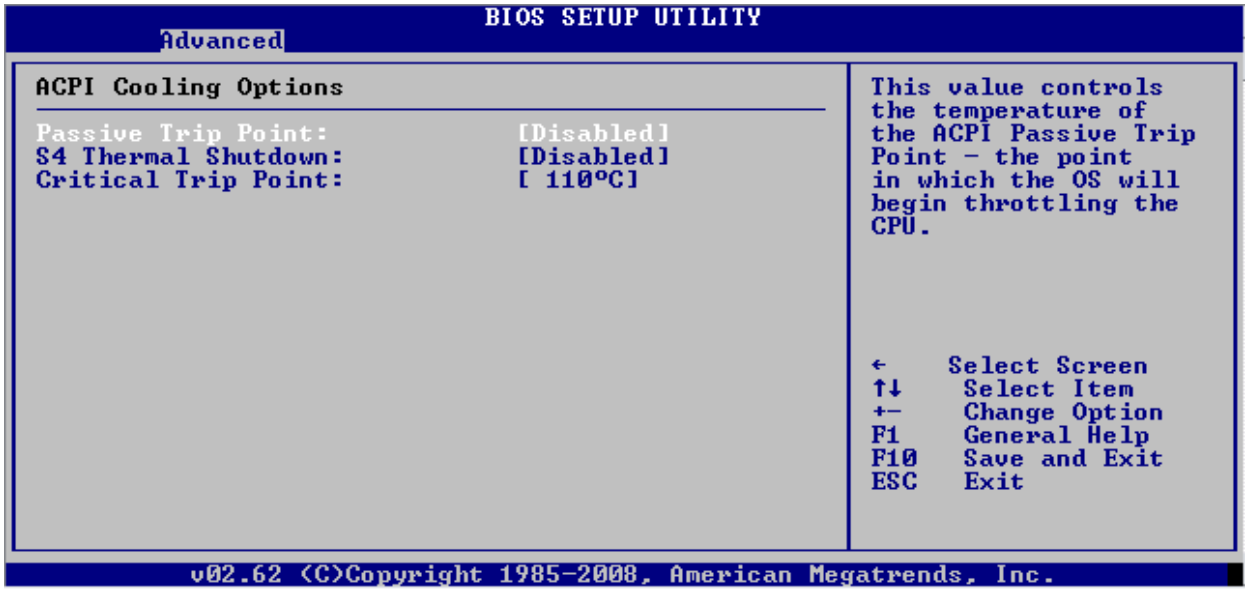
Feature	Option	Description
Repost Video on S3 Resume	**No** Yes	Determines whether to invoke VGA BIOS post on S3/STR resume

ACPI Configuration - Advanced ACPI Configuration



Feature	Option	Description
ACPI Version	ACPI 1.0 **ACPI 2.0** ACPI 3.0	Selects the desired ACPI specification (OS depending)
ACPI APIC Support	Disabled **Enabled**	Include ACPI APIC table pointer to RSDT pointer list. APIC supports more IRQs and faster interrupt handling
AMI OEMB Table	Disabled **Enabled**	Includes the AMI OEMB table pointer. The OEMB table is used to fill in POST data in AML code during ACPI OS operations. This option should only be disabled if ACPI 1.0 is used
Headless Mode	**Disabled** Enabled	Indicates support for headless operation, that means without keyboard, mouse and/or monitor. The OS must support the headless mode

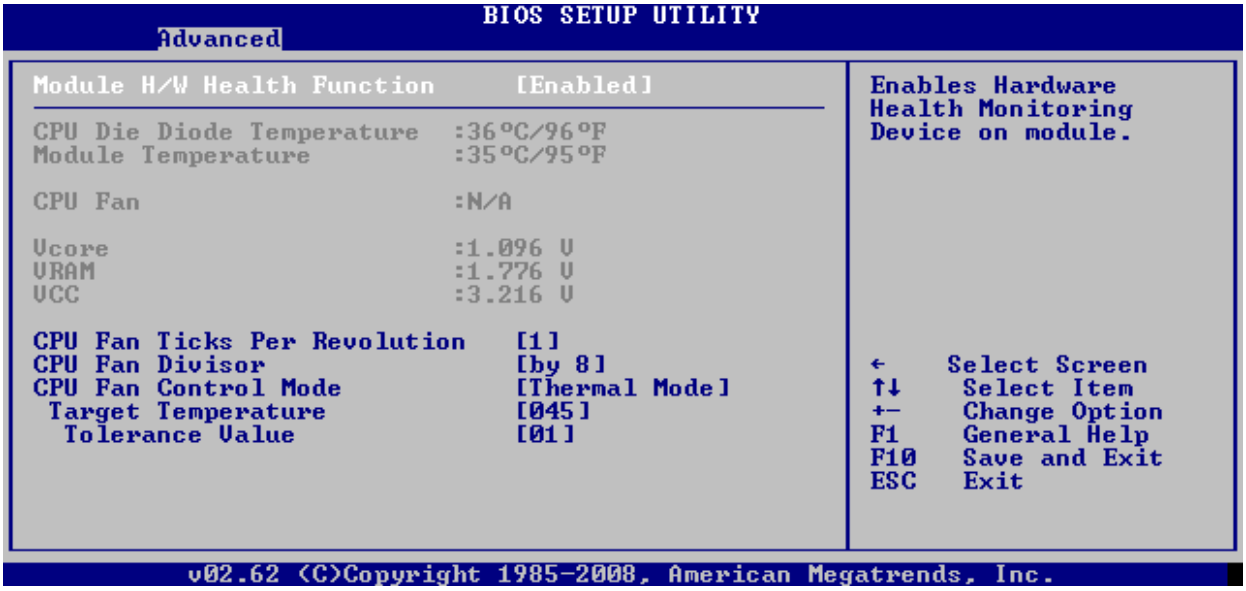
ACPI Configuration - ACPI Cooling Options



Feature	Option	Description
Passice Trip Point	**Disabled** 40°C 45°C 50°C 55°C 60°C 65°C 70°C 75°C 80°C 85°C 90°C 95°C 100°C 105°C 110°C	This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the CPU.
S4 Thermal Shutdown	**Disabled** 40°C 45°C 50°C 55°C 60°C 65°C 70°C 75°C 80°C 85°C 90°C 95°C	This value controls the temperature at which the system will shutdown to a S4 state (if S4 was enabled before)

	100°C 105°C 110°C	
Critical Trip Point	40°C 45°C 50°C 55°C 60°C 65°C 70°C 75°C 80°C 85°C 90°C 95°C 100°C 105°C **110°C**	This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut the system off.

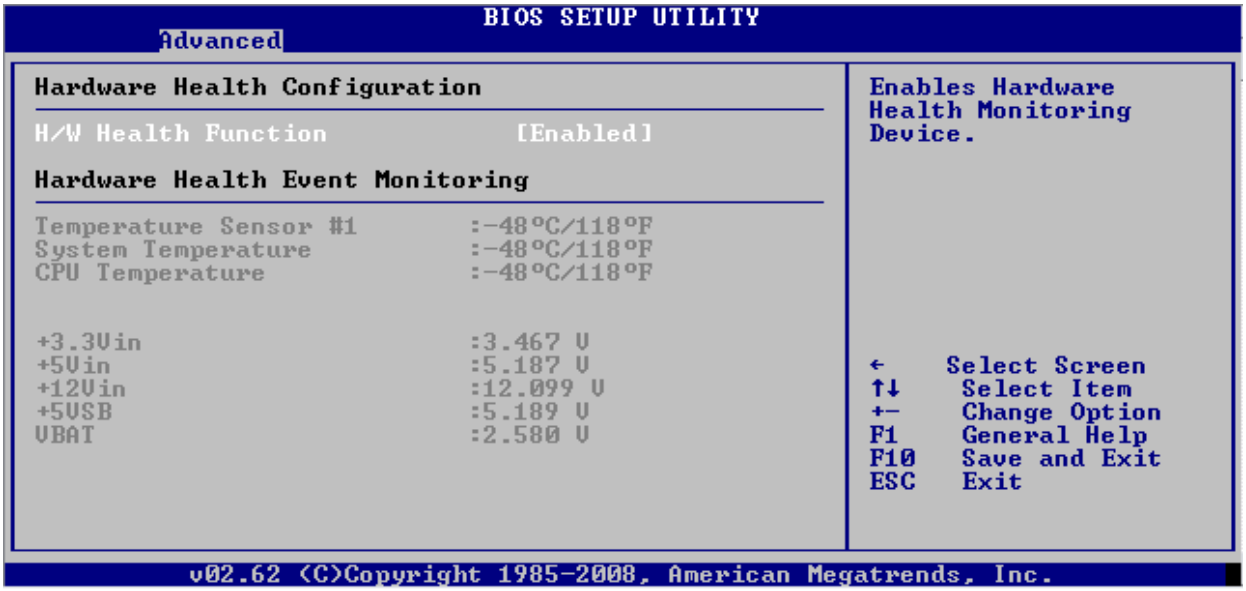
Module Hardware Health Configuration



Feature	Option	Description
Module H/W Health Function	**Enabled** Disabled	Enables Hardware Health Monitoring Device on module
CPU FAN Ticks Per Revolution	**1** 2 4 8	Set 'Ticks per rev' according to number of impulses sent by this type of fan during one full revolution
CPU Fan Divisor	1 2 4 **8** 16 32 64 128	Adjust Fan Divisor to allow for best display when the rotation is at the edges of the range. If the value gets out of range the fan would be displayed non-working although still running. Divisor 1: 8800 rpm Divisor 2: 4400 rpm Divisor 4: 2200 rpm Divisor 8: 1100 rpm Divisor 16: 550 rpm Divisor 32: 275 rpm Divisor 64: 137 rpm Divisor 128: 68 rpm
CPU Fan Control Mode	Manual Mode **Thermal Mode** SMARTFAN TM II	Specify different modes to control the fan
CPU Fan Output Level	15	PWM/DC Output Level 0: fan output is always logical low or at min voltage 15: fan output is always logical high or at max voltage xx: fan output logic output level is (xx/16*100%)
Target Temperature	045	Temperature value where the fan starts to work Min = 0, Max = 127
Tolerance Value	01	Tolerance Value

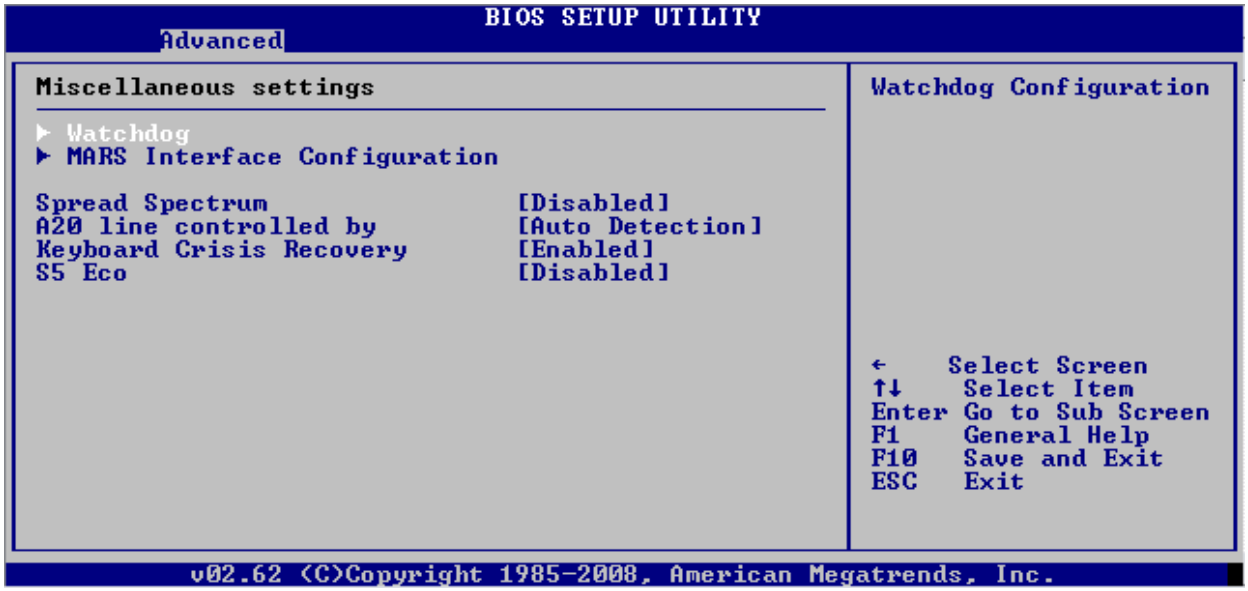
		Min = 0, Max = 15

(Baseboard) Hardware Health Configuration Menu



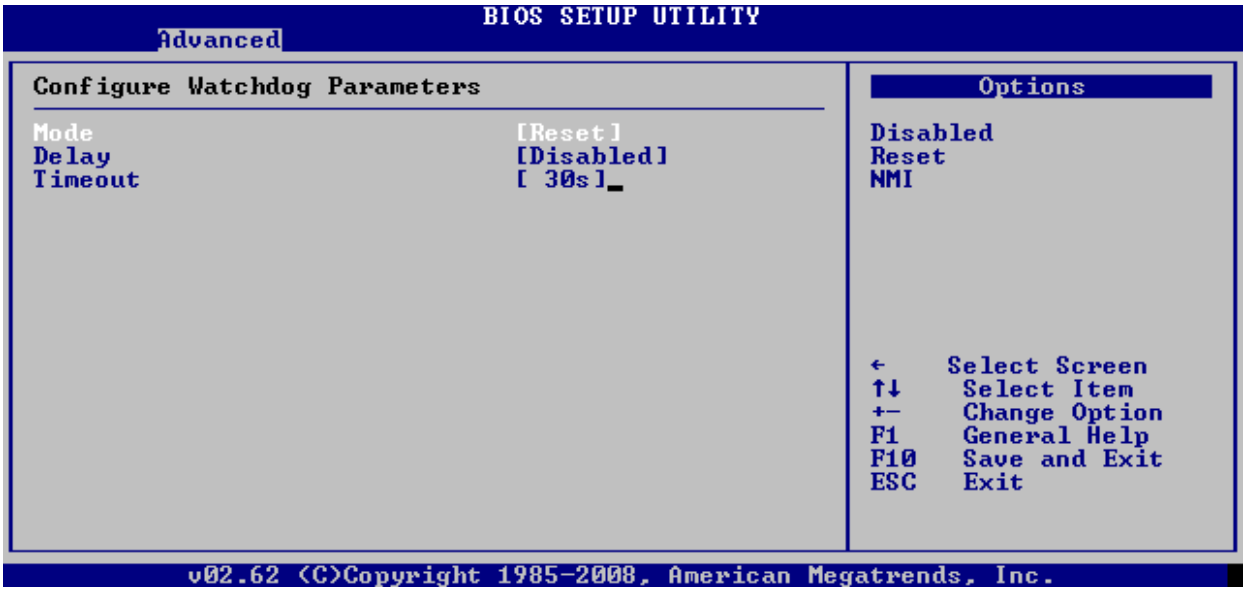
Feature	Option	Description
H/W Health Function	**Enabled** Disabled	Enables Hardware Health Monitoring Device on baseboard.

Miscellaneous



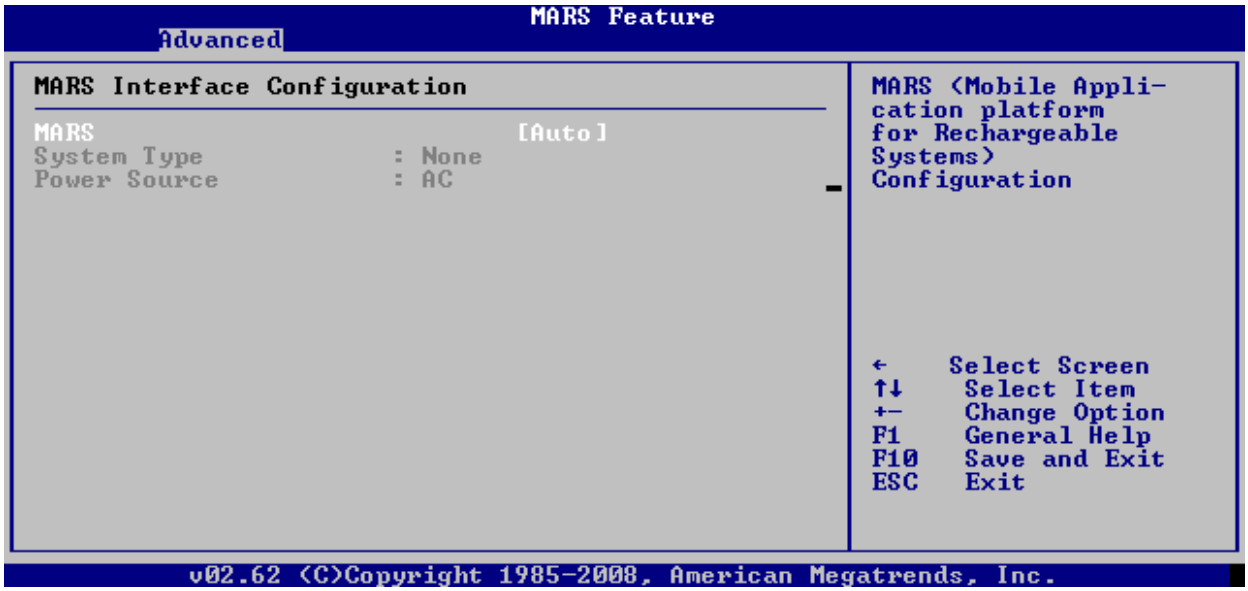
Feature	Option	Description
▸ Watchdog	Submenu	
▸ MARS Interface Configuration	Submenu	
Spread Spectrum	**Disabled** LVDS Core Both	Enables or Disables spread spectrum for the selected Clocks. LVDS: Enables LVDS Spread Spectrum Core: Enables CPU, PCIe, Chipset Spread Spectrum
A20 line controlled by	**Auto Detection** Legacy Keyb Ctrl. Port 92h / emul.	This setting allows to choose how address line A20 is controlled for legacy systems. If 'Keyb. controller' is chosen an active KBC is needed
Keyboard Crisis Recovery	**Enabled** Disabled	Enables or Disables Crisis Recovery by USB Keyboard Hotkey. 'Disabled' saves boot time (up to 2s) but no recovery functions are active.
S5 Eco	**Disabled** Enabled	Enables and Disables the S5 Eco Feature.

Miscellaneous - Watchdog



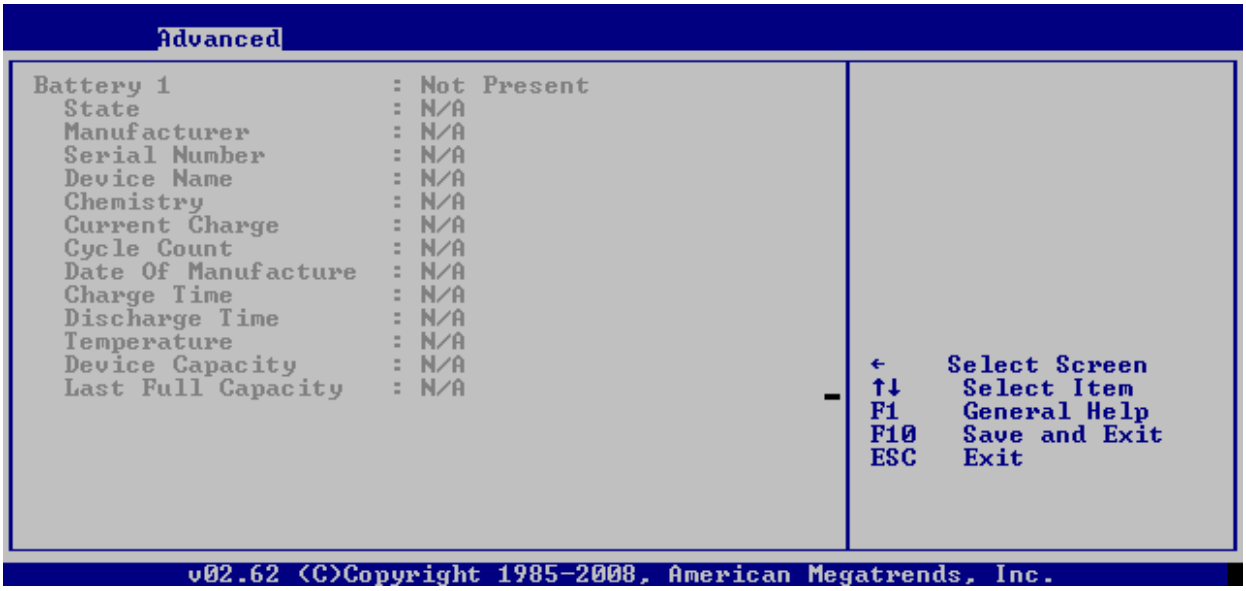
Feature	Option	Description
Watchdog Mode	**Disabled** Reset NMI	Enables / disables Watchdog
Delay	**Disabled** 1s 5s 10s 30s 1:00m 5:00m 10:00m 30:00m	Set the delay before the Watchdog gets active
Timeout	0.4s 1s 5s **10s** 30s 1:00m 5:00m 10:00m	Set the timout for Watchdog Reset mode

Miscellaneous - MARS Interface Configuration

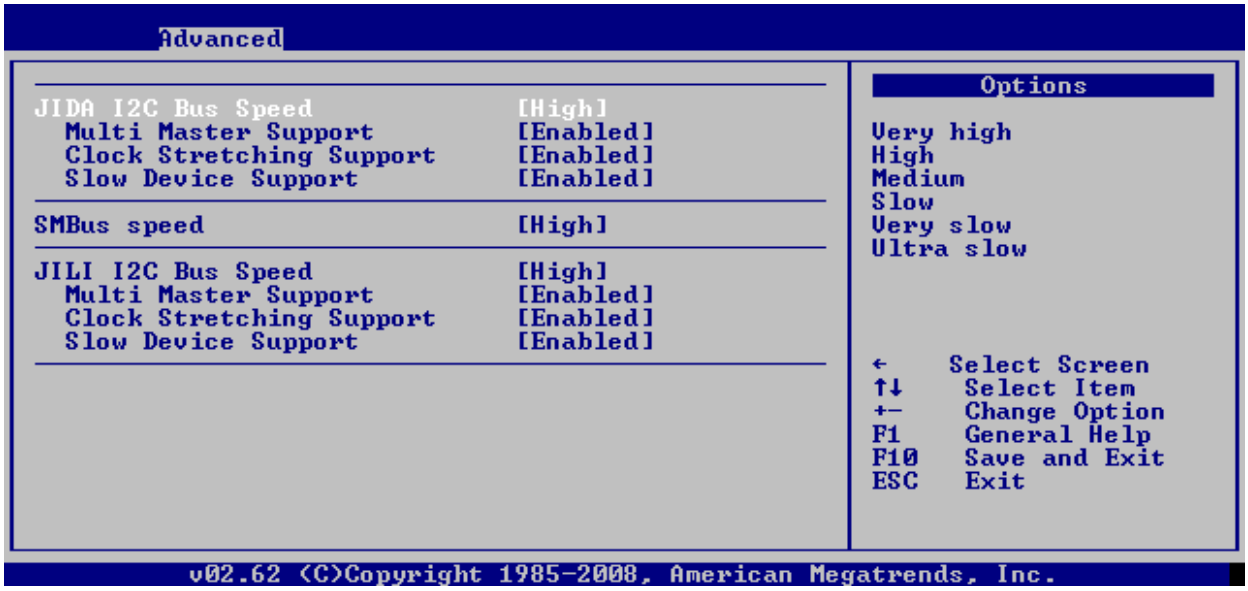


Feature	Option	Description
MARS	**Disabled** Auto SMB Charger SMB Manager	MARS (Mobile Application platform for Rechargeable Systems) configuration
▸ Battery 1	Submenu	Shows Battery Information if SMB Manager is present
▸ Battery 2	Submenu	Shows Battery Information if SMB Manager is present

Miscellaneous - MARS Interface Configuration - MARS Battery 1/2 Information



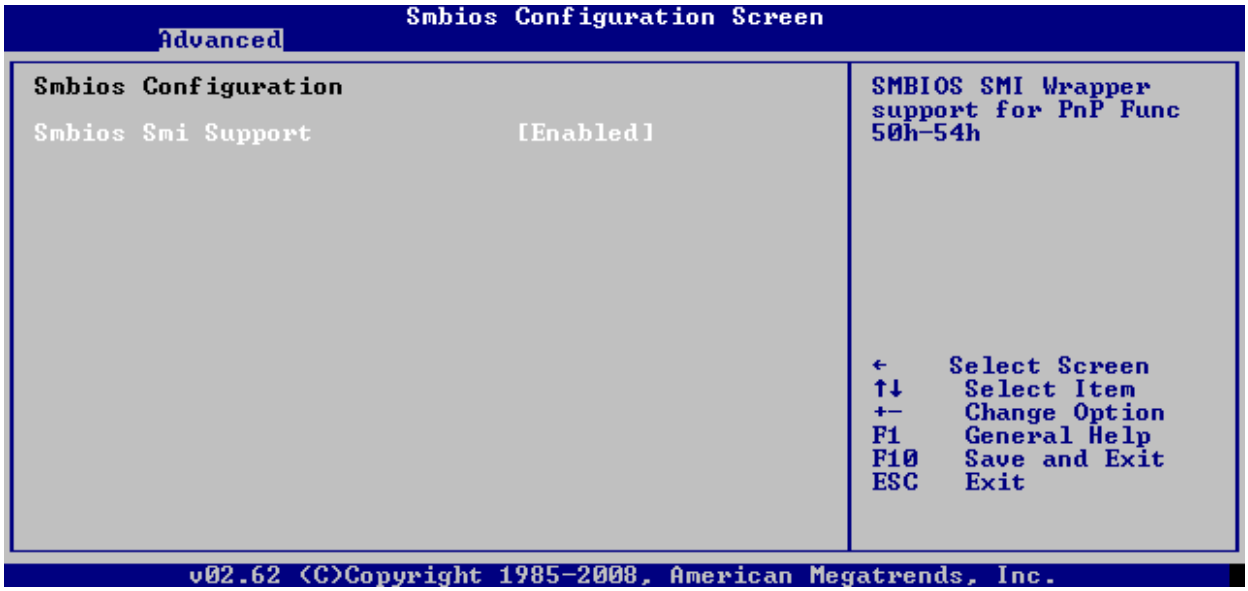
I2C Buses



Feature	Option	Description
JIDA I2C Bus Speed	**Very high** High Medium Slow Very slow Ultra slow	Select speed for JIDA/external I2C bus. See table below for speed settings.
Multi Master sup.	**Enabled** Disabled	Enables / disables I2C Multi Master Support
Clock Streching Sup.	**Enabled** Disabled	Enables / disables support for I2C clock stretching
Slow Device Support	**Enabled** Disabled	Enables / disables support for slow I2C devices
SMBus Speed	Extra high Very high **High** Medium Slow Very slow	Select SMBus Speed
JILI I2C Bus Speed	Very high **High** Medium Slow Very slow	Select speed for external JILI I2C on LVDS interface. See I2C speed table for values.
Multi Master sup.	**Enabled** Disabled	Enables / disables I2C Multi Master Support
Clock Streching Sup.	**Enabled** Disabled	Enables / disables support for I2C clock stretching
Slow Device Support	**Enabled**	Enables / disables support for slow I2C devices

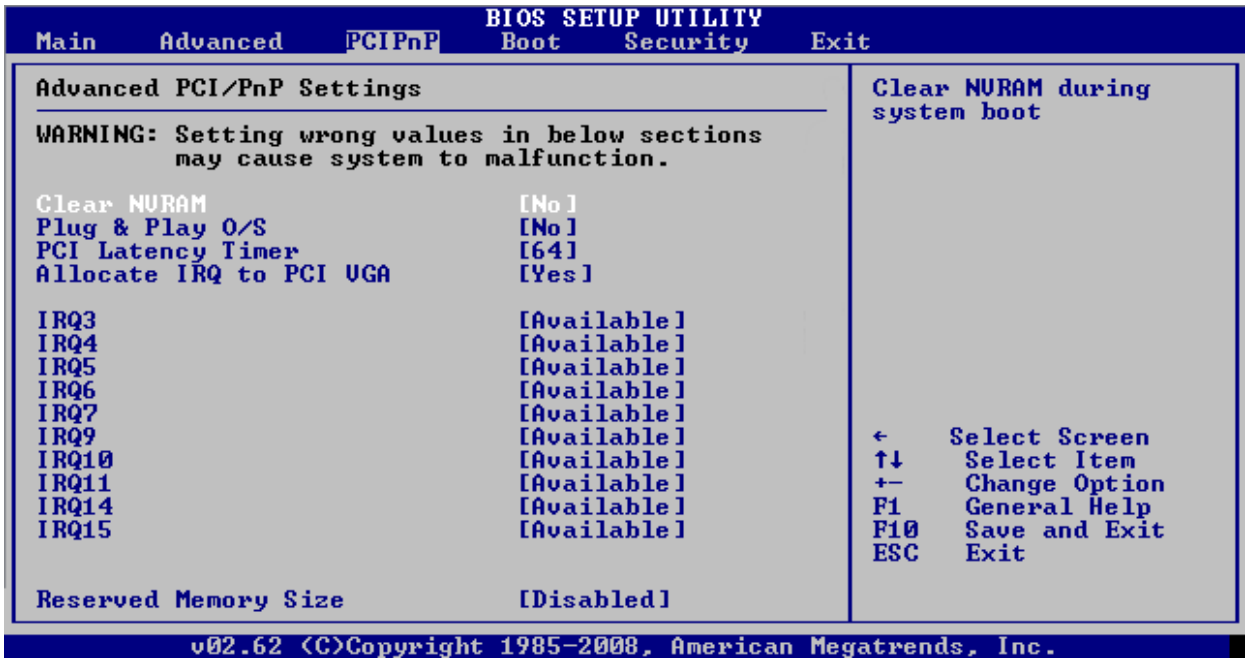
	Disabled	

SMBIOS Configuration



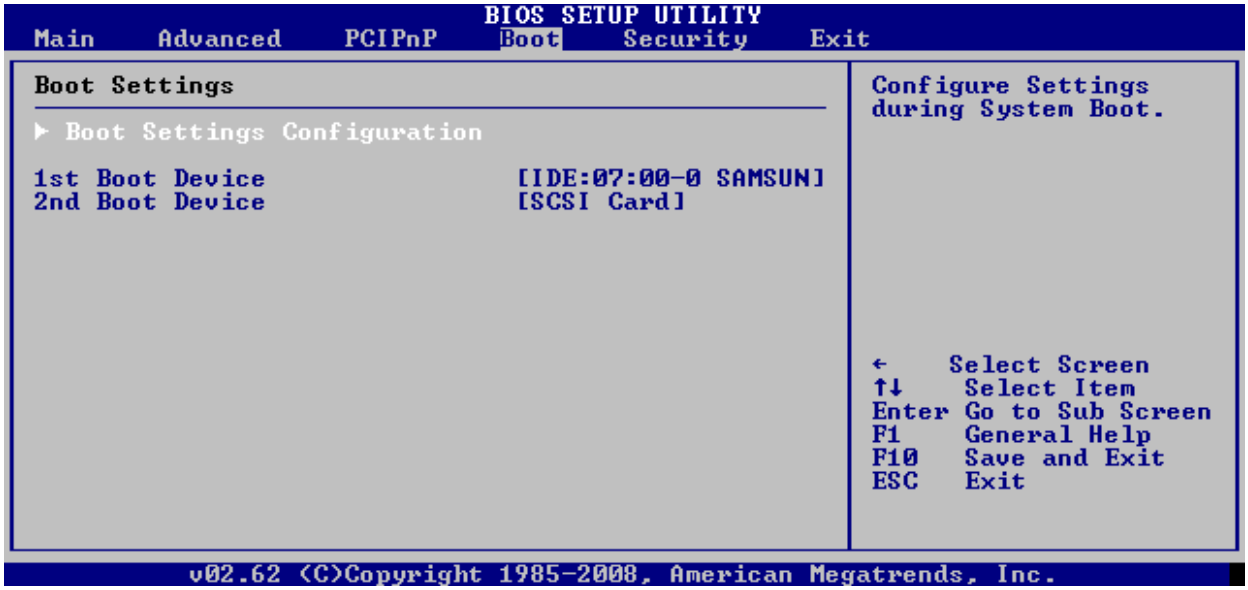
Feature	Option	Description
Smbios Smi Support	**Enabled** Disabled	SMBIOS SMI Wrapper support for PnP Func 50h-54h

8.3.4 PCI/PnP Settings



Feature	Option	Description
Clear NVRAM	**No** Yes	Clear NVRAM (None Volatile RAM) during system boot
Plug & Play O/S	**No** Yes	No: letzs the BIOS configure all the devices in the system Yes: lets the OS configure PnP devices not required for boot if your system has a Plug and Play OS
PCI Latency Timer	32 **64** 96 128 160 192 224 248	Set this value to allow the Master Latency Timer to be adjusted. This option sets the la- tency of most PCI devices
PCI IDE Busmaster	Disabled **Enabled**	If enabled improves the performance of the IDE interface for some operating systems (e.g. DOS)
IRQ3 IRQ4 IRQ5 IRQ7 IRQ9 IRQ10 IRQ11 IRQ15	**Available** Reserved	Reserved means that this interrupt is a legacy IRQ (not shared). Available defines that this interrupt can be used as a PCI IRQ
Reserved Memory Size	**Disabled** Enabled	Size of memory block to reserve for legacy ISA devices

8.3.5 Boot Settings

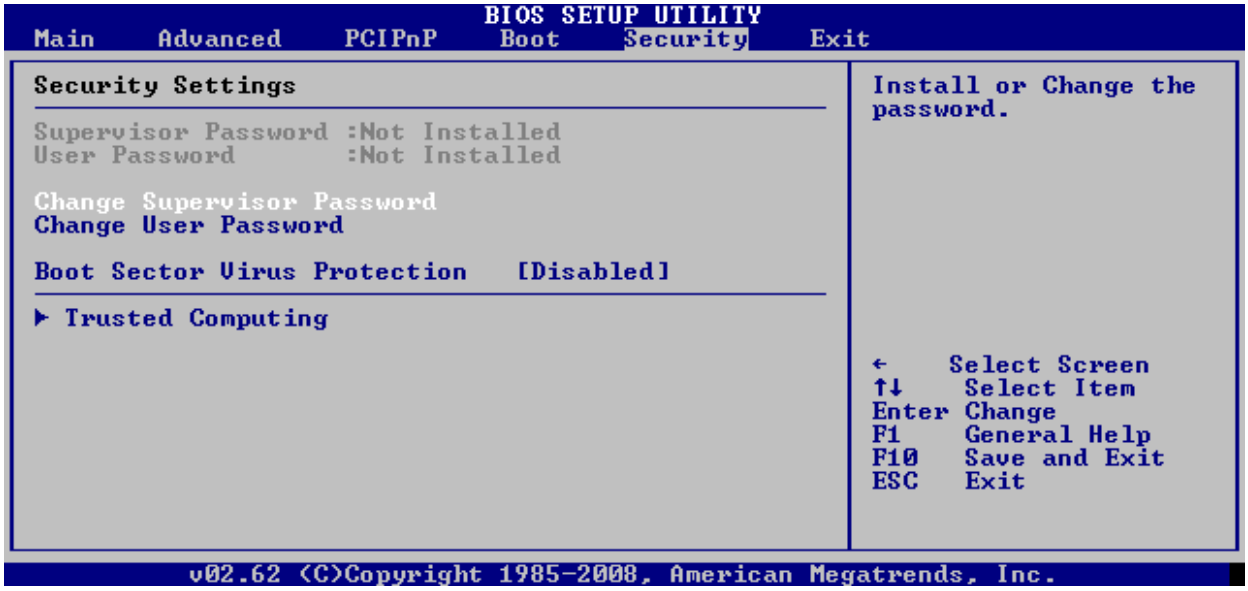


Feature	Option	Description
▸ Boot Settings Configuration	Submenu	Defines some special boot settings
1st Boot Device	Submenu	Specifies the 1st boot device
2nd Boot Device	Submenu	Specifies the 2nd boot device
3rd Boot Device	Submenu	Specifies the 3rd boot device

Boot Settings Configuration

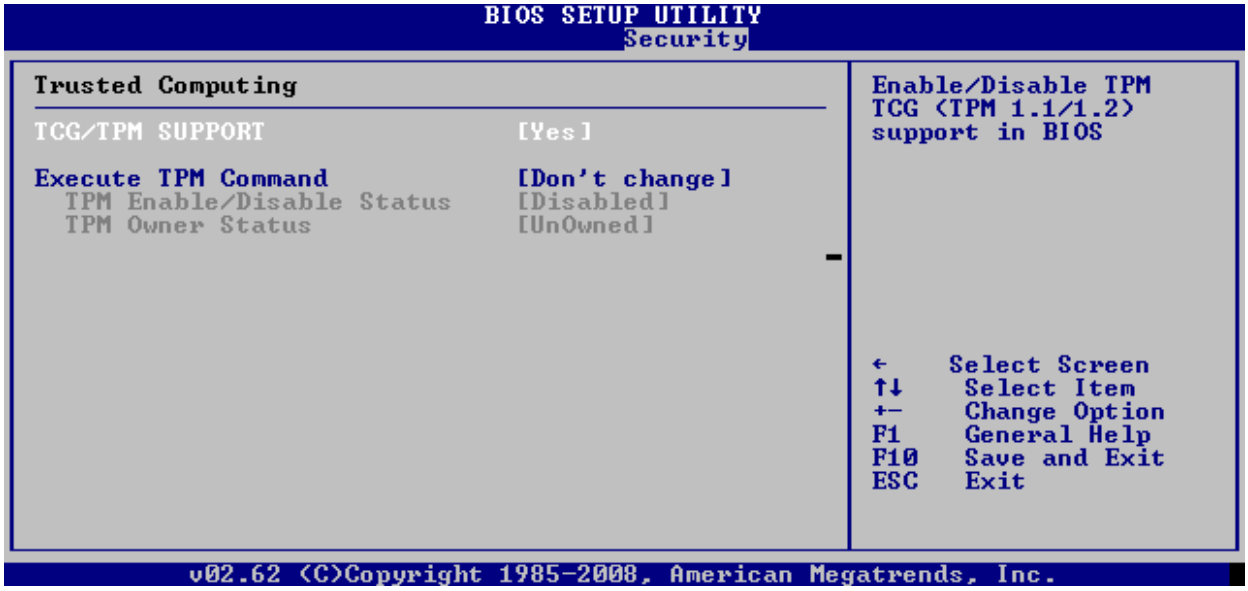
Feature	Option	Description
Quick Boot	Disabled **Enabled**	Allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system
Quiet Boot	**Disabled** Enabled	If disabled the BIOS generates the normal messages, otherwise an OEM logo can be displayed
AddOn ROM Display Mode	**Force BIOS** Keep Current	Keep Current keeps the current display mode. Force BIOS switches to BIOS mode before an AddOn ROM is called
Bootup Num-Lock	Off **On**	Select power-on state for Numlock
PS/2 Mouse Support	Disabled Enabled **Auto**	If disabled or no PS/2 mouse is found (Auto) the BIOS frees up IRQ12
Wait For F1 If Error	Disabled **Enabled**	Enabled allows the BIOS to wait for any error. If an error is detected, pressing <F1> will enter the setup and the BIOS settings can be adjusting to fix the problem
Boot USB HDD First	**Disabled** Enabled	If enabled, boots new attached USB HDD first. If disabled, sets new attached USB HDD to last boot position.
'Press DEL' Message Display	Disabled **Enabled**	Enabled allows the BIOS to display the message Press DEL to run Setup after memory initialization. Disabled suppresses this message
Interrupt 19h Capture	**Disabled** Enabled	If enabled AddOn ROMs can be trapped interrupt 19h (Boot IRQ). This option would make sense when using network boot (PXE ROM)

8.3.6 Security Settings



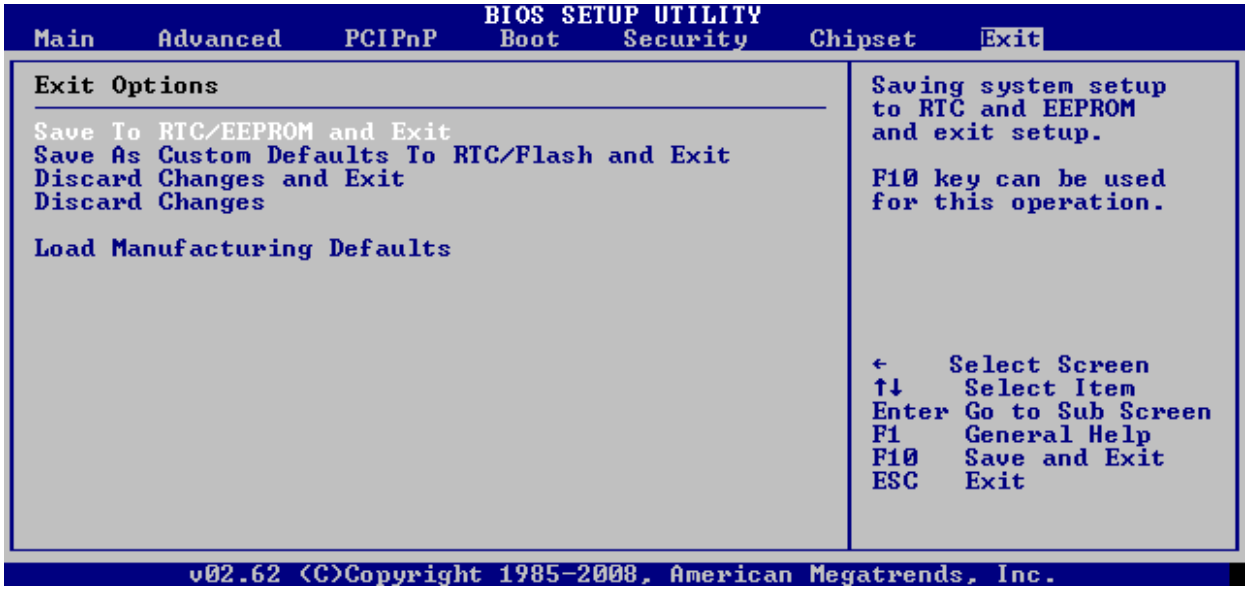
Feature	Option	Description
Change Supervisor Password		Select this option and press Enter to change the supervisor password
Change User Password		Select this option and press Enter to change the user password
Boot Sector Virus Protection	**Disabled** Enabled	If a program or a virus accesses the boot sector a warning appears if the option is enabled
▸ Trusted Computing	Submenu	

Trusted Computing



Feature	Option	Description
TCG/TPM SUPPORT	**NO** YES	Enable/Disable TPM/TCG support in BIOS
Execute TPM Command	**Don't change** Disabled Enabled	Allows to change the TPM's state to enabled as well as disabled. Don't change keeps the state as it is

8.3.7 Exit Options



Feature	Description
Save To RTC/EEPROM and Exit	Saving system setup to RTC and EEPROM and exit setup. F10 key can be used for this operation
Save As Custom Defaults To RTC/Flash and Exit	Saving system setup as custom defaults to RTC and Flash and exit setup. F11 key can be used for this operation
Discard Changes and Exit	Exit system setup without saving any changes. ESC key can be used for this operation
Discard Changes	Discards changes done so far to any of the setup questions. F7 key can be used for this operation
Load Manufacturing Defaults	Load manufacturing default values for all the setup questions. F9 key can be used for this operation

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